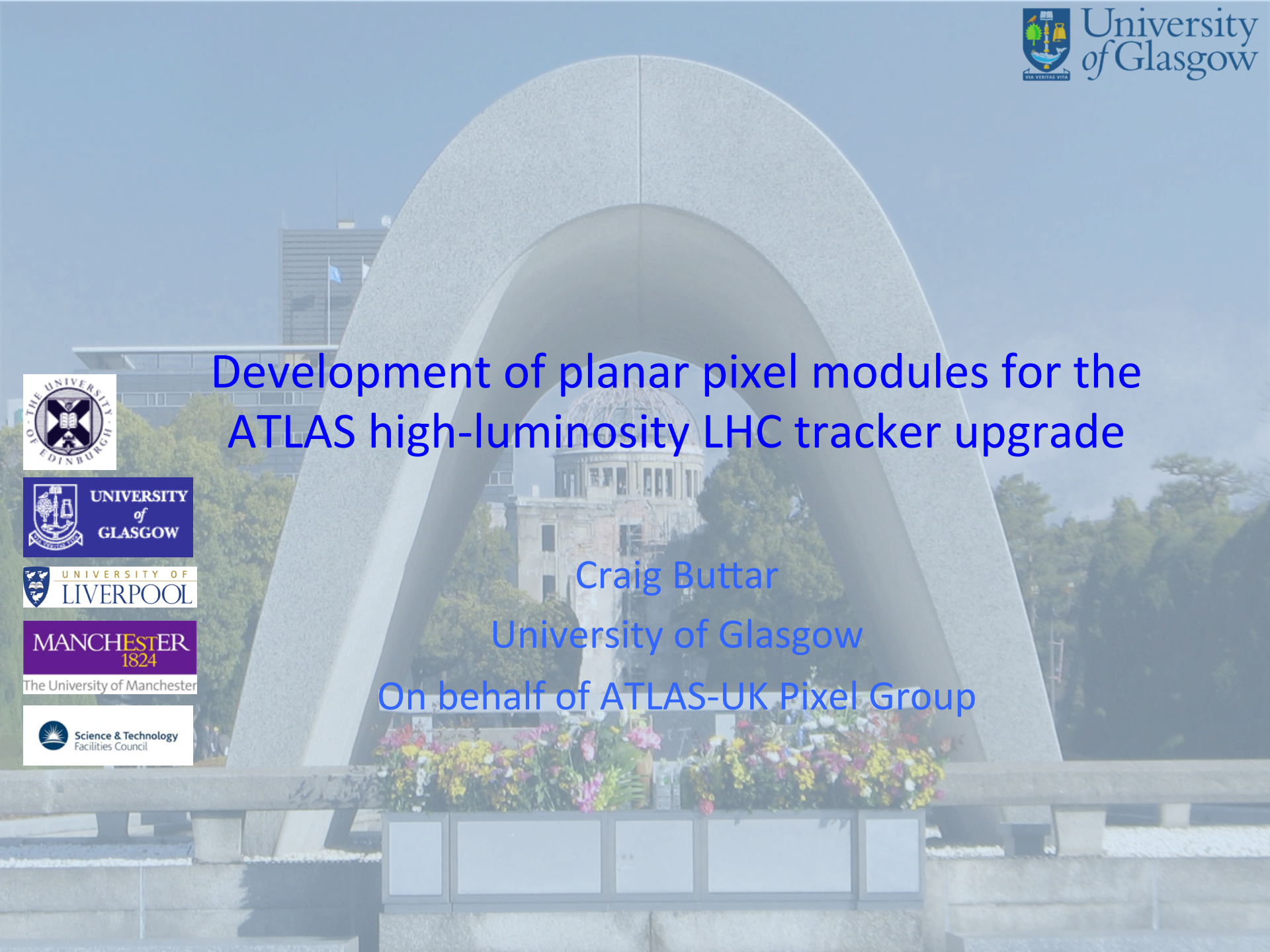


Development of planar pixel modules for the ATLAS high-luminosity LHC tracker upgrade

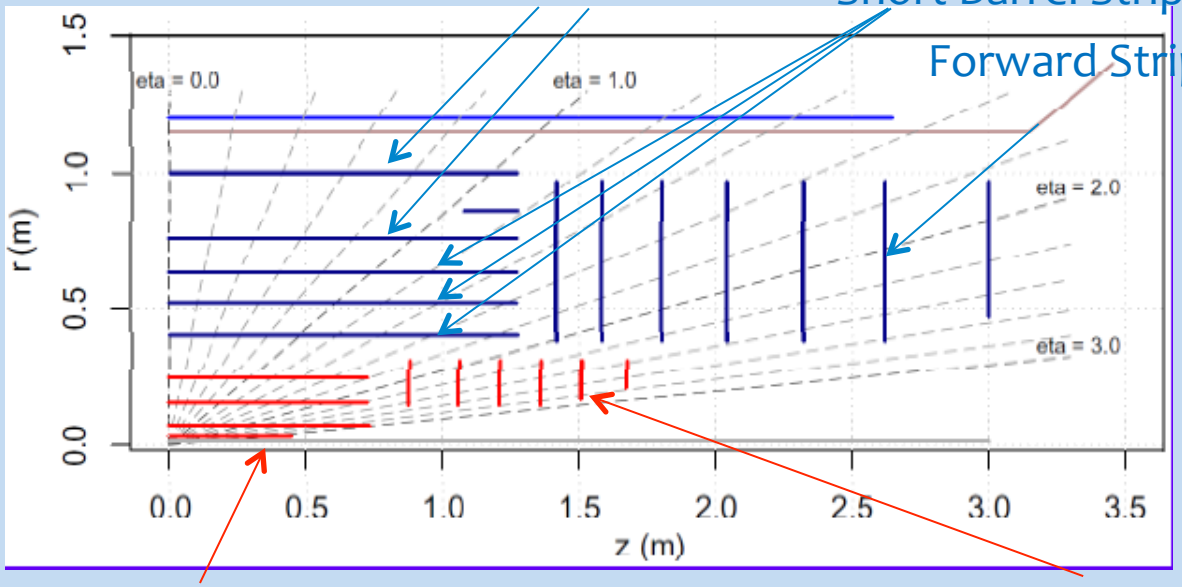
Craig Buttar

University of Glasgow

On behalf of ATLAS-UK Pixel Group

ATLAS Phase-II Tracker Upgrade

All-silicon inner detector (strips + expanded pixel system)



Occupancy for
<μ>=200 (in %)

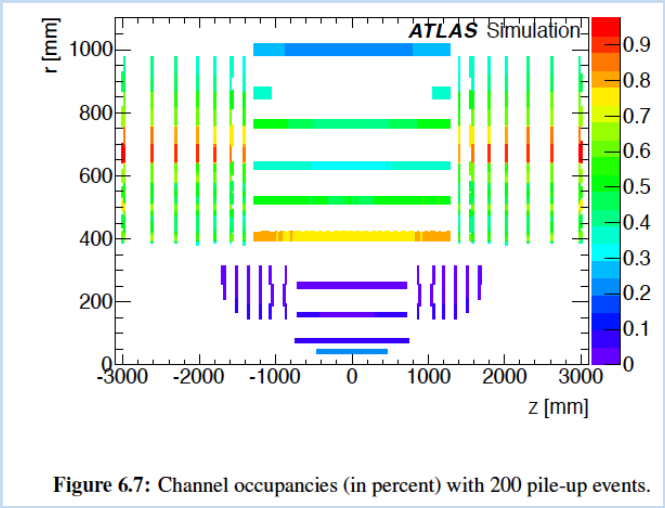


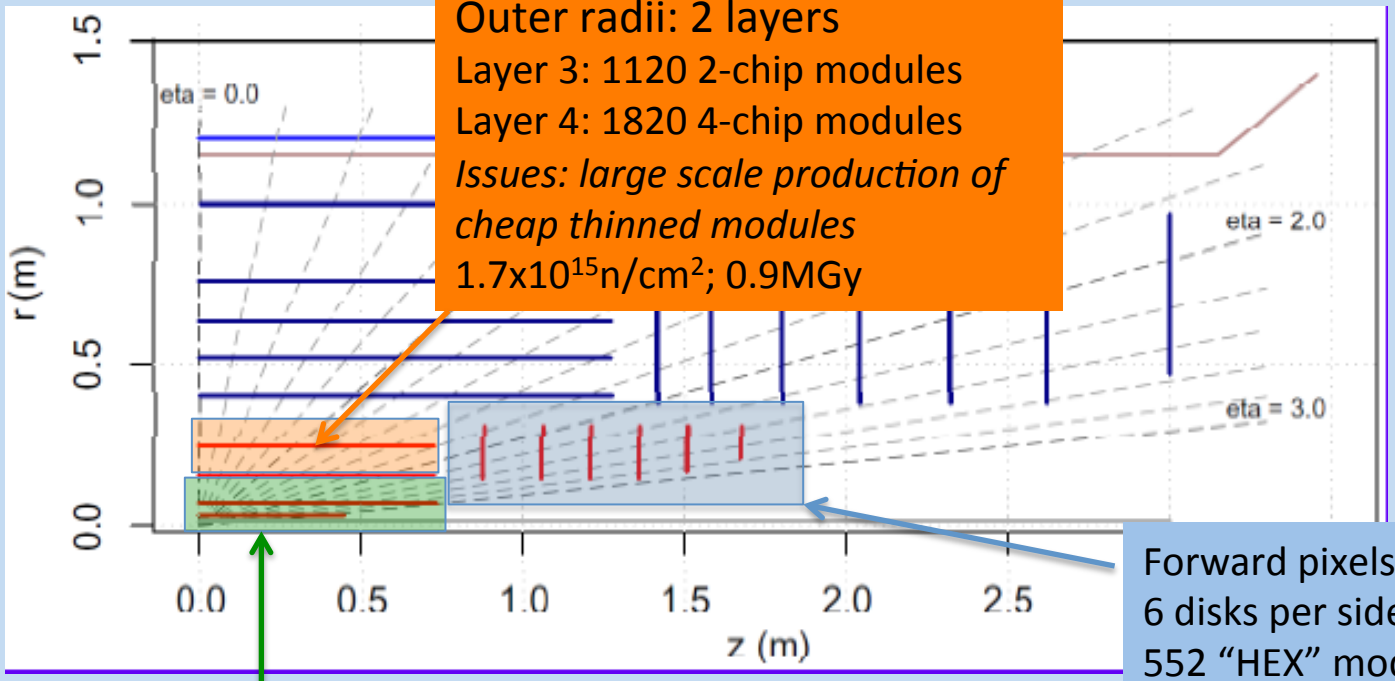
Figure 6.7: Channel occupancies (in percent) with 200 pile-up events.

Baseline LoI layout of the new ATLAS inner tracker for HL-LHC
Aim to have at least 14 silicon hits everywhere (robust tracking)

ATLAS Letter of Intent
CERN-2012-022
LHCC-I-023

Phase-II pixel system in numbers

ATLAS Letter of Intent
CERN-2012-022
LHCC-I-023



Outer radii: 2 layers
Layer 3: 1120 2-chip modules
Layer 4: 1820 4-chip modules
Issues: large scale production of cheap thinned modules
1.7×10^{15}n/cm^2; 0.9MGy

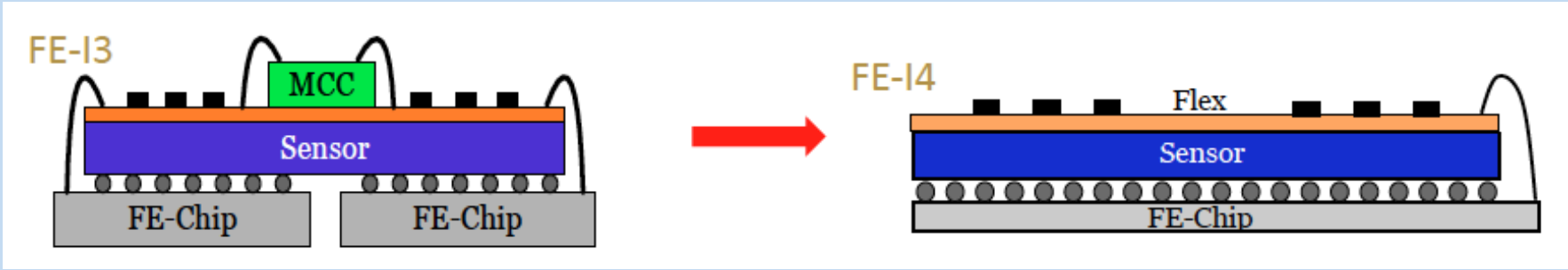
Forward pixels
6 disks per side
552 "HEX" modules
280 "QUAD" modules
Issues: large scale production of cheap thinned modules
1.8×10^{15}n/cm^2; 0.9MGy

Inner radii: 2 layers
Layer 1: 352 2-chip modules
Layer 2: 576 4-chip modules
Issues: radiation damage & small pixels
1.4×10^{16}n/cm^2; 7.7MGy

Outer radii pixel system

- Pixel modules should be
  - Large with high active fraction
  - Small contribution to material budget
  - Radiation tolerant
  - Highly granular
  - Optimised for production

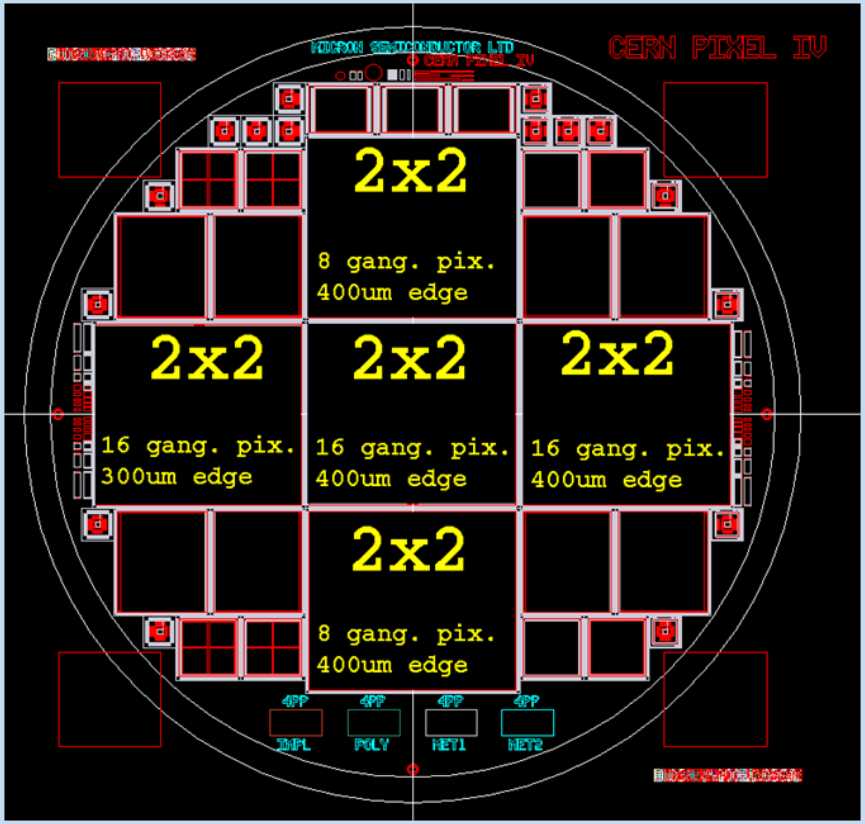
- 2 outer Barrel layers & Disks
  - Sensor planar n-in-p
  - Match to FE-I4 geometry ~2x2cm^2
  - Pixel size 50 µm x 250 µm
  - *2x2 FE-I4 (Quad) ~4x4cm^2*
  - Aim for sensor & ROIC thickness ~150 µm



Current ATLAS

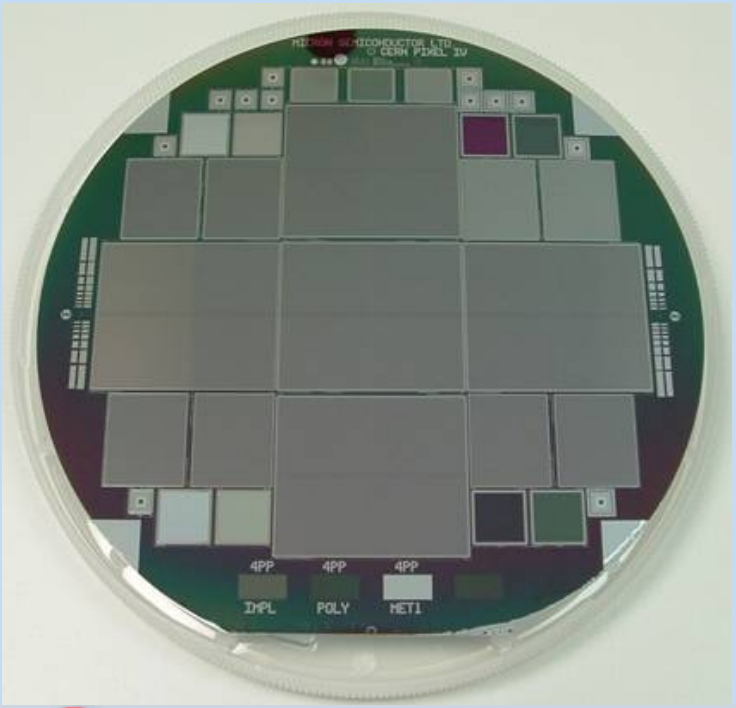
Phase-II upgrade ATLAS

Quad sensor design



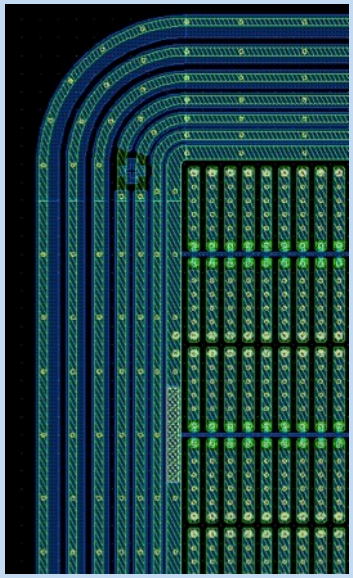
Sensor type:
SC1, SC2 – "test" 450 µm edge.
SC3, SC4 – 500x25, 450 µm edge.
SC5 – **SC8** "test", 300 µm edge.
SC6 – **SC7** "production", 300 µm edge.
QUAD1 – "production", 450 µm edge.
QUAD2 – "test", 300 µm edge.
QUAD3 – "test", 450 µm edge.
QUAD4 – "test", 450 µm edge.
QUAD5 – "production" 450 µm.

Quad sensor design

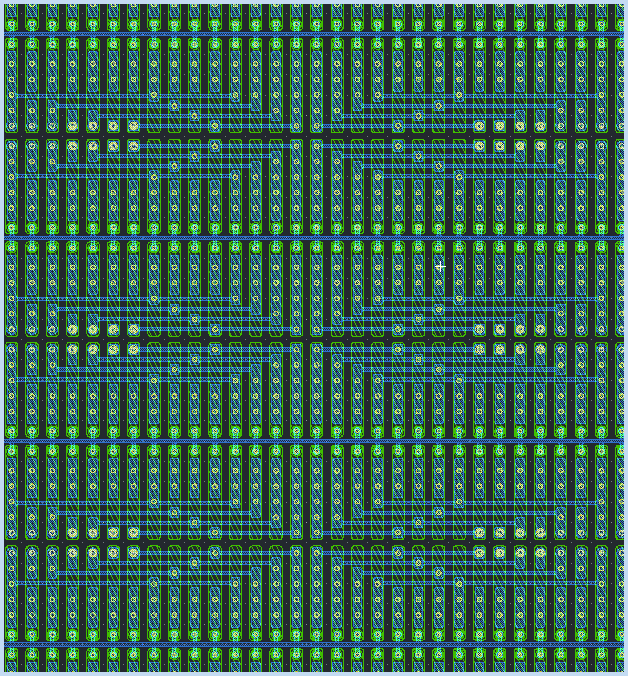


MICRON SEMICONDUCTOR ltd

n-in-p on substrate with resistivity ~10kΩ
Quads are roughly 4x4cm



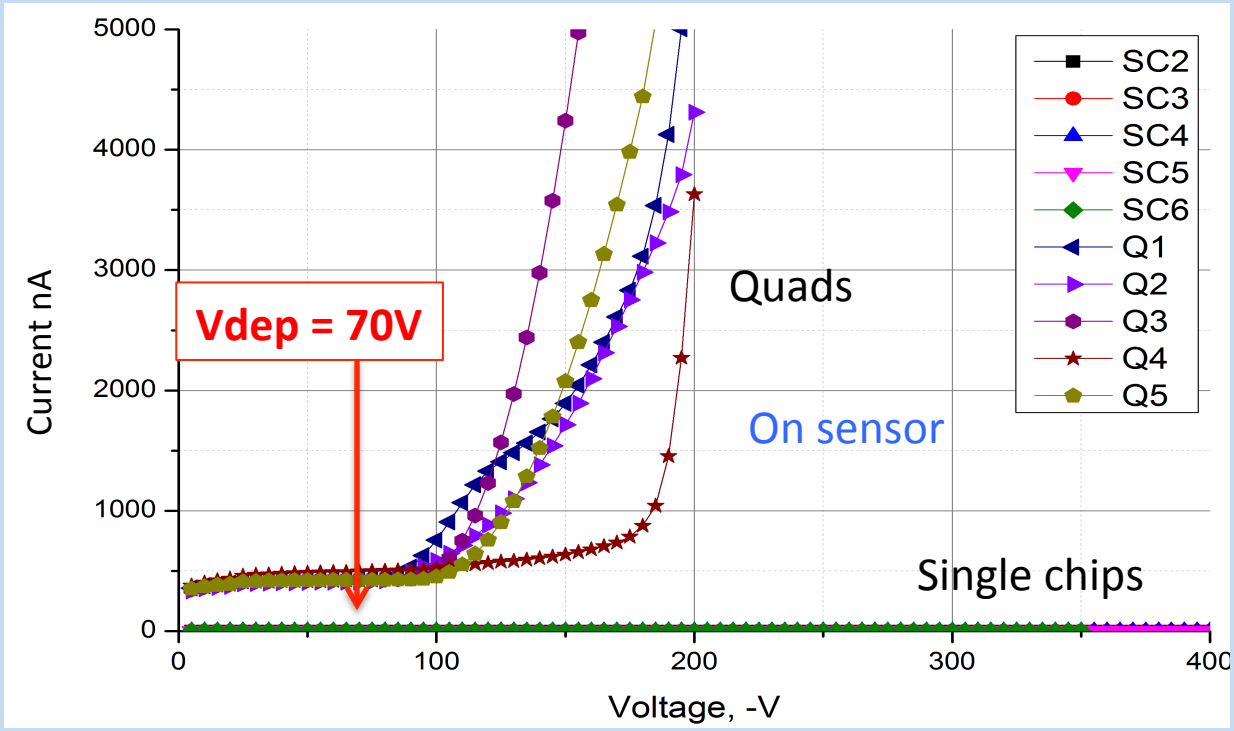
long pixels (250->500um) are used to maintain active sensor area active in vertical direction



Ganged pixels (multiple pixels per channel) used to maintain active sensor area along horizontal direction

Quad I-V characteristics

- 107,520 readout channels
- General silicon resistivity used ~10kΩ, 300μm thick
- Single and Quad FE-I4 compatible sensors
  Vdep = 70V
- No significant difference between 300μm and 450μm edges



- On sensor, using punchthrough biasing, IV measurements at -100V are around 500nA (~40nA/cm^2)
- Reduced to ~100nA with 4 ROC enabled @V=100V
  punch-through biasing is bypassed (~8nA/cm^2)
- Single chips ~3nA/cm^2

Sensor yield

Yield is determined for different processing runs, with different processing techniques performed to optimize production at Micron

Pass or failure of device depends on the current at V_{dep} + 50V = 130V <= 1.5µA with no sharp breakdown

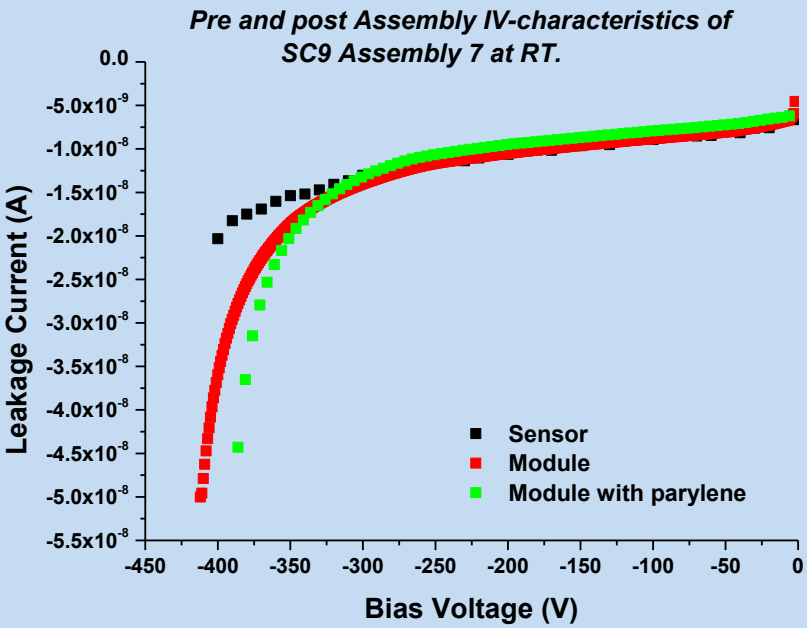
Batch No.	Quad- No. of Devices	Quad – Avg Yield	Single – No. of Devices	Single – AVG Yield
#1 - 2	40	55%	15	80%
#3	20	65%	20	81%
#4	20	60%	-	-
#5	30	80%	24	100%
#7	20	90%	28	100%
#8	35	97%	49	78%

N+ implant under dice street

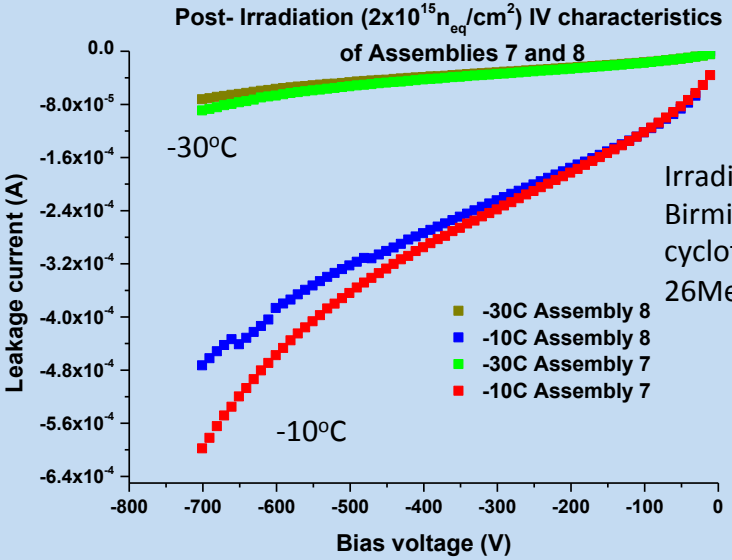
No implant at Dice street

P+ implant at Dice street

I-V characteristics



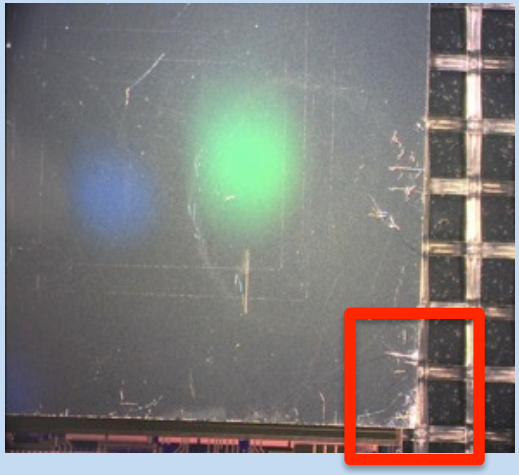
$\alpha(+20)\sim 4\times10^{-17}\,Acm^{-1}$



Irradiated at Birmingham cyclotron 26MeV protons

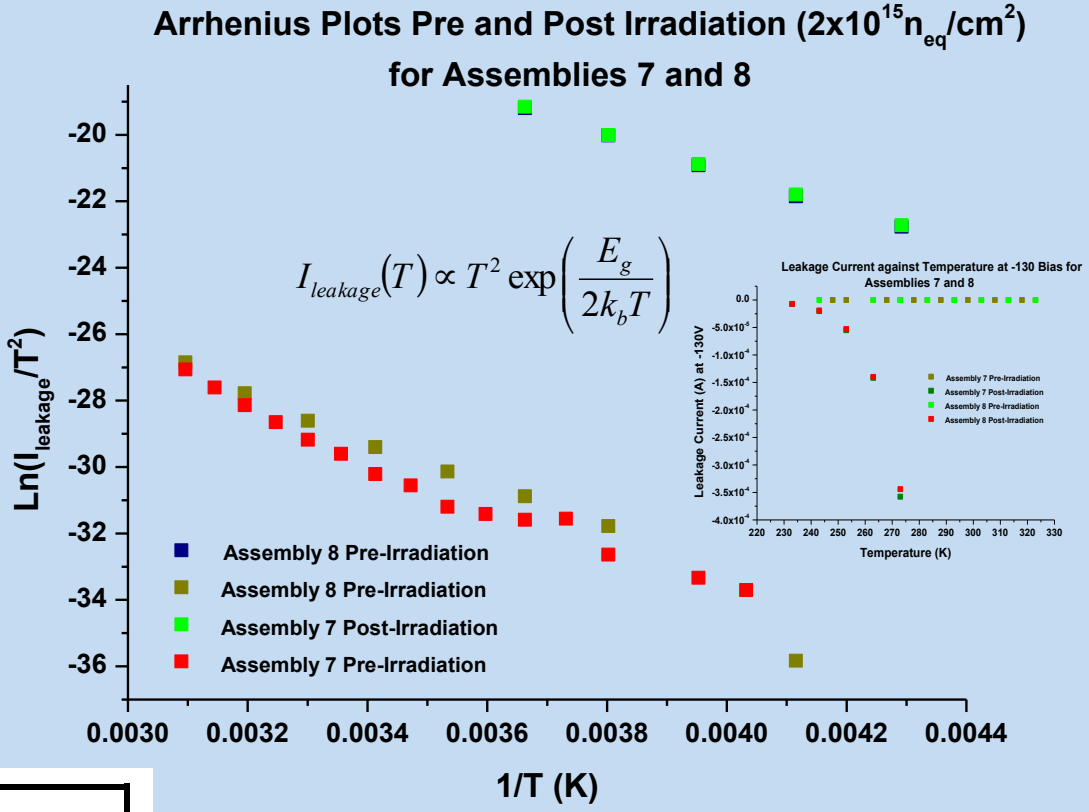
Add parylene coating to module to enhance resistance to breakdown

Assemblies sometimes have lower breakdown, possible damage during flip-chipping
Investigating dicing streets to avoid this issue



I-V characteristics

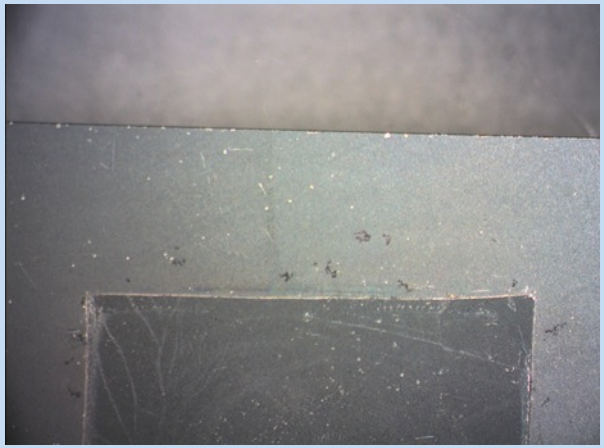
I-V measurements made on cooled chuck on probe station, investigate detector characteristics as a function of temperature



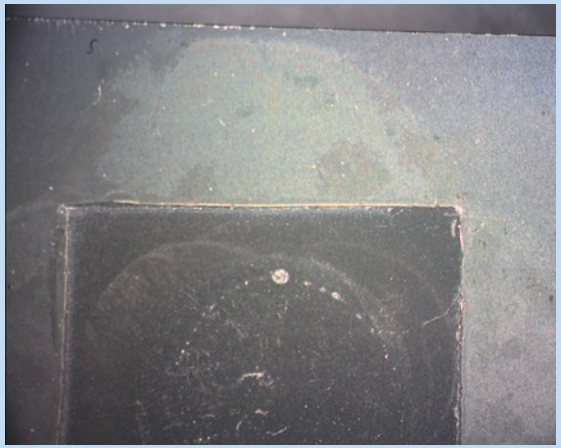
Assembly	*Band Gap Energy (eV)*	
	Pre-Irradiation	*Post-irradiation*
2	1.52	1.06
7	1.19	0.98
8	1.40	0.98

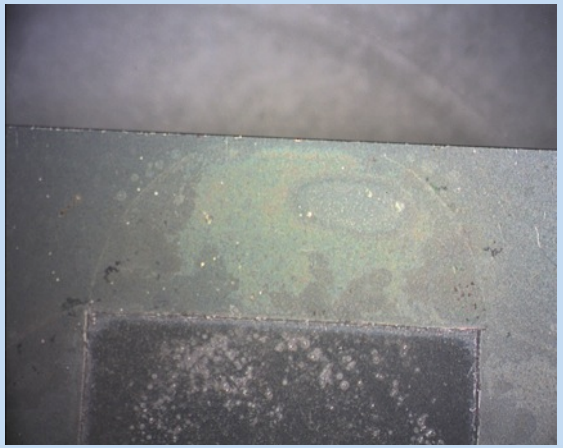
Effect of irradiation on parylene coatings

Visual inspection shows defects in parylene coatings at high dose
Possibly delamination at Al-parylene interface



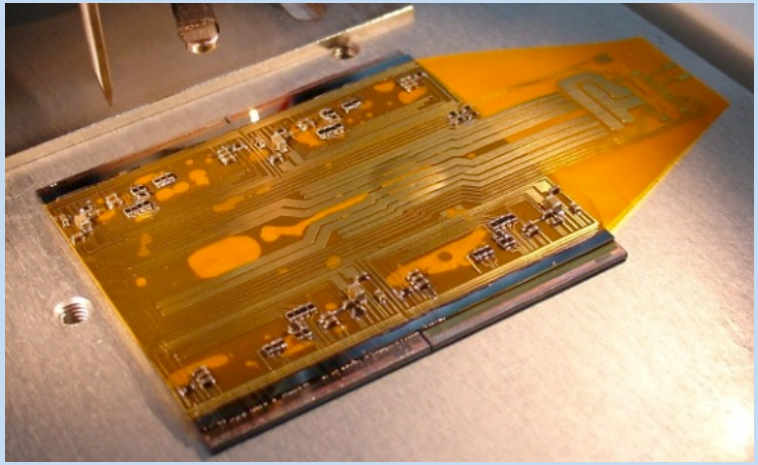
$2x10^{14}n_{eq}cm^{-2}$



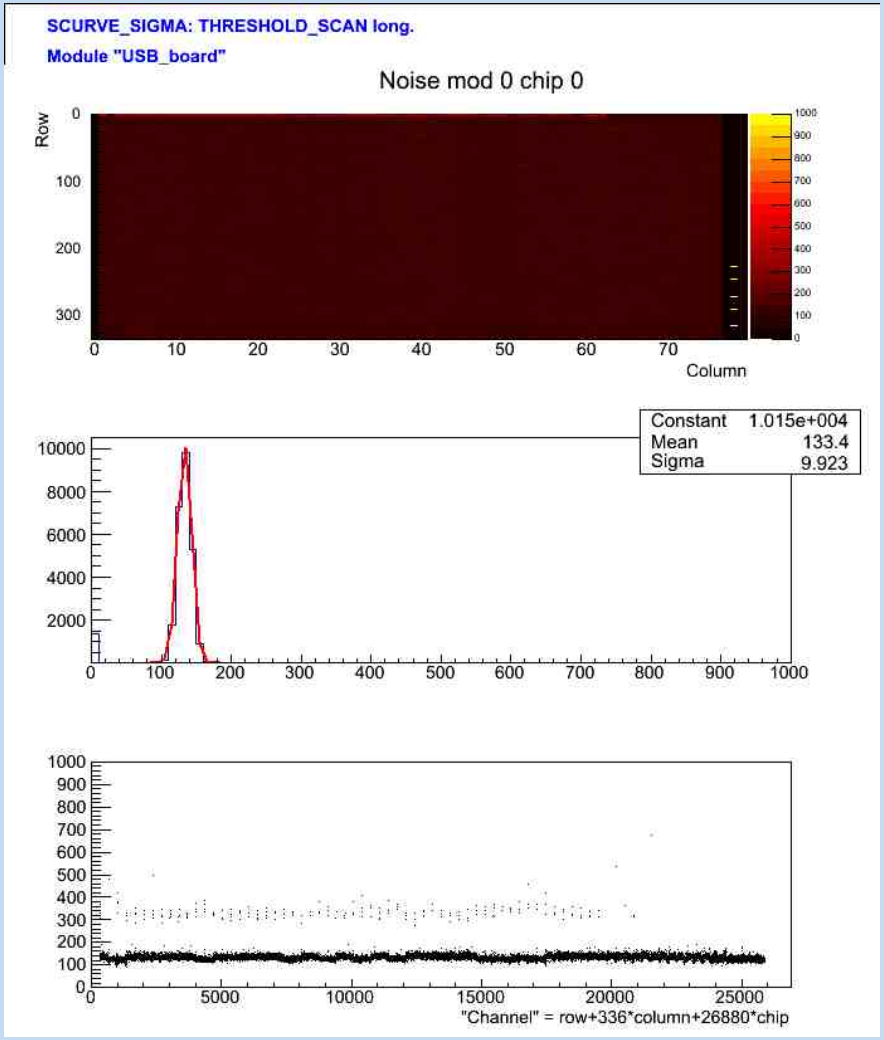


$2x10^{15}n_{eq}cm^{-2}$

Quad modules

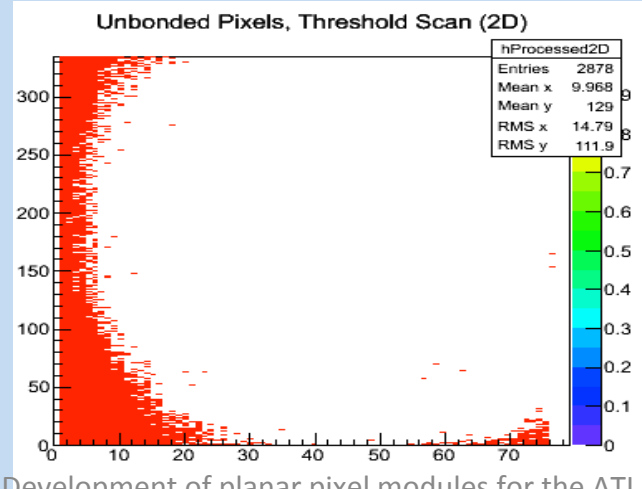


- Quad module assembly with thinned readout chip, using Bonn Flex hybrid
- Tuning of FE-I4 chip to 1600e @100V
- Mean noise = 133e
- Noise is comparable to single chip assemblies



Thinned module bump-bond yield

- Evaluated bond yield of thinned single chip and quad-module, using noise measurements and cross-talk
- All assemblies show issue with bump-bonding
- Large areas of non-bonded pixels at the corners & edges
  - Have 3% to 66% open bumps
- Good yield for full thickness devices

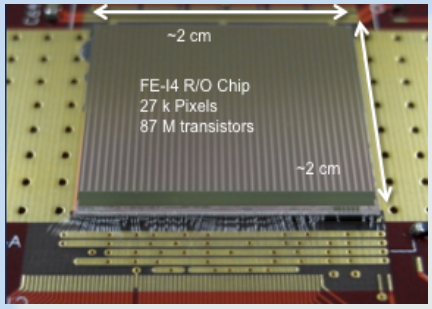


Bump Process Flow (VTT)

1. Deposit UBM and bumps on ROIC
2. Thin ROIC to 200 µm / Diced
3. On vacuum jigs perform flip-chip for tack bond
4. Re-flow in reducing atmosphere in oven (260C) unsupported assembly

Self-align bumps

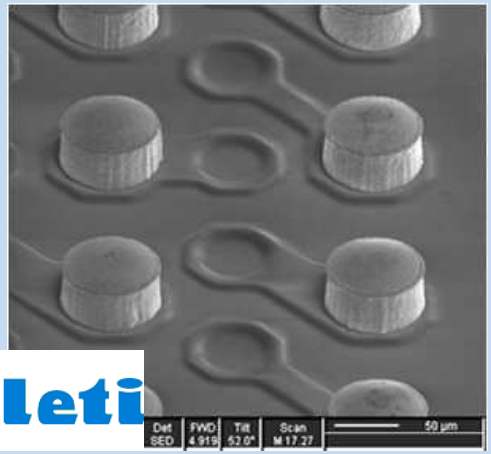
Obtain good electrical properties

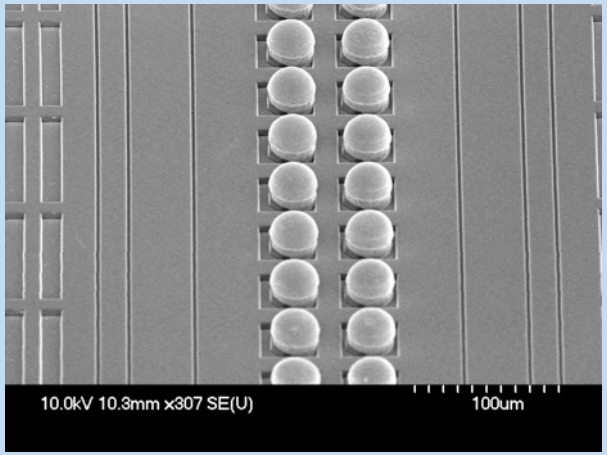


Issues with bump yield due to significant bowing of large readout chip

Bump bond development

- Investigate use of backside compensation with Cea-Leti to remove bowing issue
- Process FE-I4s:
  - Front side processing: UBM & micro pillars
  - Bond front side to carrier wafer
  - Thin
  - Backside deposition
  - Release front side
- UBM on sensors and flipping at Advacam



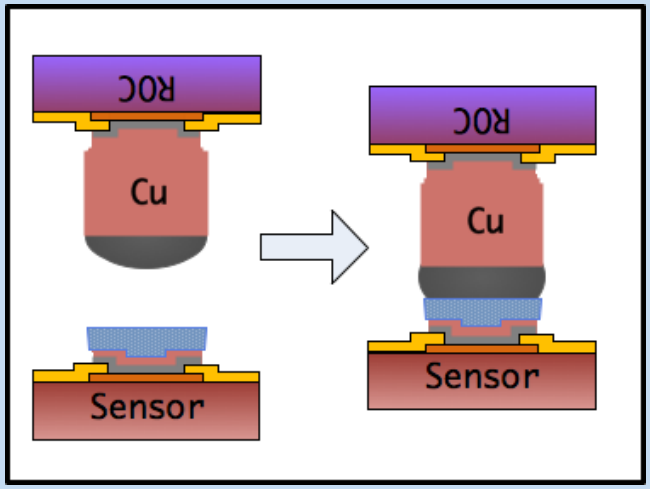


- UBM and Micro pillar
  - UBM
    - TiNiAu
    - 0.5 – 1.5µm
    - 40µm pitch
    - 20µm width (minimum)
  - Micro pillars
    - Cu post / SnAg Solder
    - 50µm pitch
    - 25µm diameter
    - 8-12µm thickness

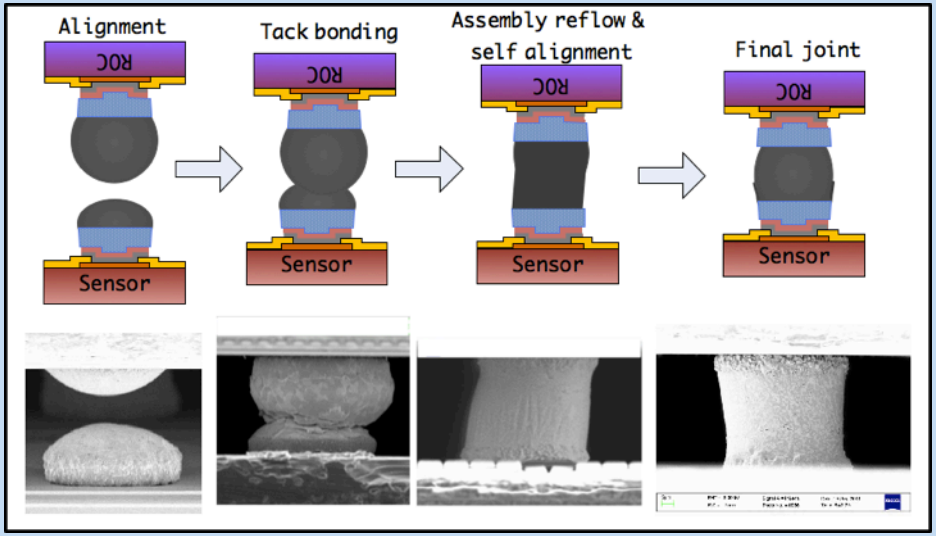
FE-I4B with micro-pillars

Bump-bonding programme

- Several different bump structures will be evaluated for FE-I4B modules:
  - Structure #1: ROC: Cu/SnAg (CEA LETI) – SC: Ni/SnPb (VTT)
    - to be avoided –mixing of different solder alloys
  - *Structure #2: ROC: Cu/SnAg (CEA LETI) – SC: thin film UBM (Advacam)*
  - Structure #3: ROC: Ni/SnPb (Advacam) – SC: thin film UBM (Advacam)
  - Structure #4: ROC: Ni/SnPb (VTT) – SC: Ni/SnPb (VTT)



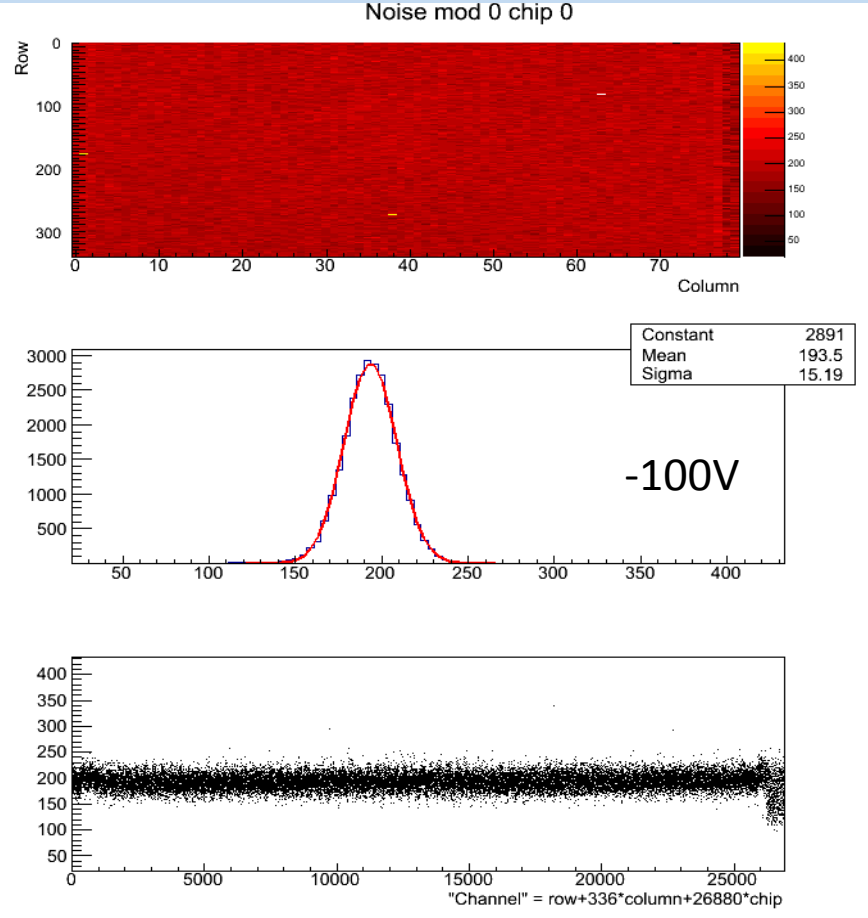
Structure #2, CEA LETI Cu pillars bonded against Pt UBM of Advacam



Structure #4, VTT solder bumps structure and assembly sequence

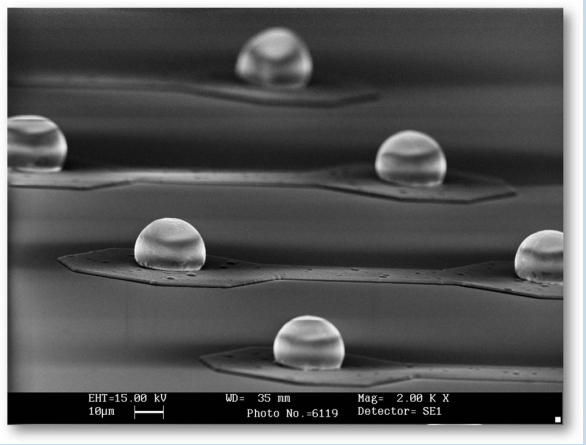
Bump-bond yield

- Set of single chip modules delivered (more in Helen Hayward's talk)
- *Preliminary* results for bond yield for structure 2
  - Structure #2: ROC: Cu/SnAg (CEA LETI) – SC: thin film UBM (Advacam)
- No thinning of sensor or FE-I4B wafers
- Bump yield for 2 modules measured from noise scans
- Yields are: >99.9%
- Other devices appear good from online testbeam plots



In based bump bonding at RAL

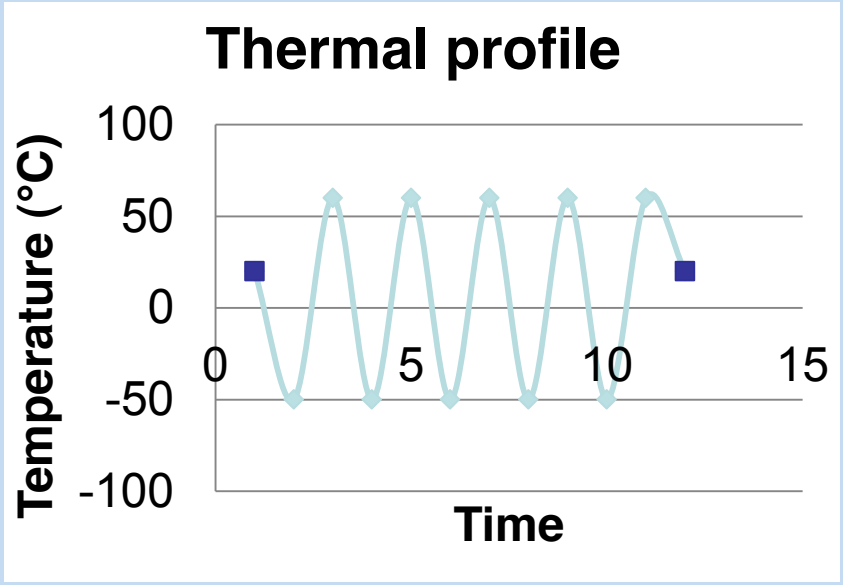
- In bump bonding can be done at low temperature, which would avoid issues with bowing of ROICs
- Indium process
  - currently developing cold (room temperature) compression
- Now have Cr/Ni based in-house UBM process
- 99.9% Electrical yield using daisy chain test structures
- Preparing FE-I4 daisy chains and to produce FE-I4 modules

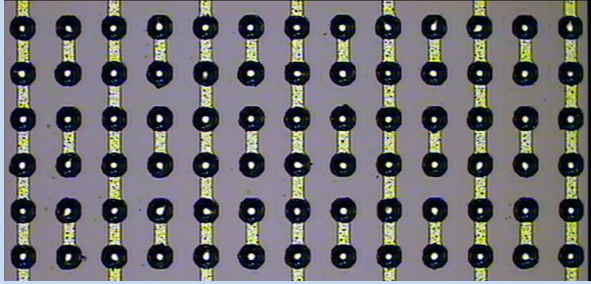


22micron bumps grown using evaporator and formed using reflow oven at RAL

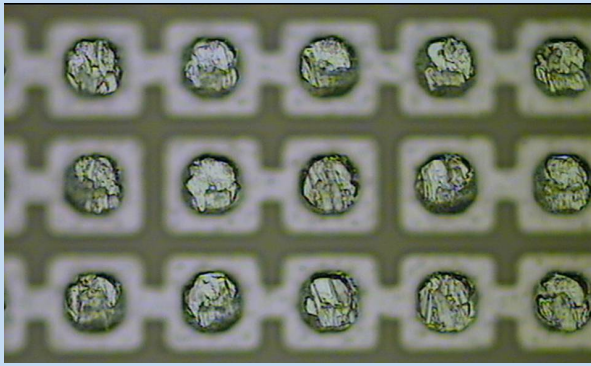
Mechanical characterisation

- Thermal cycling
  - Thermal cycle in dry N_2, Test chain resistance during cycles
  - 500 cycles -50 -> +60 degC, 120s per cycle
  - No defects introduced (testing 3 different bonding recipes with >3.5k bumps from each)





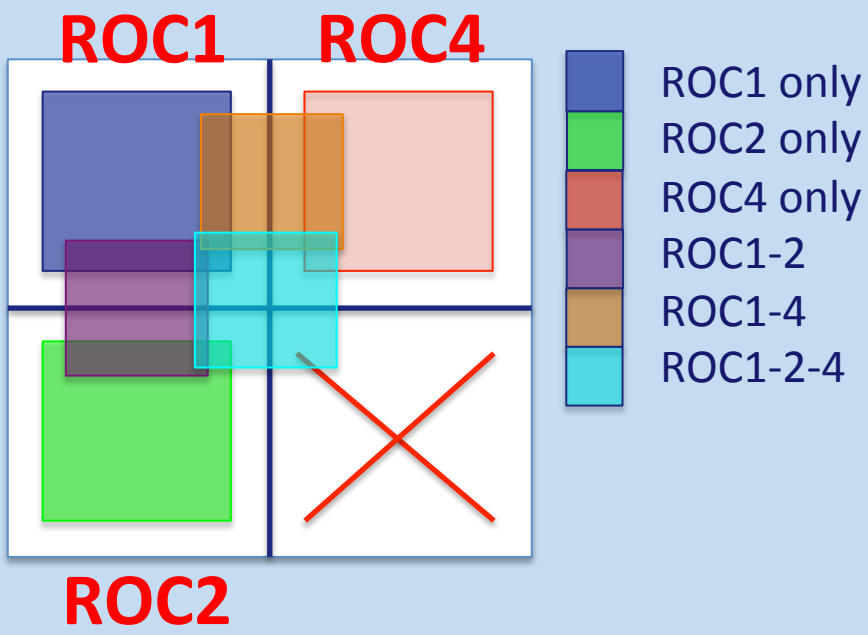
Bumped medipix geometry test device prior to bonding (bumps formed at RAL, CNM under bump metallization).

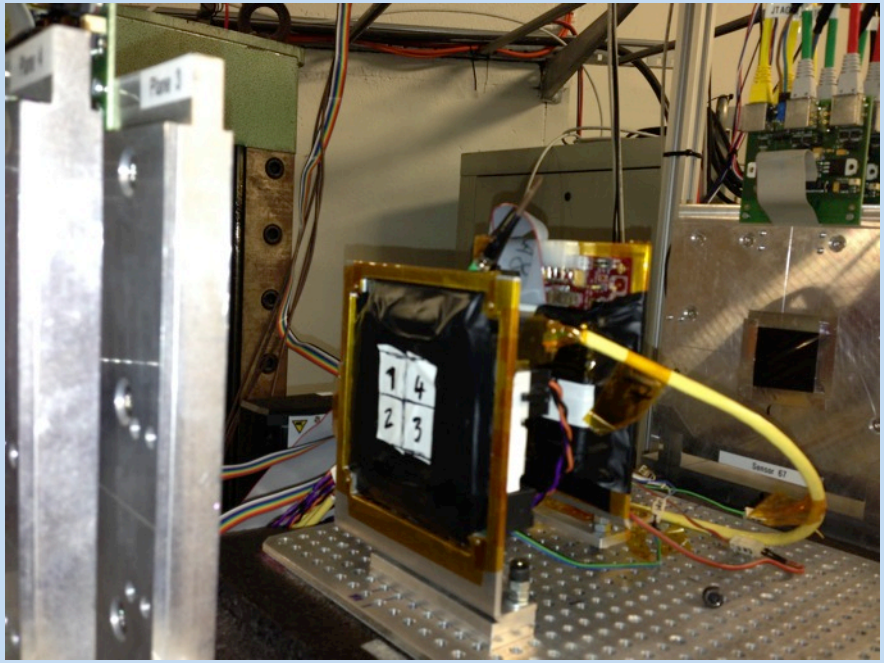


A medipix geometry test device after bonding and shear testing.
The rough finish of the bumps is evidence of successful bonding followed by shearing

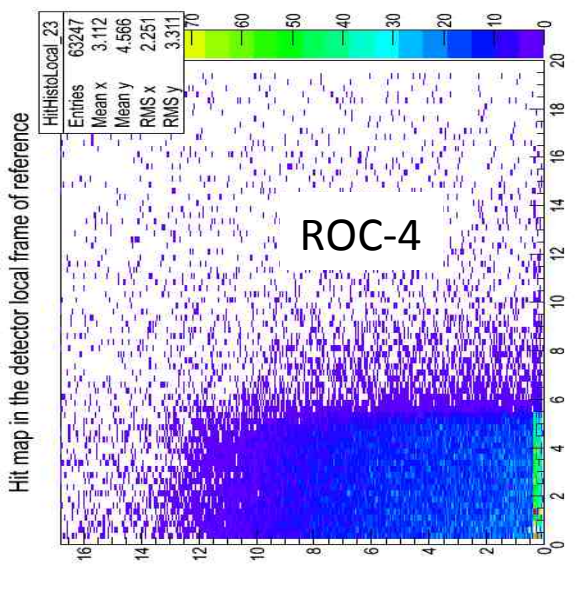
Quad testbeam measurements

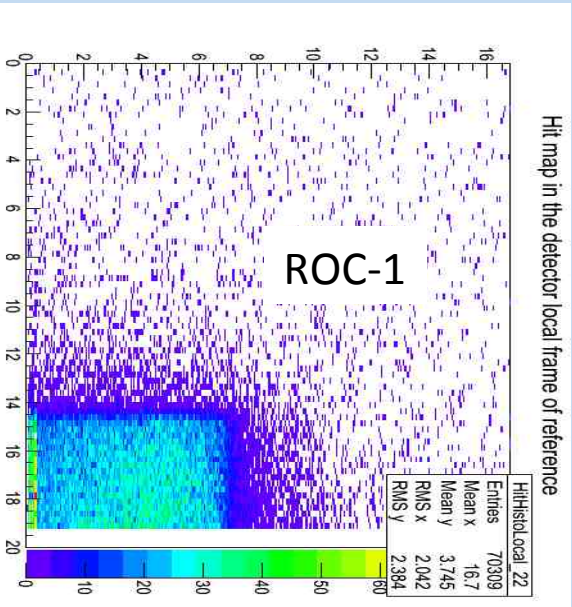
- Quads installed in March 2013 DESY Testbeam, read out using USBpix
- ROC3 was not working for Test beam due to broken wire bonds
- Data taken in the colour coded area's
- All ROC's tuned to 3200e threshold at 100V
- Single chip module MSS02 used as reference

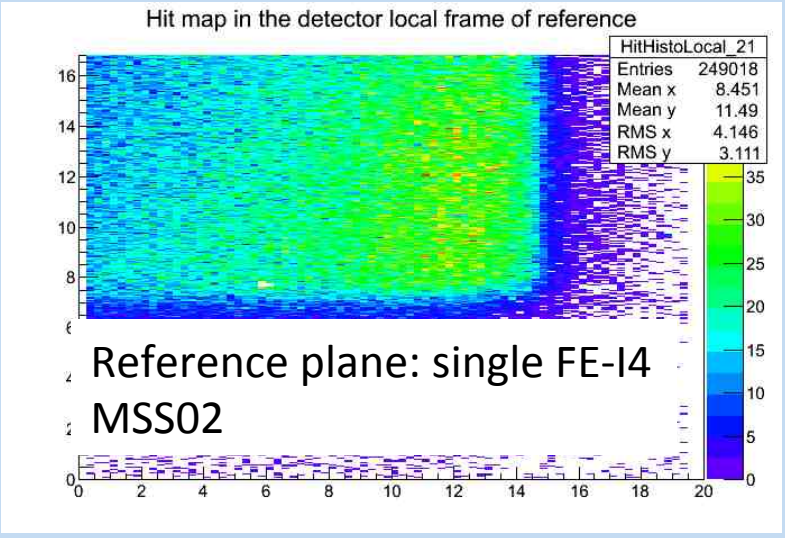


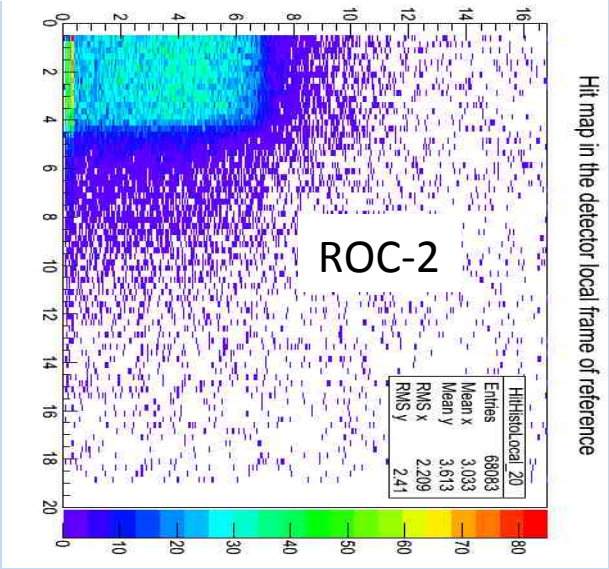


Testbeam analysis







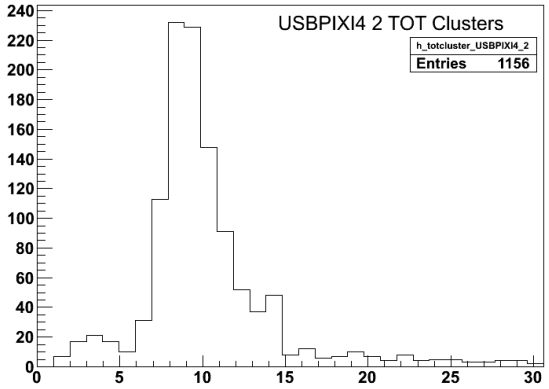


Reconstruction of local hit maps

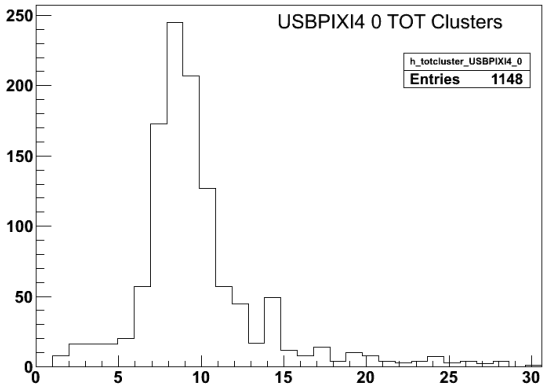
3 out of 4 chips all working fine
ROC3 had a few broken wire bonds during testbeam

Testbeam analysis

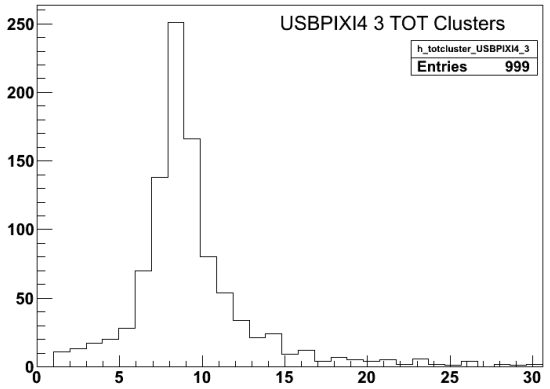
ROC1



ROC2



ROC4



- All active ROC's performing well
- All ROC's tuned to 10 T0T = 20 ke
- Reconstruction has started – software being developed for Quad module

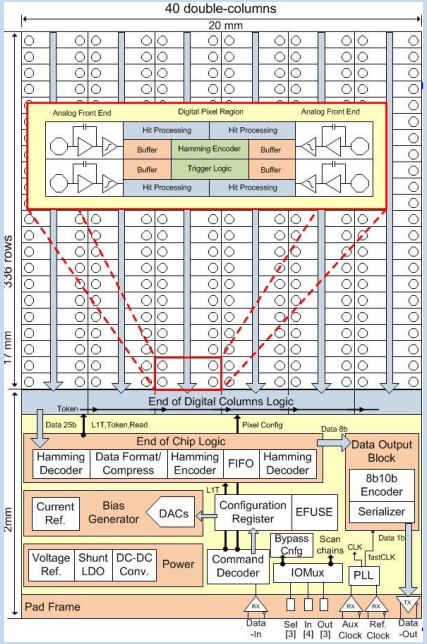
Summary and conclusions

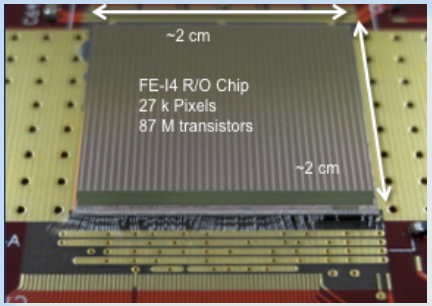
- Quad sensors for the ATLAS Phase-II Pixel upgrade have been manufactured
  - I-Vs on sensors show yield of ~97% for latest devices
- I-Vs show some reduction in current after assembly, due to bypassing sensor punchthrough biasing
- I-Vs (single chips) after irradiation show good characteristics
- Assemblies with parylene coating have been made and show good I-V characteristics
  - Visual inspection shows changes in parylene after irradiation
- Quad modules have been assembled and characterised
  - Single FE-I4 tuned to 1600e with noise comparable to single chip
  - Bump yield for thinned single and quad modules was in range 40-97% due to bowing of FE-I4
  - New bump bonding processes, both solder and In based, being investigated
  - Backside compensation to reduce effect of ROIC bowing during bump-bonding being investigated
  - Preliminary measurements of new process show that new set of single chip standard thickness assemblies have bump yields >99.9%
- Data taken with quad at PPS testbeam at DESY in March 2013
  - Hit maps show that the 3 out of 4 chips are operating
  - Data analysis ongoing
- Work on different geometries → next talk by Helen Hayward

BACKUP

FE-I4

- FE-I4
- Area 2.0x1.9cm2; active area: 3.36cm2; 26880 channels: 80columns@250umx336rows @50um pitch
- cf Medipix: 1.4x1.7cm2; 1.94cm2
- cf ALICE1LHCb: 1.4x1.6cm2; 1.74cm2





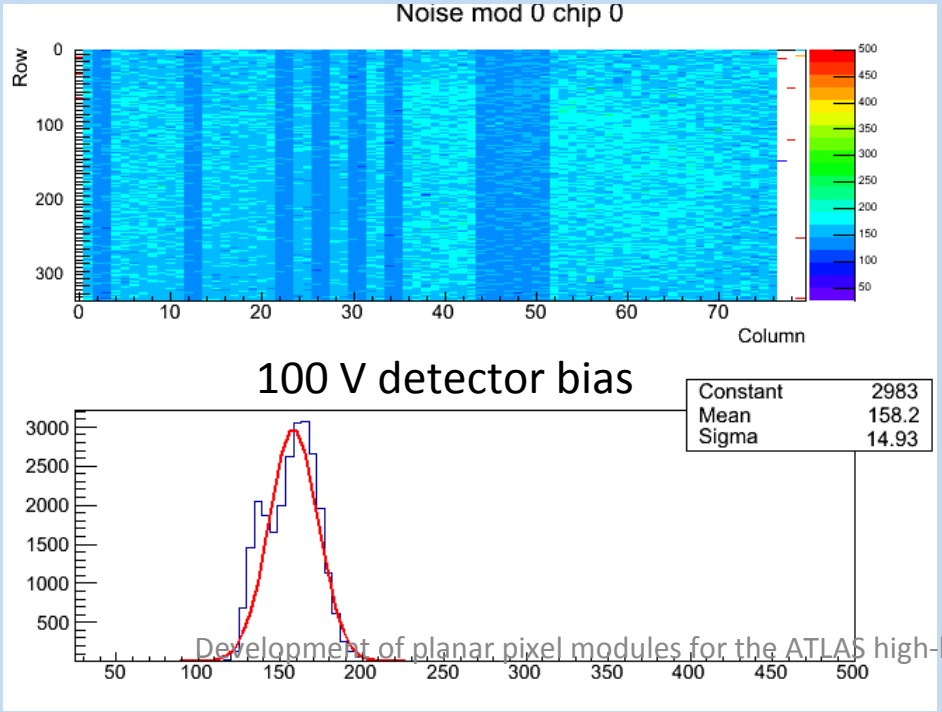
FE-I4 Pixel Chip (26880 channels)

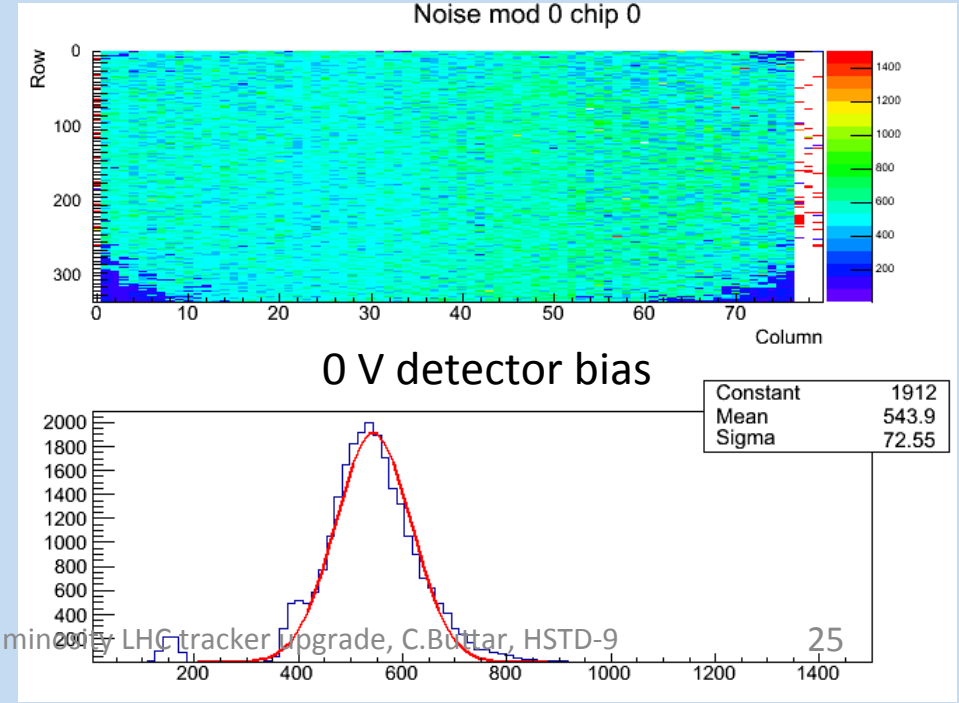
19 x 20 mm^2 130 nm CMOS
based on an array of 80 by 336 pixels
Pixel size: 50 x 250 μm^2

Un-bonded Channels
A: Pixel noise

Threshold scan for high and 0 V detector bias

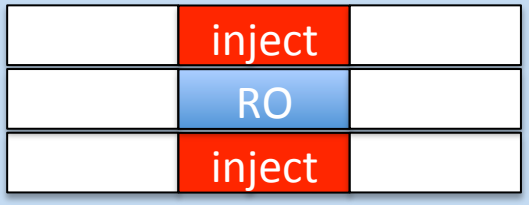
- At high detector bias noise over matrix approximately constant
  - 150e for this device
- Observe low noise pixels
  - No detector capacitance load
  - Ignore dead/masked pixels





Un-bonded channels
B: Pixel Cross-talk

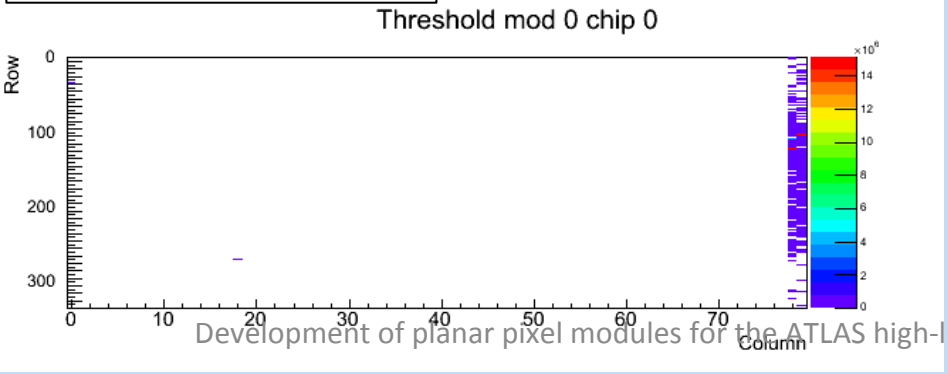
- Cross-talk measured by
  - Applying injection and readout mask



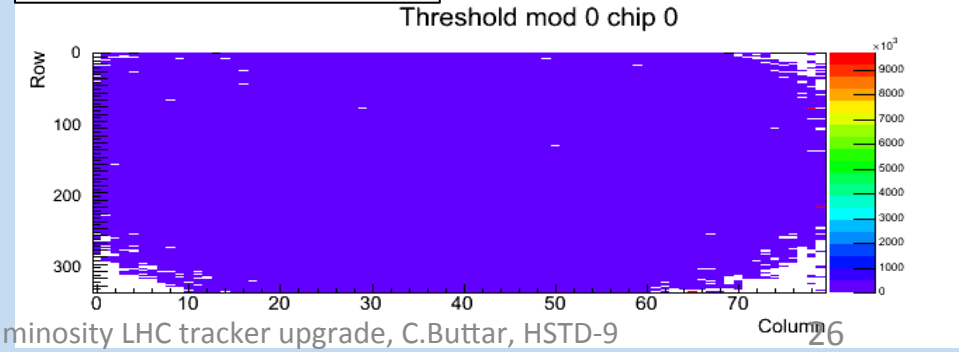
  - Inject large charge w.r.t. in-time threshold

- There is no cross-talk between un-bonded pixel channels
- For 0 V bias
  - Pixels coupled via detector capacitance
  - ➢ cross-talk high
  - Un-bonded channels those with no cross talk

S-curve mean 100V



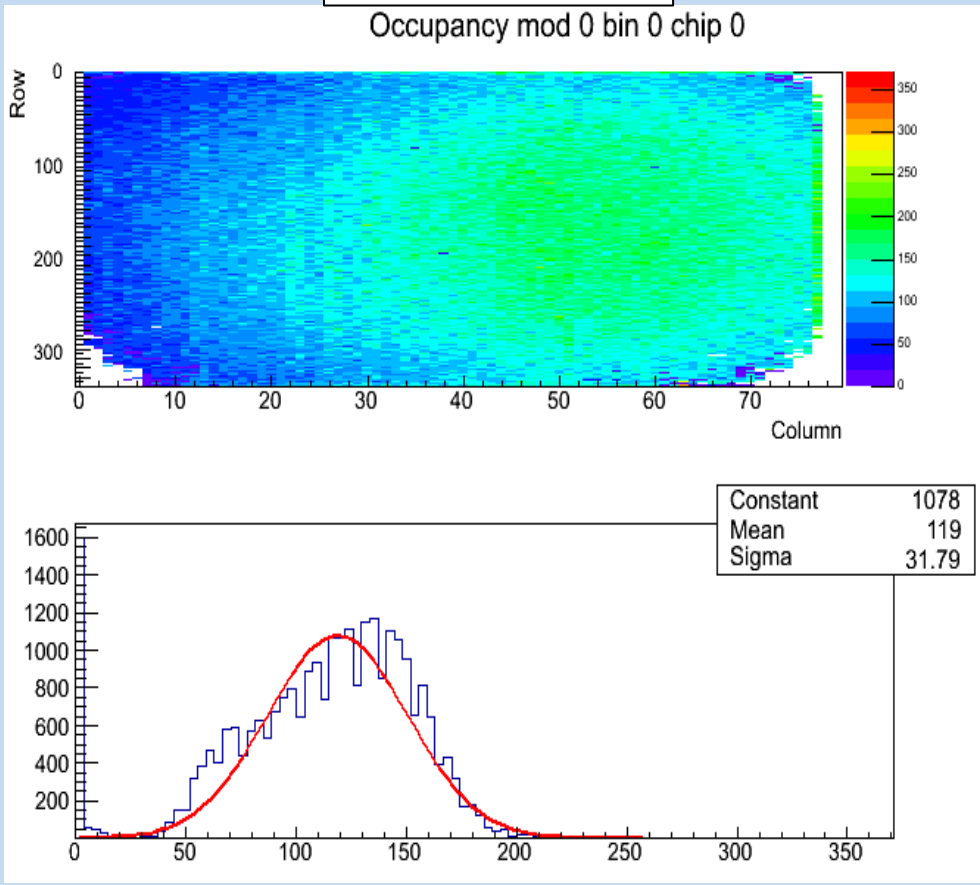
S-curve mean 0V



Un-bonded channels
C: Am-241 Gammas

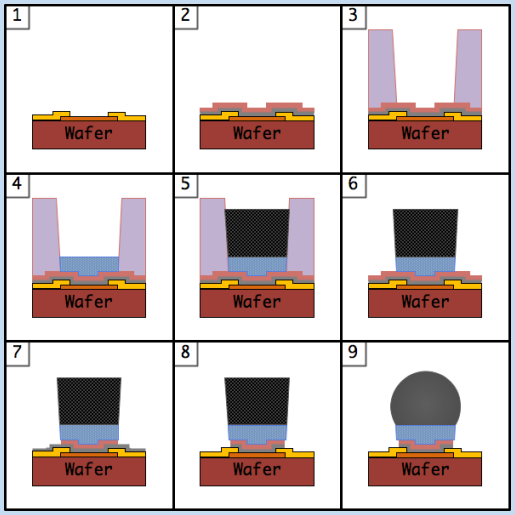
- Flood illuminate sensor with 60keV gammas from Am-241
- Use HitOr (hit in a pixel) output from FE-I4 for self trigger
  - Required to remove stuck/noise pixels
- Non-responding pixels are not bonded

3 million events

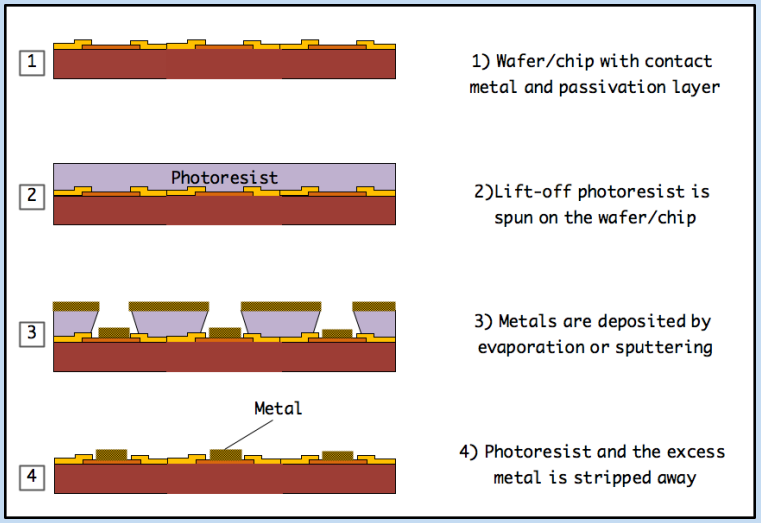


Electroplating vs. Lift-Off

- A key part of quad development programme is optimising cost of production
- Typically solder bumps are deposited on the ASIC wafers and solderable UBM pads/ bumps on the sensor wafers
- Electroplating is the most common way to deposit UBM/solder alloy
- Alternative way to deposit/pattern the UBM pads/solder on the sensors is to use PVD deposition in combination with lift-off process (Advacam UBM)
  - Sputtering or evaporation of metal films through resist mask and resist stripping
  - Lift-off is tricky but a cost effective way to deposit UBM pads on small sensor wafers



Electroplating process flow



Lift-off process flow