



Double-Sided Super-Module R&D for the ATLAS Tracker at HL-LHC – a Summary

9th Hiroshima Conference on Development and Application of Semiconductor Tracking Detectors
(HSTD9)

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Outline:

1. Why: Global Requirements and Motivation
2. Recap of Super-Module scope and set-up
3. Electrical performance of the Super-Module
4. Mechanical status of the Super-module
5. The next steps:
 - what needs more work (cable bus)
 - design evolution
6. Comments and Summary

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Global Requirements and Motivation

Global Requirements

- Compatible with performance specifications of ATLAS but in high pileup
- Compatible with other R&D projects involving the groups
 - ABCN 250 nm and future ABCN 130 nm + HCC development
 - Sensor n-in-p R&D developments
 -
- Build on merits of proven ATLAS tracker, identify and correct limitations

Guidelines

- True stereo space-point reconstruction using stereo strips
- Ability to provide z-overlap for modules (high alignment modes) if chosen
- Long term stability during operation and good placement accuracy
 - Stiff supporting structures
- Minimize thermo-mechanical stress at all levels (low and compatible CTE)
 - Modules,
 - Local support and structure
- Modularity of components: (evolution of what learned on SCT)
 - Ease of prototyping, component supply, Q&A + rework, large-scale fabrication and construction
- Low material budget
- Good electrical performance at operating voltages > 500V

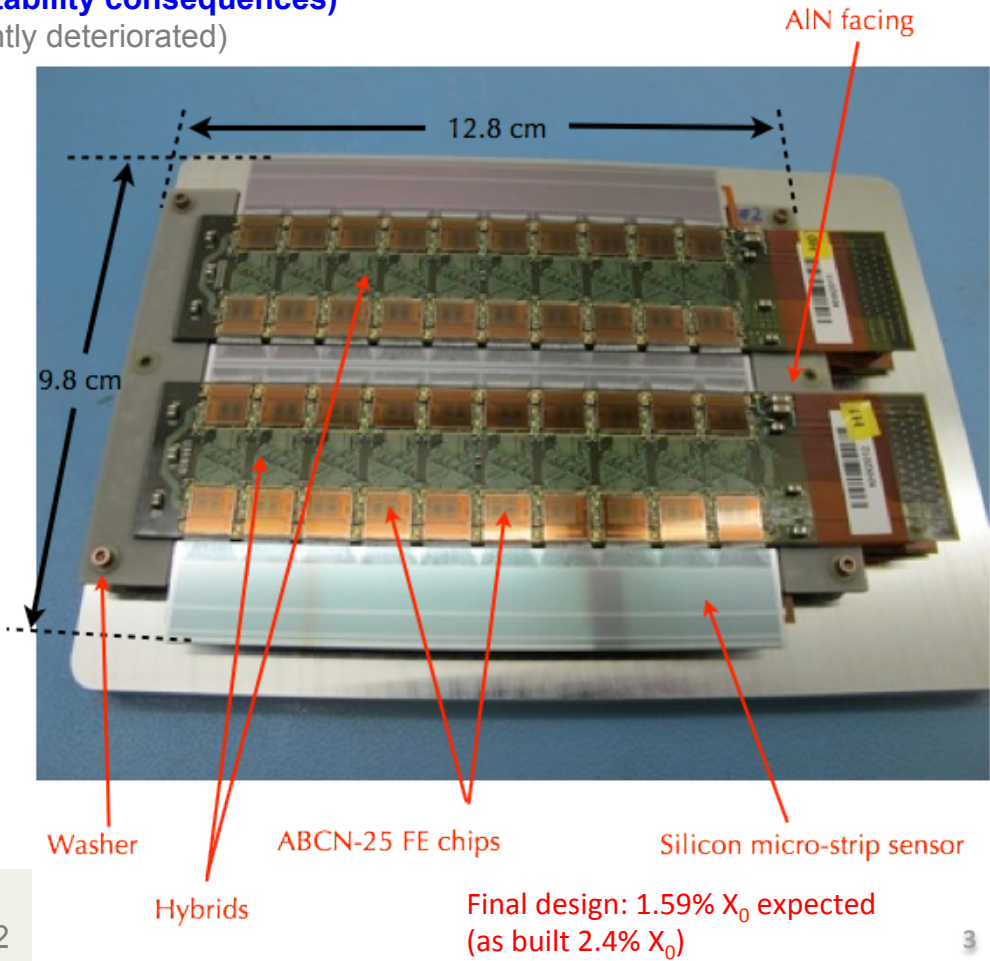
Project Status

- Backup option for ATLAS Tracker at HL-LHC* (STAVE option is ATLAS base-line)
- Scope of R&D project using the ABCN 250 nm FE chip successfully completed
 - Separate summary publications on electrical and mechanical aspects currently in preparation
- Future developments will use the ABCN 130 nm FE chip and the HCC readout controller

* ATLAS Phase II LOI
CERN-2012-022
LHCC-I-023

Module Design and Status – 1

- **Detectors are mounted back-to-back, true stereo reconstruction (400 μm sensor separation, will be 300 μm)**
 - Space point determined by the module assembly with the precision of the jigs
(build precision < ±1 μm rms)
 - Sensor (n-in-p Hamamatsu) 96 x 96 mm², (short) strips 24 x 0.075 mm², (long) strips 48 x 0.075 mm²
- **Precise module location on a local structure**
 - Centering bushes: origin + alignment - (mounting precision on support ±10 μm)
- **Bridge hybrid allows FE thermal path different from Si (stability consequences)**
(NB: Direct mounting is feasible, thermal performance slightly deteriorated)
- **Low CTE material and good thermal conductivity:**
 - Si, TPG, CC, AlN
 - Low deformation @ -35°C (FEA)
- **Hybrid pigtailed + connector for electrical connections (option)**
 - Modularity and flexibility
- **Module assembly known and simplified WRT existing SCT modules in terms of procedure and QA:**
 - > 950 SCT modules were fabricated by HPK and Seiko in Japan
 - 6 ABCN 250nm modules fabricated by industry (HAYASHI) + 3 in-house at KEK
 - Hybrids industrialized (Taiyo Industrial Co.)
 - > 650 SCT modules were fabricated by UniGe
 - 7 ABCN 250 nm modules fabricated in-house

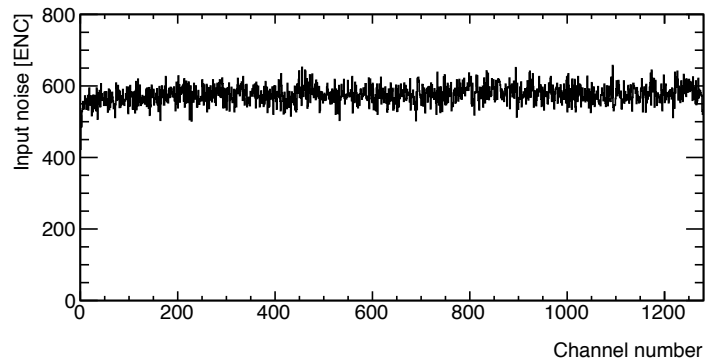


See
ATL-UPGRADE-PUB-2011-002

Module Design and Status – 2

Assembly Site	Module id	Sensor type	Hybrid version	Super-module	Comments
KEK	KMX-1000	FZ1 p-stop	v1		- long strip test module
KEK	KMX-1001	FZ1 p-stop	v1		
KEK	KMX-2002	FZ1 p-stop	v2		
KEK	KMX-2003	FZ1 p-stop	v2		- 5 dead ABCN-250 asics
KEK	KMX-2004	FZ1 p-stop	v2		- sensor crack during assembly
KEK	KMX-2005	FZ1 p-stop	v2	Yes	- industry
KEK	KMX-2006	FZ1 p-stop	v2	Yes	- industry
KEK	KMX-2007	FZ1 p-stop	v2	Yes	- industry
KEK	KMX-2008	FZ1 p-stop	v2	Yes	- industry
Geneva	GMX-1000	FZ1	v1		- "half module" used for irradiation studies - manual assembly of SMD's
Geneva	GMX-1001	FZ1	v1		- manual assembly of SMD's
Geneva	GMX-2002	FZ1 p-stop	v2	Yes	
Geneva	GMX-2004	FZ1 p-stop	v2	Yes	
Geneva	GMX-2006	FZ1 p-stop	v2	Yes	
Geneva	GMX-2007	FZ1 p-stop	v2		- electrical coupling between HV and V _{dd}
Geneva	GMX-2008	FZ1 p-stop	v2	Yes	

see also [ATL-UPGRADE-PUB-2011-002](#)

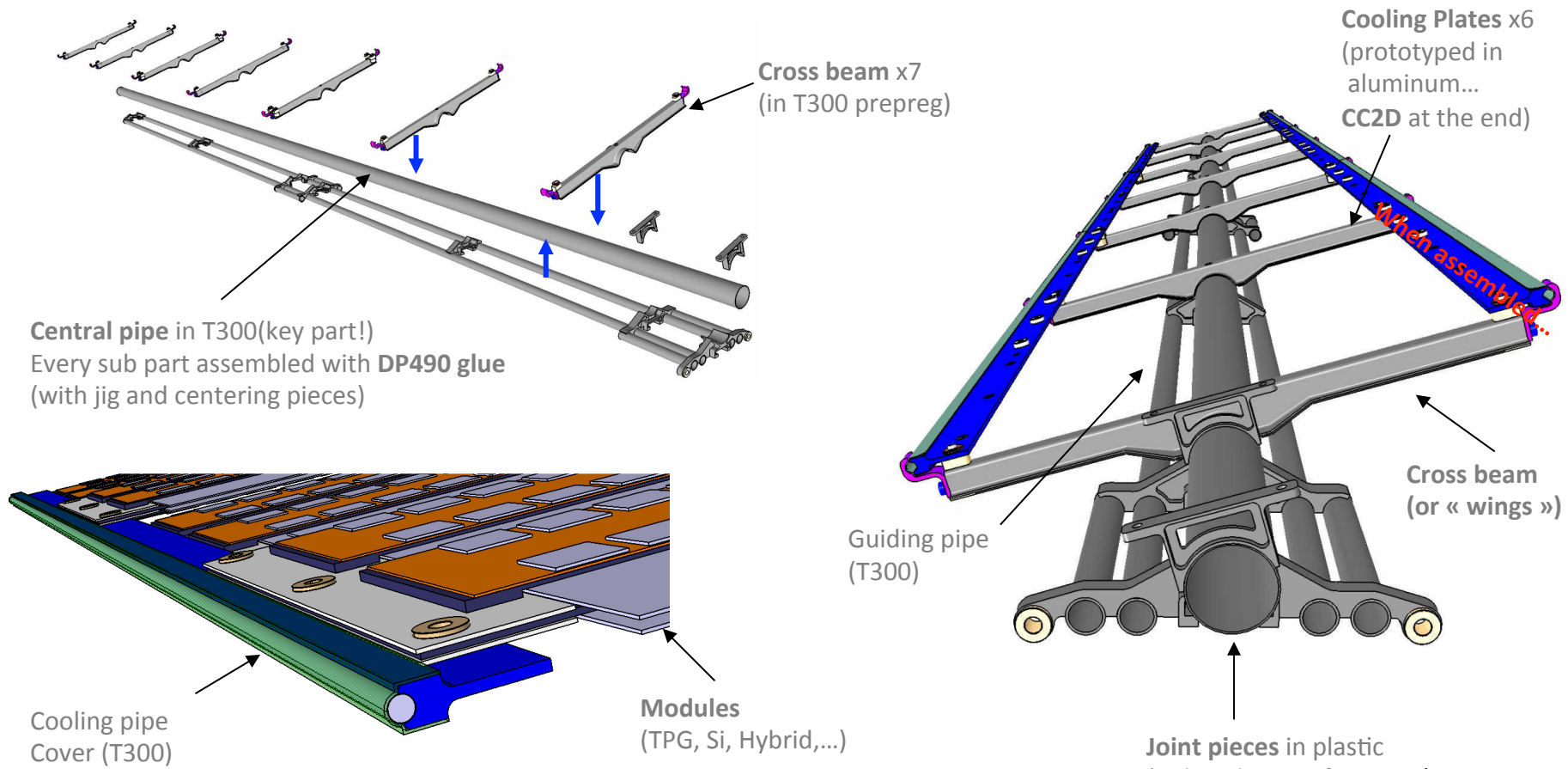


- Table shows modules constructed in Japan and CH + modules used in 8-module electrical super-module
- Module GMX-1000 used for radiation studies at level expected for LHC (previously reported)
 - ✓ Noise level after irradiation very satisfactory
 - ✓ Similar excellent results from STAVE R&D for single module
 - ✗ But ... sensor leakage current high (low temperature operation)
 - ✗ no test-beam results

- ✓ Typical individual module input noise (ENC) using direct powering (10 ASICS of a single hybrid shown):
 - $\langle \text{ENC} \rangle \sim 575 - 600$
 - $\sigma_{\text{ENC}} \sim 25$
- ✗ No modules used so far in test-beam

Super-Module Mechanical Design

CAD view of the SM (modules removed for clarity)

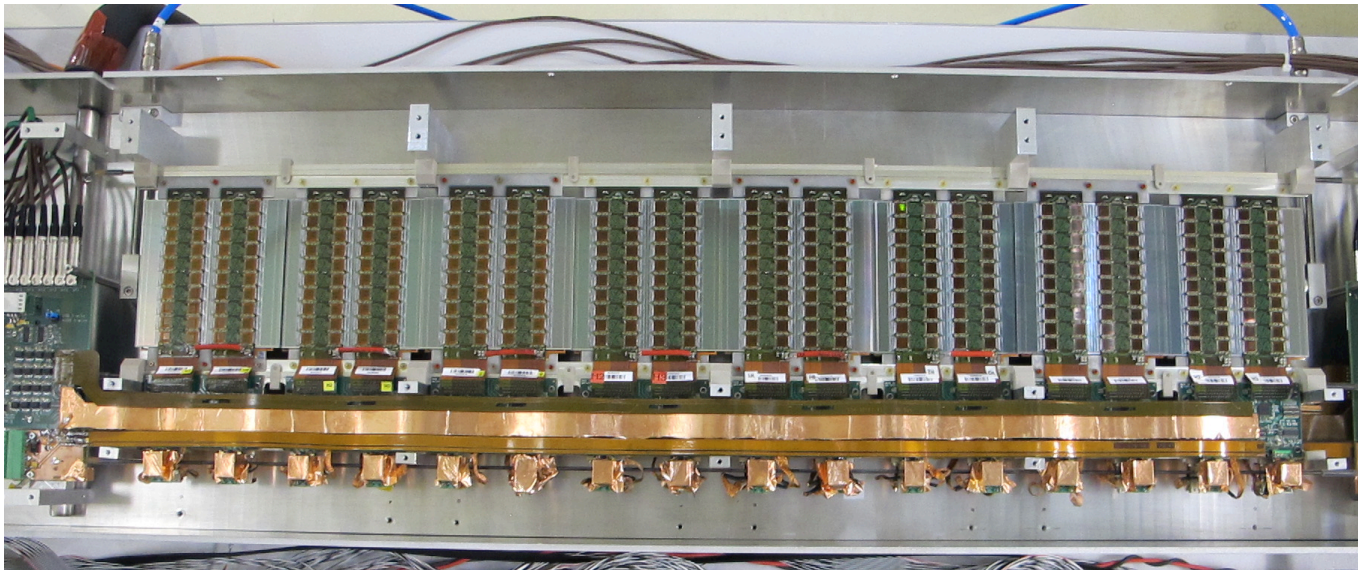
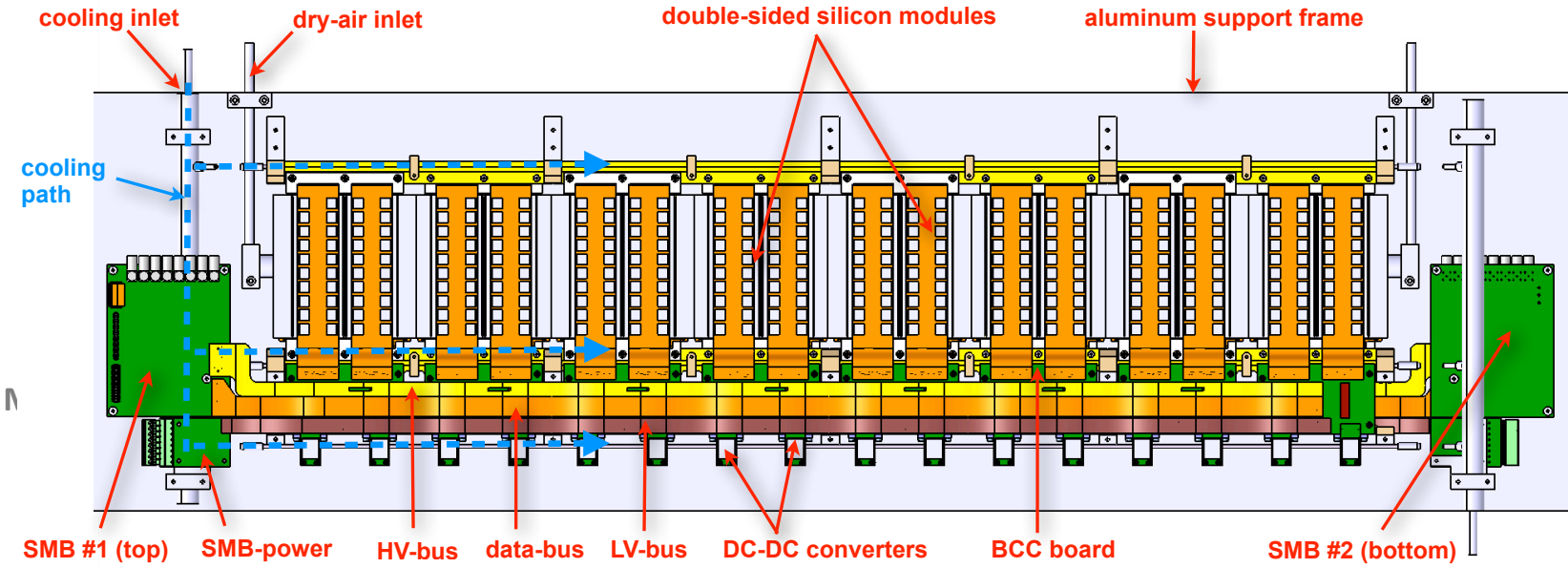


Mechanical studies discussed later (baseline ATLAS layout foresees 13 modules, studies for this R&D assumed 12 modules))

In parallel an 8-module electrical prototype has been developed, replicating all electrical and cooling aspects and allowing parallel prototype development

Super-module Electrical Prototype – 8 modules

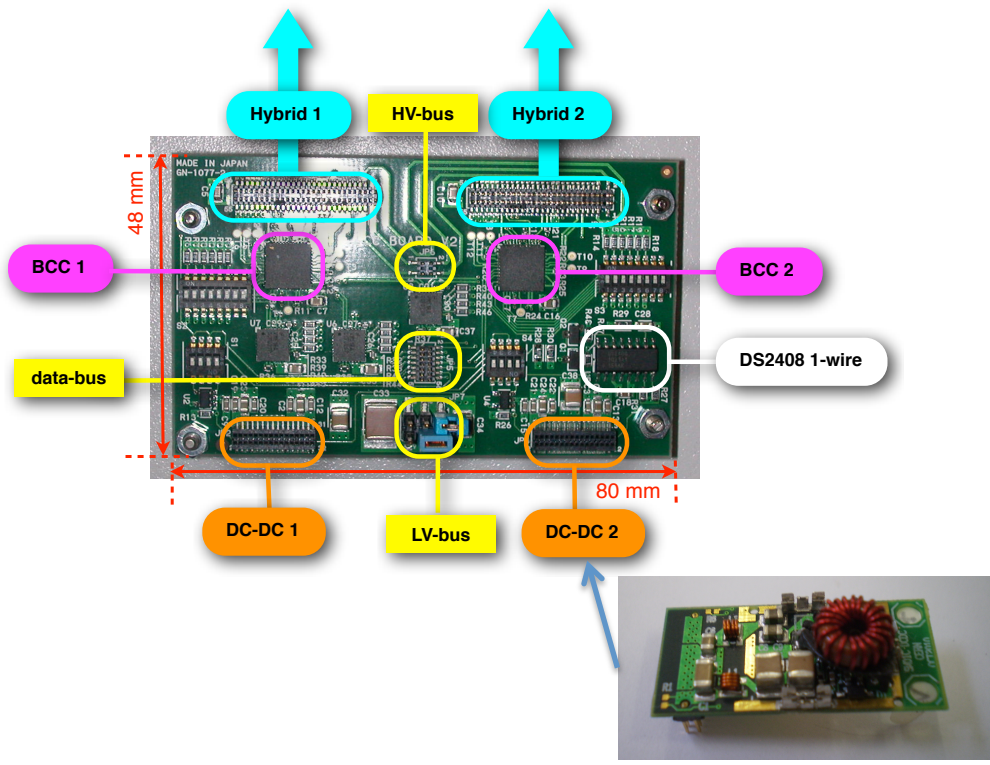
8 modules = 16 sensors = 32 hybrids = 640 ABCN250 FE chips = 81920 channels



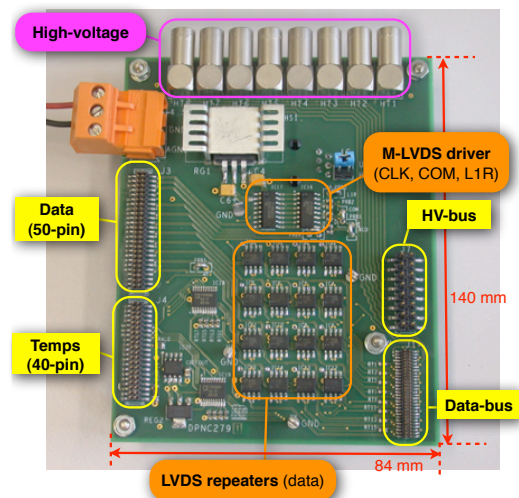
4 x larger than any other DC-DC implementation for HL-LHC R&D

Super-module Electrical Prototype – off-module interfaces

- BCC chip (common with stave R&D):
 - clock multiplier for 80 MHz readout
 - LVDS buffering, command decoder, configuration register
 - data multiplexing
- BCC Board (KEK) – 1 each side of module
 - 2 BCC chips (packaged)
 - interface for 2 hybrids+ 2 DC-DC boards
 - service bus connection
 - prototype usage only



- SMB board (1 per Super-Module side)
 - Interface to DAQ (HSIO/USB), (similar for Seabas DAQ developed by KEK)
 - Provides DC-DC control, monitoring
 - Interface to HV, LV and data buses



Super-module Electrical Prototype – cable bus

Least developed aspect of SM program

- electrical
- mechanical

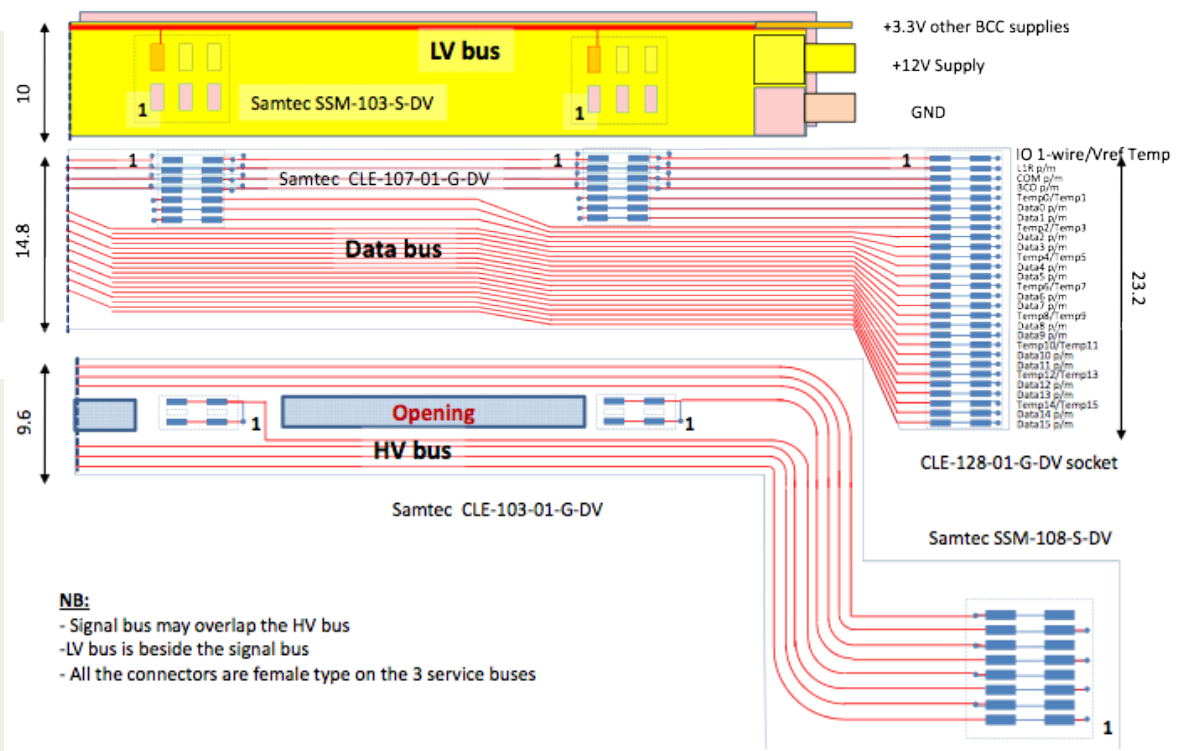
Intended as a first version prototype

- initial conservative design

2 identical 765 mm long sets of LV, HV and data buses, 1 on each side of SM

- design and constructed at CERN
- HV bus drives HV for 8 sensors
- LV bus drives 10-12 V lines for DC-DC converters + 3.3 V BCC supply
- Data bus has 16 LVDS pairs (2 per module)
- Currently use Samtec connectors to BCC and SMC boards (excepting LV)

Expected evolution of cable bus considered later in this talk



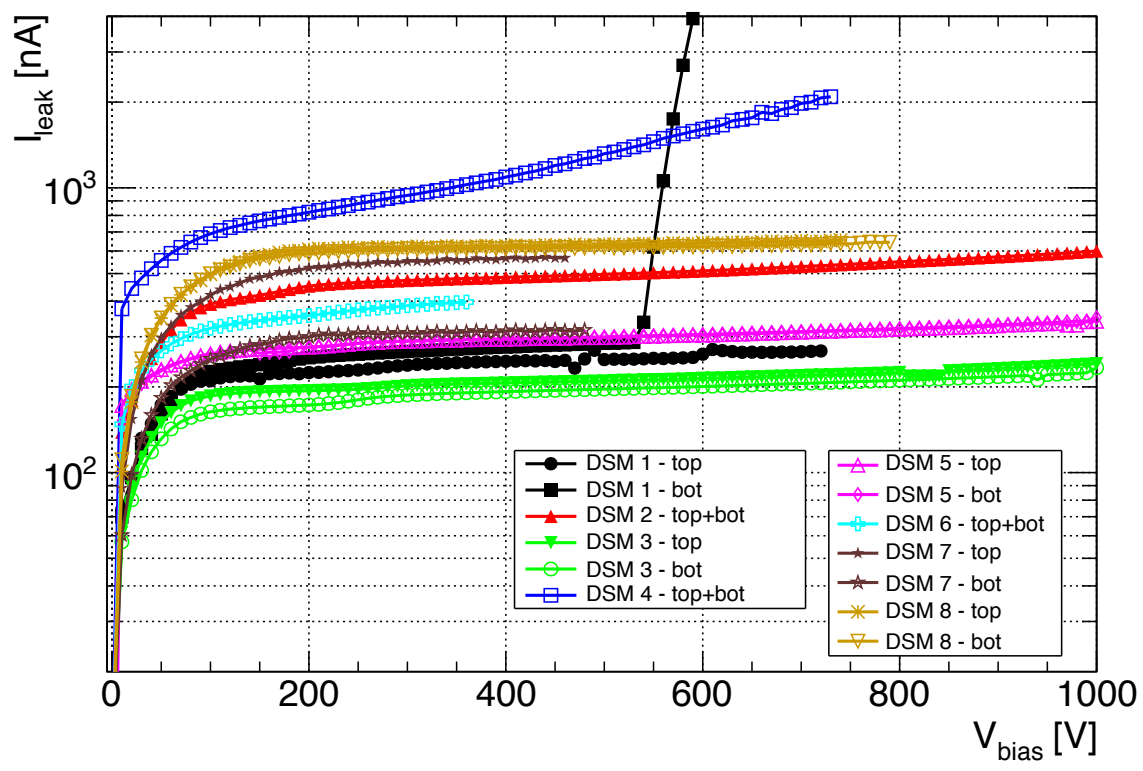
NB:
 - Signal bus may overlap the HV bus
 - LV bus is beside the signal bus
 - All the connectors are female type on the 3 service buses

	HV	Data	LV
Total number of layers	2	2	2
Total number of traces:			
• Layer 1	8	28	2
• Layer 2	8	28	1
Trace width	0.2	0.1 - 0.2 [†]	2.2 - 9.5*
Cu-layer thickness	0.035	0.035	0.2
Minimum / Maximum bus width	9.6 / 22.3	16.0 / 26.0	10.0 / 10.0

Parameters of the service buses. Thicknesses and widths are given in mm.

I-V Performance of the 8 Modules

- HV provided individually to top and bottom sides of each module via HV bus
 - iSEG EHS-8210n-F (2 cards with 8 6U channels): 1 kV & 8 mA

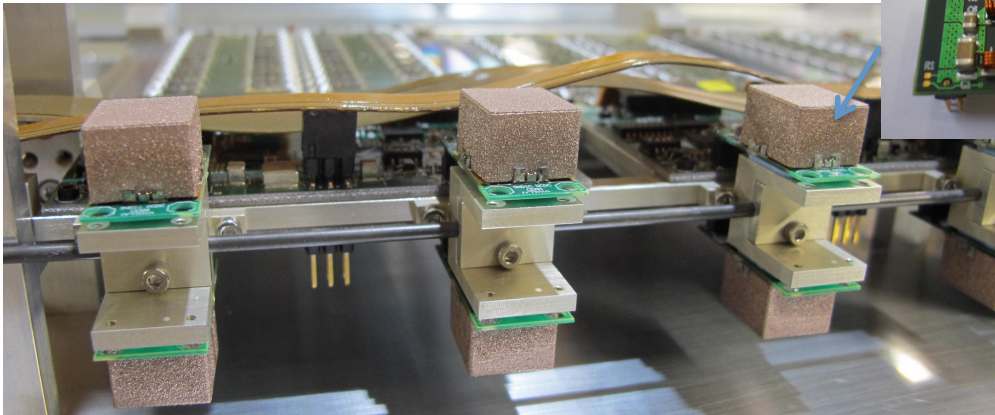


- Good HV behaviour for all modules
 - Breakdown of DSM1 top side at 550V
 - DSM2, DSM4 and DSM6 have HV coupling between top and bottom sides (pin-holes in TPG coating?)
- Future designs will use single HV channel for several modules to reduce service material

Low Voltage Performance of the 8 Modules

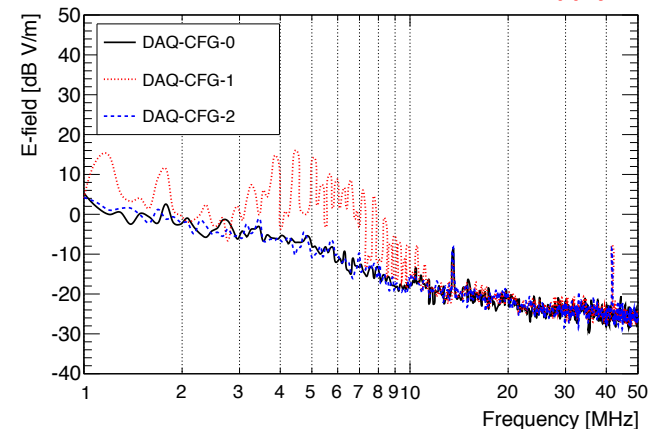
- Low voltage supplied using a TDK supply
 - Constant voltage source maximum 20 V and 76 A
 - Supplied with common 10-12 V line to DC-DC converters
- Each hybrid supplied via DC-DC converter (developed at CERN)*
 - SM01C prototype using air-core toroidal inductor
 - Shielded to reduce EM emissions (10 μm Cu cover)
 - Some variability in DC-DC shielding and peaks at harmonics of 2 MHz carrier

* G. Blanchot et al.,
TWEPP 2009 Proceedings,
pp276-280.



- Additional noise sources identified from the LV supply (~5 MHz) HSI0 board (1-10 MHz) and the DAQ (42 MHz)
 - Effect on noise measurements for modules difficult to quantify
 - Consequence on noise of DC-DC not fully understood

Electric field on one hybrid in different DAQ-HSIO configurations
CFG-0: **HSIO DAQ off**
CFG-1: **HSIO DAQ on**
CFG-2: **HSIO DAQ on, external 12 V supply**

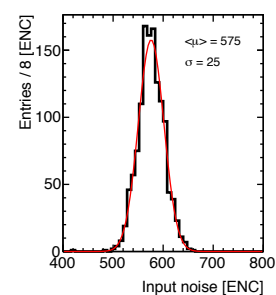
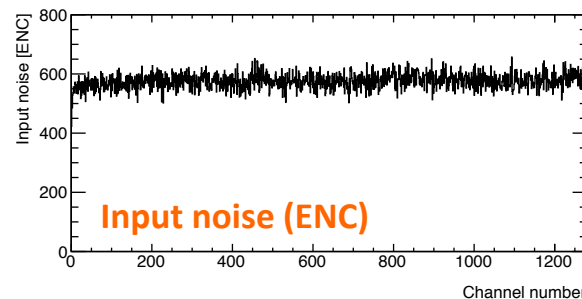
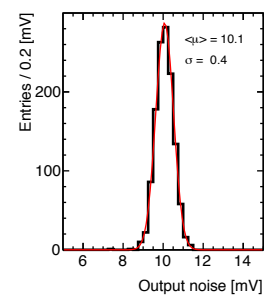
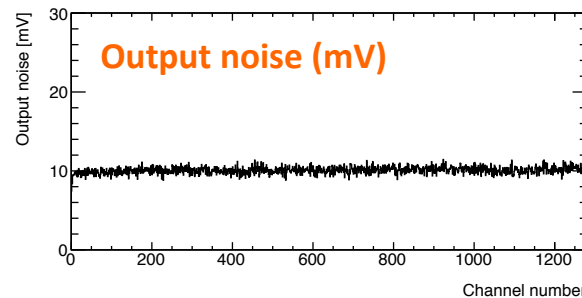
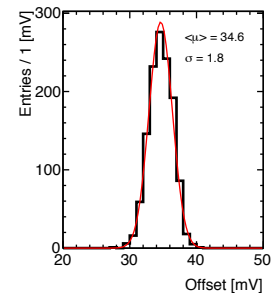
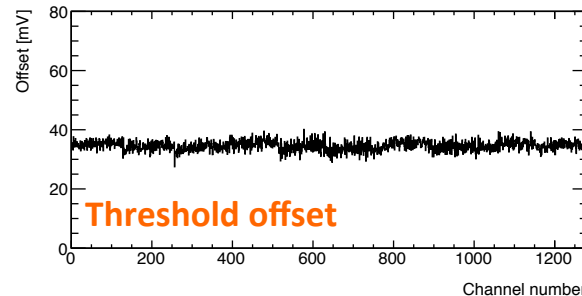
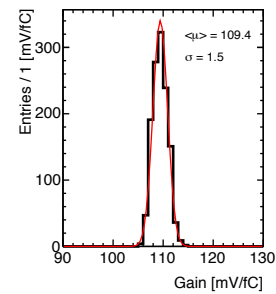
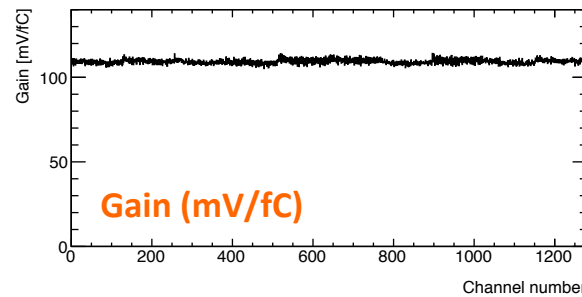


Calibration of Modules – 1

- Initial channel-by-channel calibration of each ABCN 250 ASIC
 - Calibration delay
 - Discriminator threshold corrections
- Gain and noise (ENC) evaluation using threshold scans
 - 3-point gain test uses 3 input charges

3-pt gain for 1280 channels of a single hybrid column (10 ABCN ASICS)

Noise (~ 600 ENC) and gain (~ 110 mV/fC) are as expected



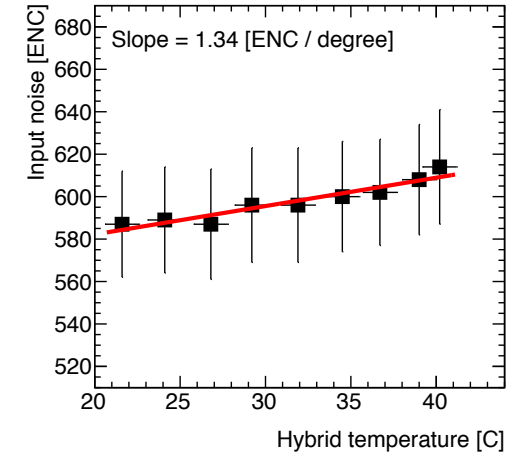
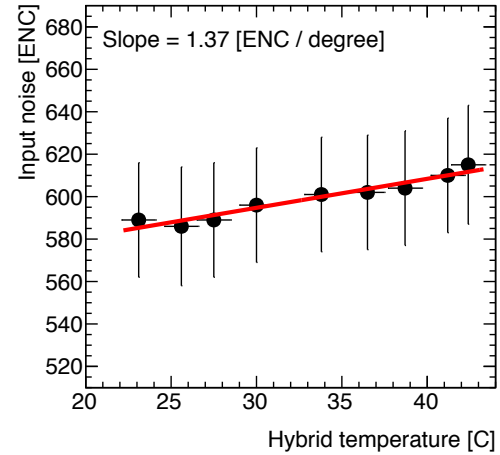
Calibration of Modules – 2

Dependence of ENC on hybrid temperature (2 hybrids)

- No corrections made
- $\Delta_{ENC} \sim 1.37 \text{ }^\circ\text{C}^{-1}$

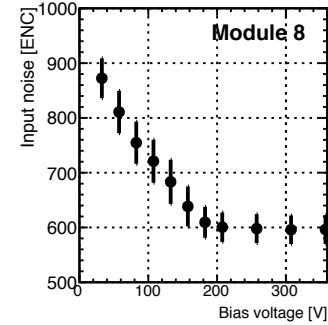
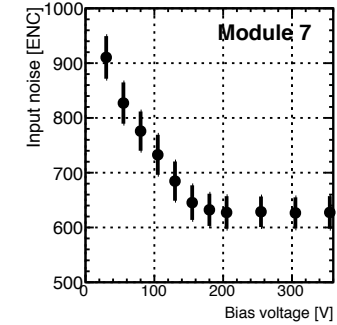
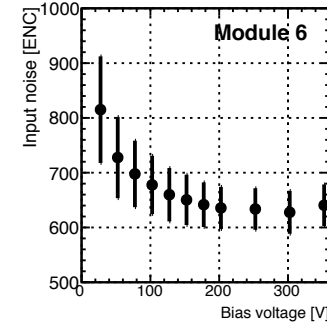
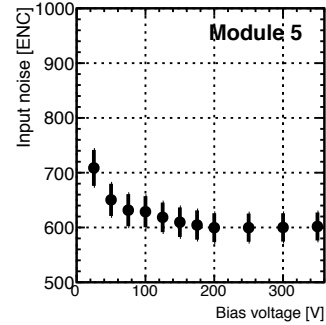
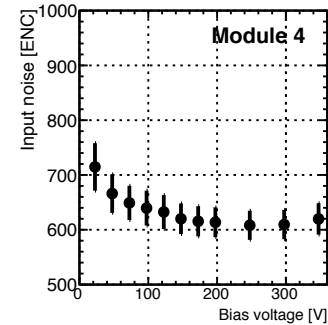
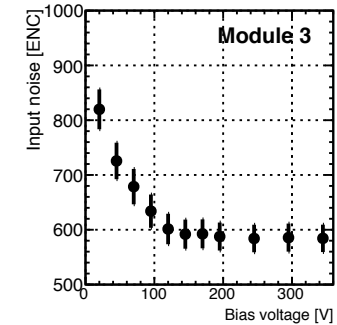
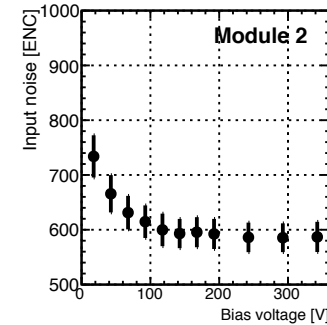
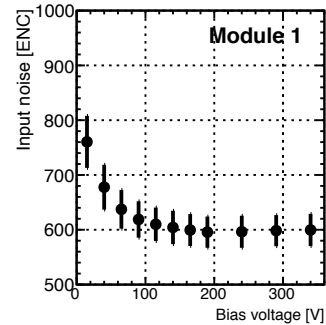
Noise measurements made at:

- Coolant: $\sim 5 \text{ }^\circ\text{C}$
- Hybrid: $\sim 32 \text{ }^\circ\text{C}$
- Sensor: $\sim 20 \text{ }^\circ\text{C}$



ENC vs. V_{bias}

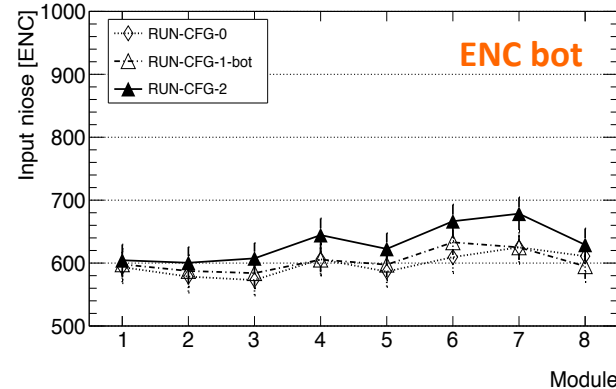
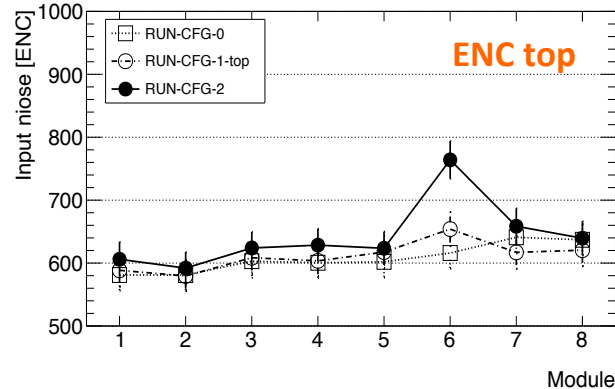
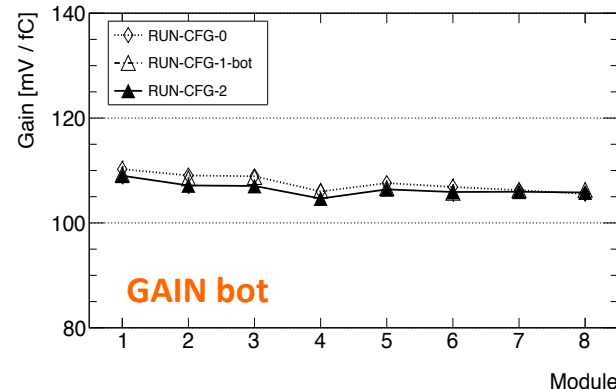
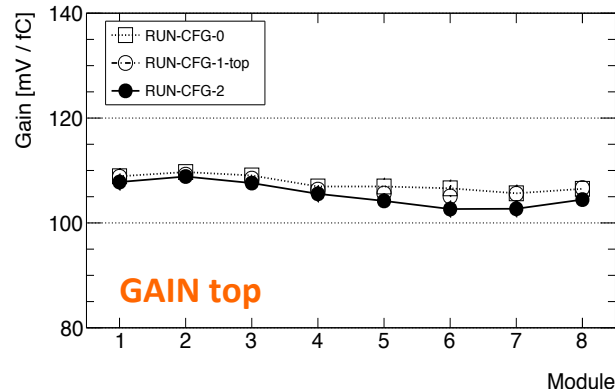
- Top side of each module shown
- Saturation knee consistent with V_D (ENC primarily from sensor)



Gain and Noise Measurements

Run configuration	Description	# DC-DCs enabled
RUN-CFG-0	- A single side of each module tested individually	2
RUN-CFG-1-top	- 8 module-sides (SM top-side) tested simultaneously - DC-DCs on opposite sides disabled	16
RUN-CFG-1-bot	- 8 module-sides (SM bottom-side) tested simultaneously - DC-DCs on opposite sides disabled	16
RUN-CFG-2	- 8 module-sides (SM top and bottom-sides) tested simultaneously - DC-DCs on opposite sides enabled	32

- When operated in CFG-2 mode, noise increases in range 10 – 60 ENC
- No significant DC-DC effect on same side (CFG-1)
- Deteriorated performance of module 6 (hybrids 3 and 4) is not understood
- Also deterioration of common mode noise for module 7



Results very satisfactory but further work on coupling of DC-DC converters needed between top and bot

Double Trigger Measurements

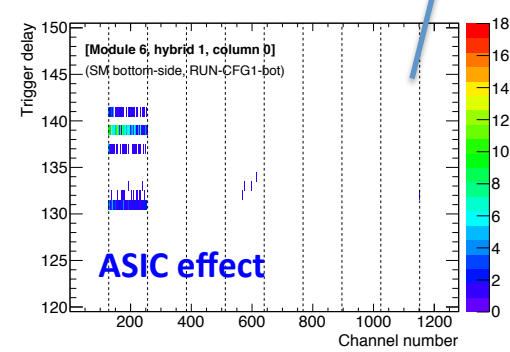
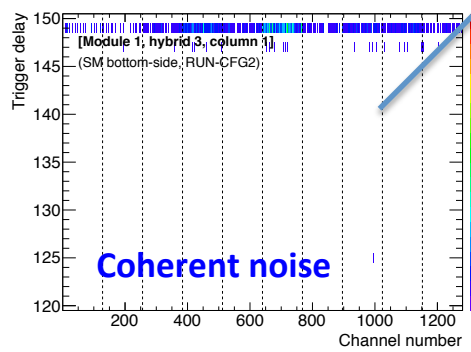
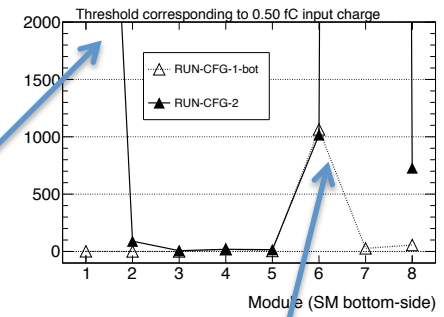
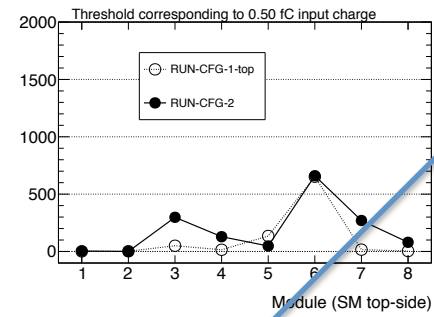
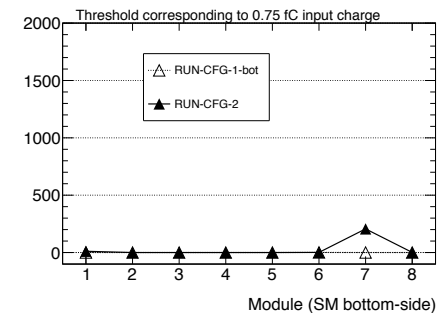
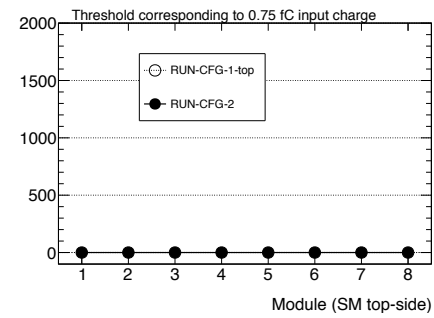
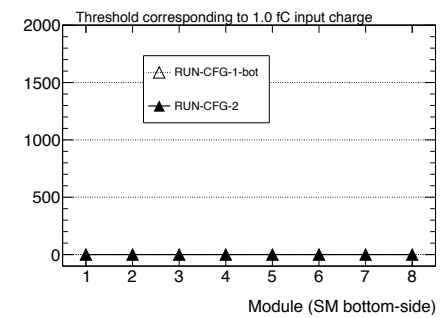
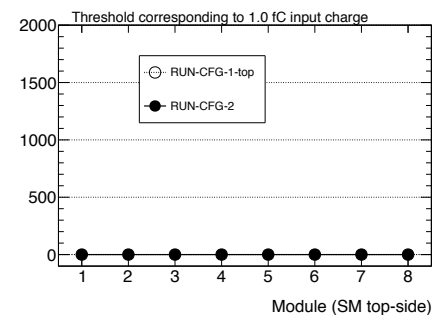
In collider operation, triggers are random and closely spaced triggers can occur

DTN measurements send 2 triggers separated by specified # of clock periods

- 2nd trigger read out
- If spacing close to pipeline length, the 2nd event records module occupancy at start of readout cycle of 1st event
- Measurements made as a function of input charge and for trigger separations of 120 - 150 clock periods

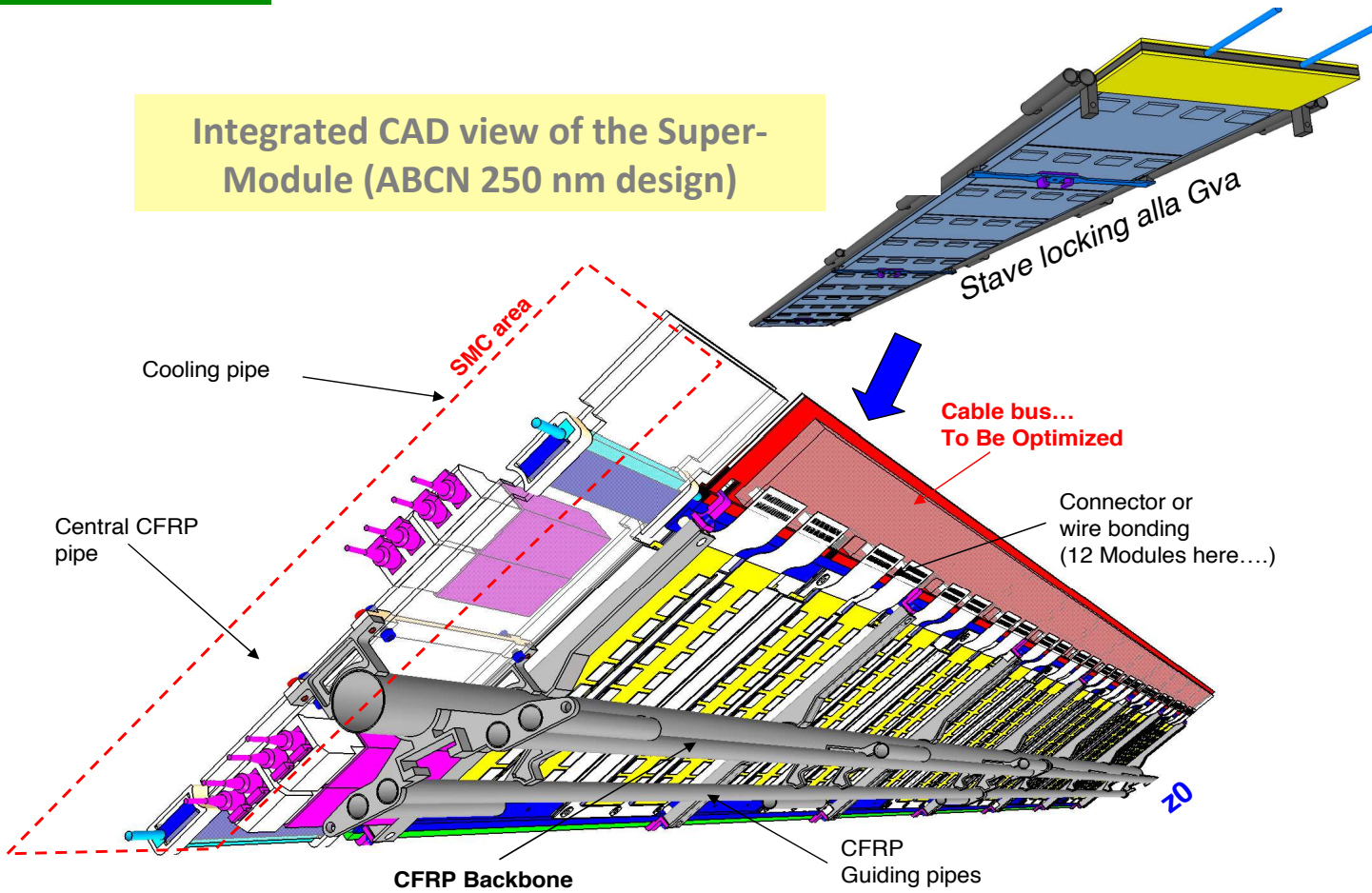
For 0.5 fC input, significant occupancy for a FEW hybrids (ASICs) in CFG-2 mode

- Further work required in future design to mitigate this



Super-module Mechanical Design Features

Integrated CAD view of the Super-Module (ABCN 250 nm design)



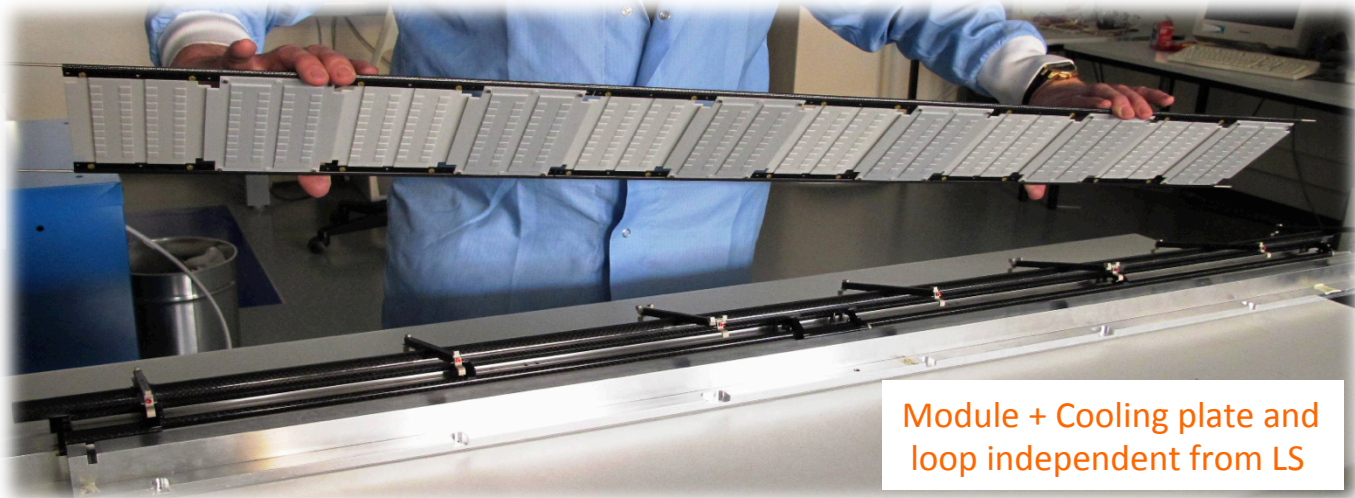
Low thermo-mechanical stress: Avoid all CTE mis-match. Service bus separated, cooling pipe uses sliding joints.
 Precision of module on local support at room temperature $\sim \pm 10 \mu\text{m}$ – surveyed
 Precision of local support on structure $\sim \pm 10\text{-}20 \mu\text{m}$
Module position at -35°C coolant determined by CTE and ΔT of local support

Mechanical prototype previously described (photos next page)

A few comments on this

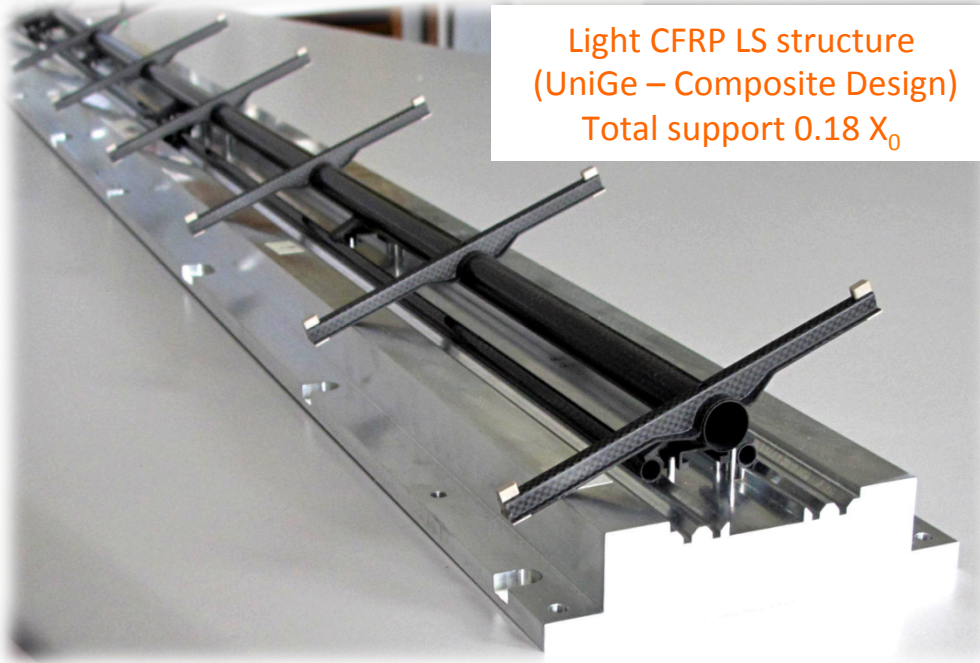
Super-module Mechanical Prototype

Concept validated with stress-free end-insertion interfacing dummy barrel locking system



Module + Cooling plate and loop independent from LS

Prototype previously described, no new results (publication in preparation)



Light CFRP LS structure (UniGe - Composite Design)
Total support $0.18 X_0$

Status and Outstanding Issues

Status: Feasibility and practicability of Super-Module demonstrated
(except possibly mechanical and electrical aspects of cable bus)

- Mechanical demonstration made
- Very successful multi-module electrical performance, although detailed studies of grounding and shielding remain important
- DC-DC architecture validated but EM interference needs optimization, as well as material (serial powering remains a valid option)
- Question of HV powering not yet addressed

Evolution: Evolution of sensor and module design with ABCN 130 nm and HCC submission
Evolution and implementation of read-out architecture and cable bus
Optimization of the mechanical support structure
Major test beam campaign with new design important

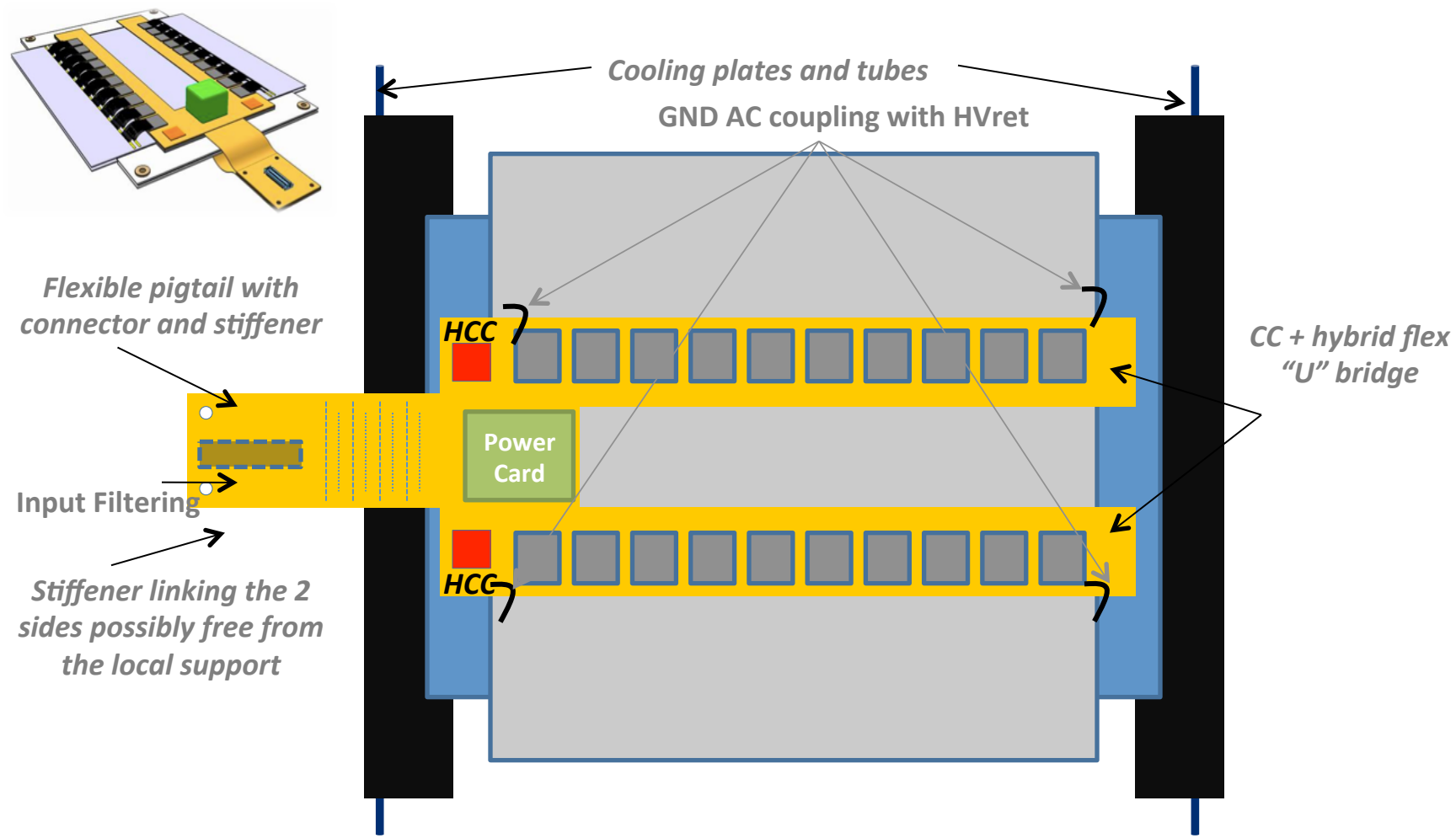


A few slides

Issues: Adapt to evolutions of the ATLAS tracker layout

- : optimization of the service bus
- : LV services (DC-DC or SP powering)
- : HV services (4 modules per HV line or HV multiplexer)
- : Tradeoff between performance (material, noise pickup) and robustness

Module Design Evolution



Comments:

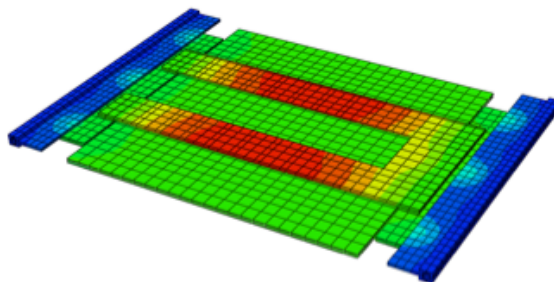
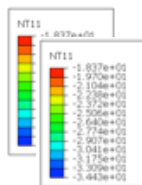
- Symmetry between the two rows is important. Also 1 hybrid type
- Power card (DC-DC or SP) is quite challenging and needs study – profit from cooling path
- Pigtail flexibility is essential to pass over the cooling plate
- EMI vs ground and shielding investigation is essential when considering DC-DC
- 1.59% X_0 with 12 mm width CC hybrid bridge, 1.49% X_0 if hybrid glued to sensor

FEA of Module Design

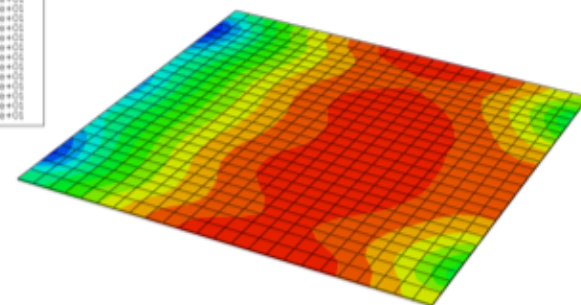
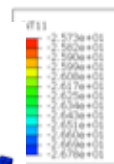
Thermal

ABCN250: 0.3W per chip(80)
 ABCN130: 0.15W per chip(40)
 + 0.8W per DC-DC(2)
 + 0.15W per HCC(2)

CO2 T (coolant) = -35 °C
 T(dry air) = 0 °C
 2mm ID Ti cooling pipe

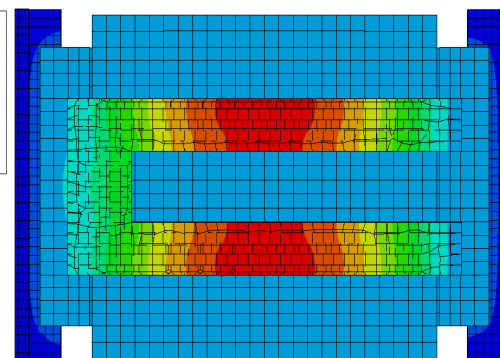
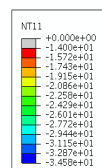


Contact at 3 points, T(hybrid) = -18 °C



T (sensor) in range [-26.7, -25.3]
 (for no hybrid bridge $\Delta T \sim +4$ °C)

More optimistic - full coverage of module and cooling plate with thermal grease (1W/mK, 50 μ m thick)



T (sensor) in range [-29.4, -31.1]

Mechanical deformation

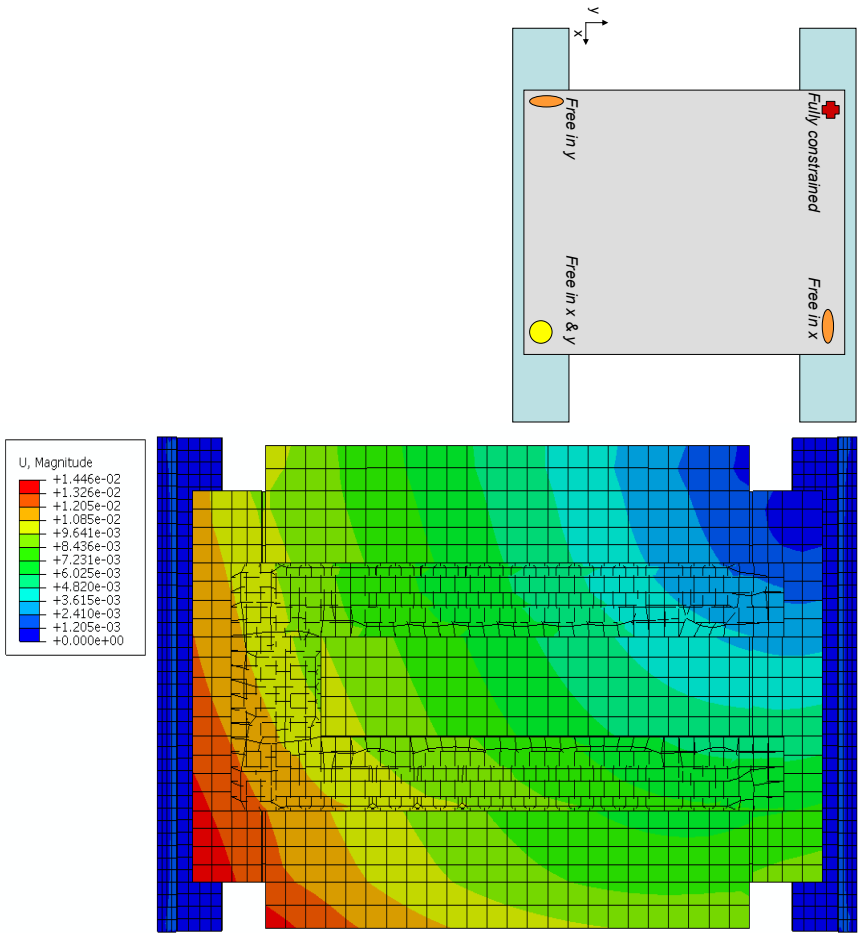
ABCN130: 0.15W per chip + 0.8W per DC-DC
 + 0.15W per HCC
 T (dry air) = 0 °C
 T (coolant) changed from T = +20 °C to T = -35 °C

Assembly: sensor-to-sensor ± 1 µm
 module fixation < ± 10 µm

Stress in TPG base-board: < 16 Mpa for ΔT = 40 °C
 (TPG tensile strength is 40 MPa)

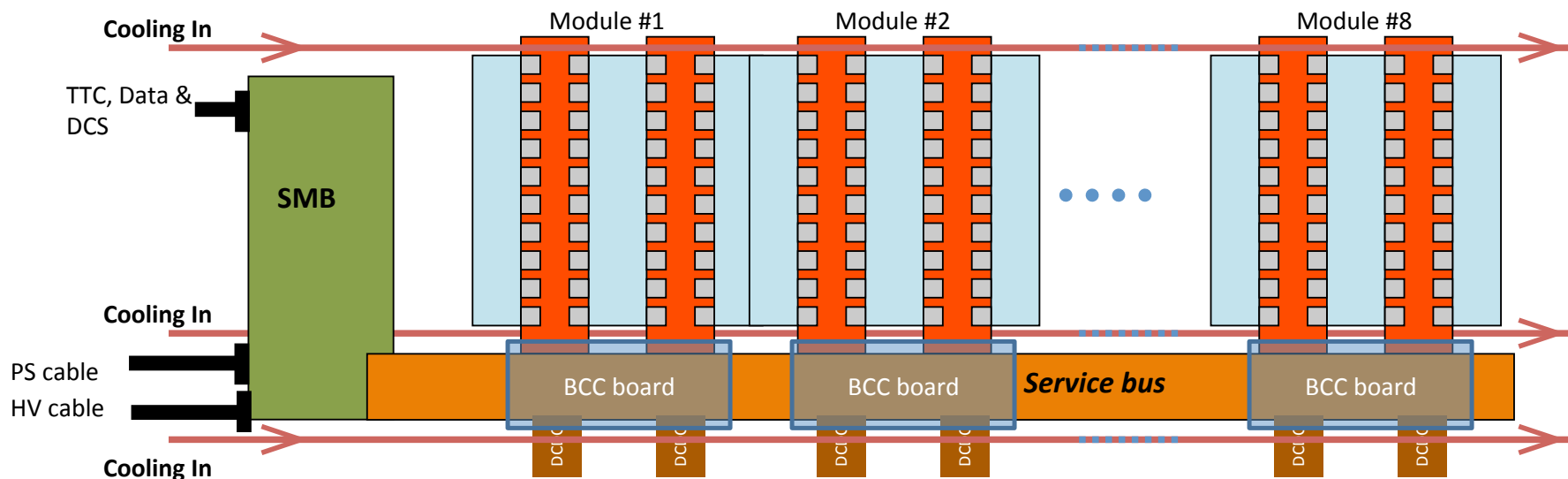
Max. in-plane module deformation: < 14.5 µm
 (< 1.5 µm deformation for ΔT = 5 °C,
 Important for long-term stability)

Max. out-of-plane module deformation: < 1.5 µm
 (TPG baseboard)

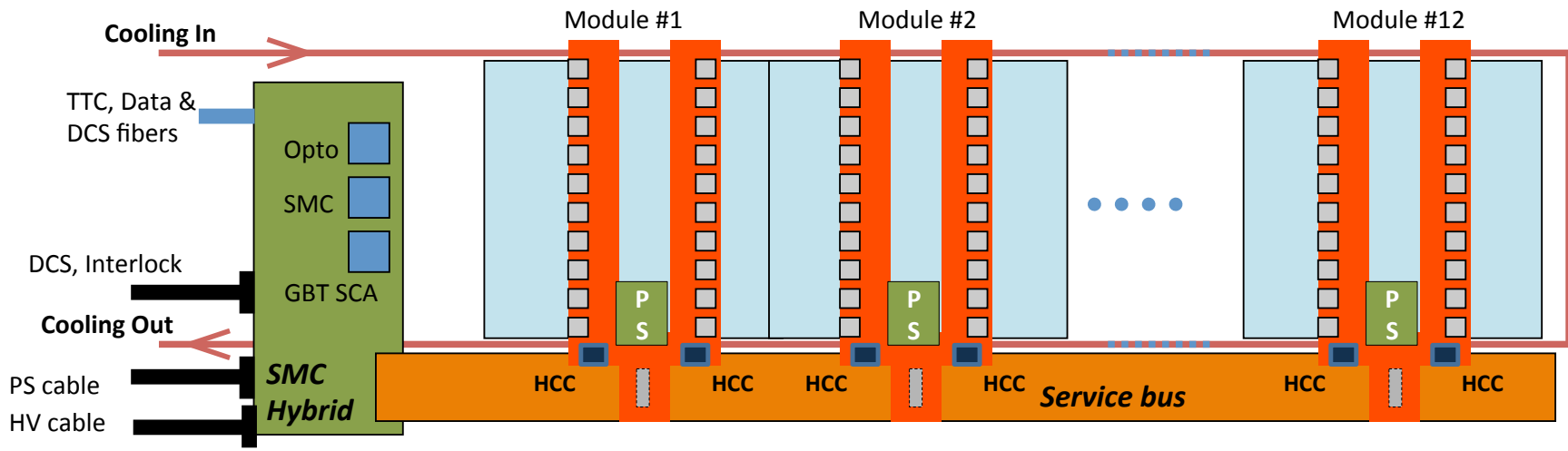


CTE (TPG)	(1.2, 1.2, 25)	ppm/°K
CTE (Si)	3	ppm/°K
CTE (AlN)	4.5	ppm/°K
CTE (kapton)	18	ppm/°K
CTE (glue)	25	ppm/°K

Super-Module Design Evolution

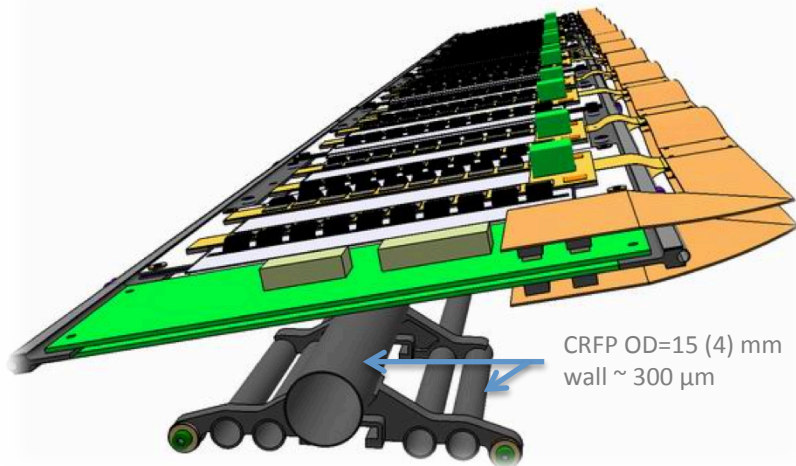
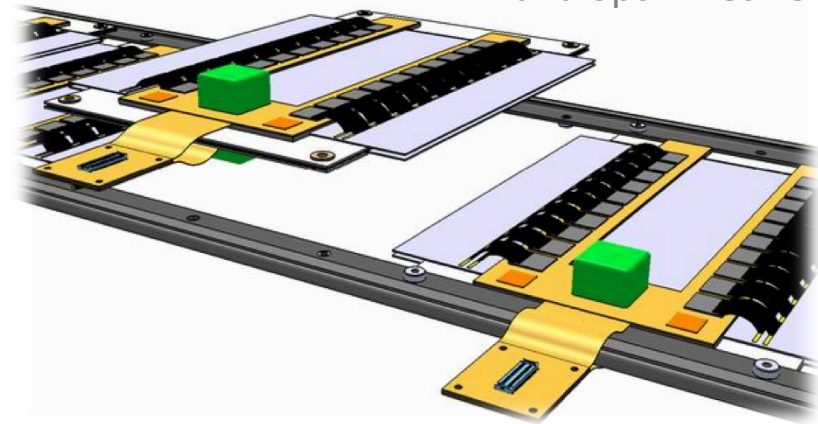


Extrapolated version with ABCN130 & HCC



Super Module Thermo-Mechanical FEA

Integration of modules on the cooling plates and optimized LS



- 1-unit and 3-unit cooling blocks being considered
- CTE of back-bone and cooling plates: 0 – -0.5 ppm/°K (tuned)
deflection between 0 and -25 μm for $\Delta T = 40\text{ °C}$
- CTE of service bus: 18 – 20 ppm/°K
deflection of order 1 mm for $\Delta T = 40\text{ °C}$
- No “distortion” acceptable from service bus
- Service bus must be stabilized:
 - wavy bus attached at each module?
 - stabilized with bonded carbon fibre?

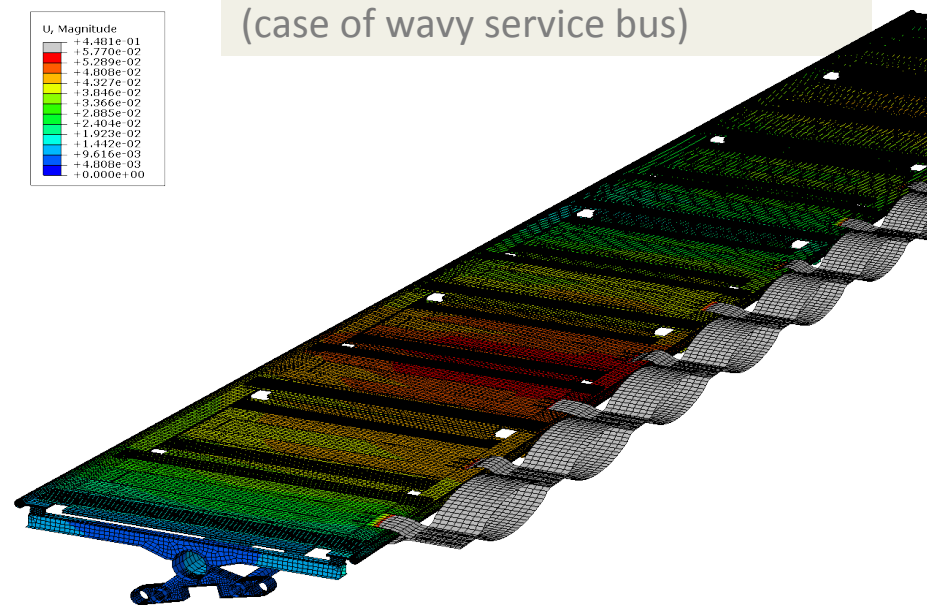
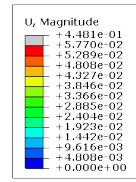
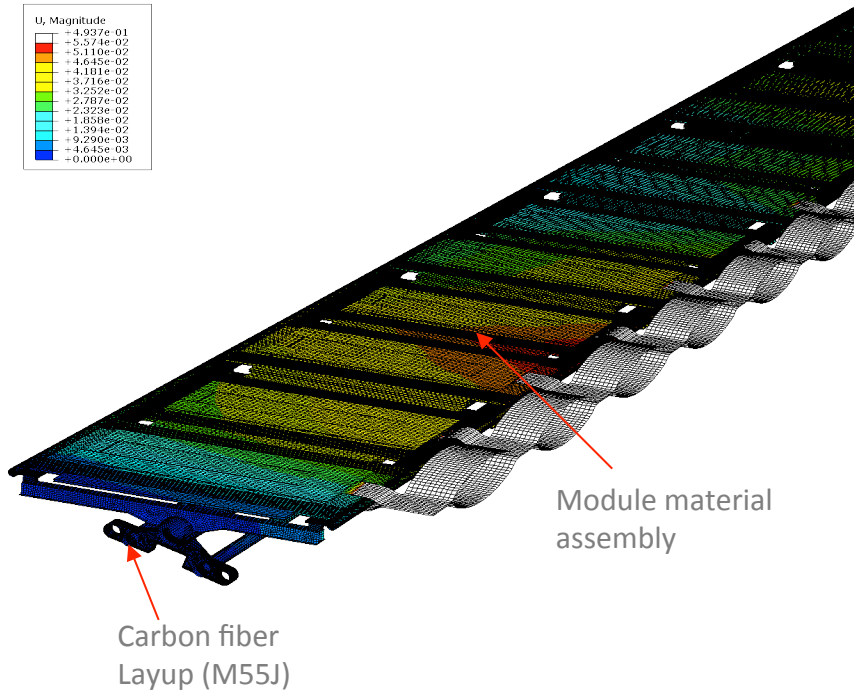
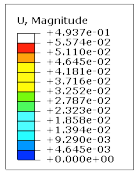


Thermo-mechanical behaviour to be understood:

- Modules on LS (kinematic mounting)
- Cable bus with respect to modules
(the major unresolved issue)

ABCN130 – Thermo-mechanical FEA at SM Level – Sag and Distortion

(case of wavy service bus)



Maximum distortion including:

- gravitational sag
- service bus

55 μm

Maximum distortion including:

- gravitational sag
- service bus
- T(coolant) = -35 °C

57 μm

Worst-case: vertical (other orientations significantly less)

Final detailed result will be determined by:

- final service bus construction and attachment
- Number and rigidity of fixed supports
- CTE tuning of the LS and cooling blocks

Maximum stress: LS < 8 Gpa, mounted modules < 21 Gpa

Material Budget Estimation

Item	Rad. length [% X0]	
Module with CC bridge (12mm width)	-	1.59
Module without CC bridge	1.49	-
Local support	0.18	0.18
Cooling plates	0.17	0.17
Bracket, inserts (interface to cylinder)	0.08	0.08
Cooling pipe (Ti 2mm)	0.04	0.04
Cable bus Al/Cu	0.11	0.11
Total	2.07	2.17

**Conservative
Needs optimization**


Extracted from evolving excel spreadsheet

NB:

- The sensor thickness is considered 320 μm. If 250 μm one gains 0.15%.
- List above does not include the power cards: serial power interface or DC-DC card
- Module without CC bridge means that the hybrid flex is directly glued on top of the Si-sensor.

Comments and Conclusions

1. The double-sided super-module prototype R&D using ABCN250 chip now concluded (currently back-up option in ATLAS Phase II LOI)

- **Required noise performance** on single module test box, combined module test box and 8-module SM prototype achieved (DC-DC LV powering, individual HV powering)
 - Ground and shielding Improvements for next-generation SM identified
 - **Position accuracy and mechanical (thermo-mechanical) stability for modules, and super-modules on LS demonstrated** (design optimized for thermal stability)
 - **Competitive material budget** while retaining good thermal-mechanical behaviour
- +
- **Design flexibility** enables parallelism of procurement and construction
 - Construction **modularity** expected to minimize rework and component cost
- 
- Not discussed here

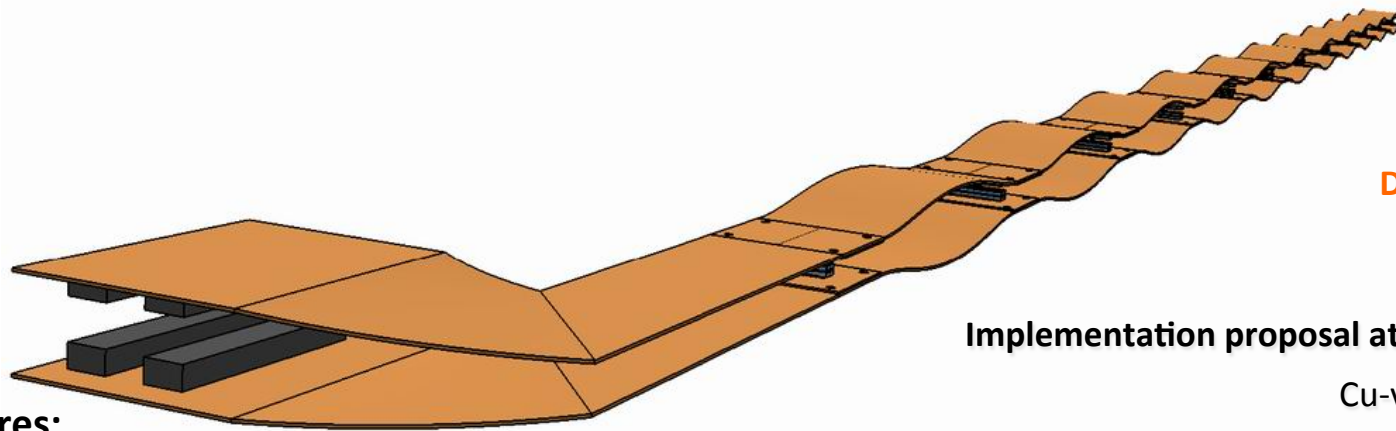
2. Preparation for realistic “pre-production” prototype described

- Use ABCN130, HCC and a dedicated service bus
- **Optimization of service bus for selected LV and HV powering schemes a key issue**
- Test beam studies of “pre-production” module before/after irradiation a priority

Many thanks for your attention

BACKUP

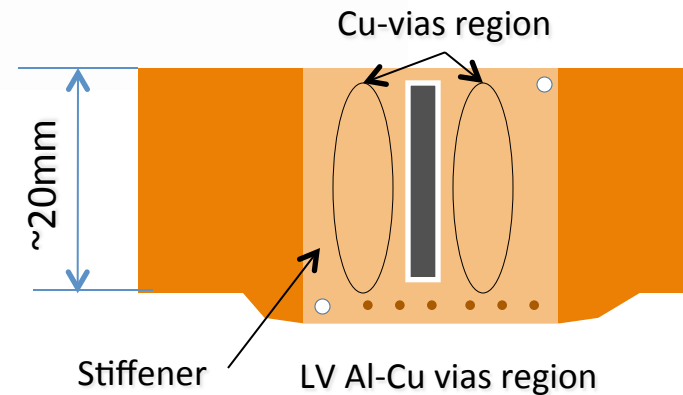
D. Ferrere, Y. Unno



Bus features:

- Length: 1250mm
- Width: 20 - 22mm
- Al layers: 2 x 50 microns (width from 11 to 20mm step)
- Cu layers: - 2 layers of 15 microns: LVDS + HV + DCS
- 1 mesh layers of 5microns for LVDS impedance

Implementation proposal at pigtail connection



Bus material	X/X0 [%]
Al layers - GND + bias (100 microns)	0.0174
Kapton + glue (240 microns)	0.0136
Other Cu layers (eq. 10 microns)	0.0155
Stiffeners (22x14x0.3 mm3)	0.0029
Connector (estimate)	0.0050
Total (1 side)	0.0544
Total (2 sides)	0.1088

NB:

- Optimization of Al thickness vs resistivity and cable power loss
100µm Al → 1.8W
- Time scale for design + fab:
5 -6 months

If 60 µm Cu → 0.204%
If 100 µm Cu → 0.291%

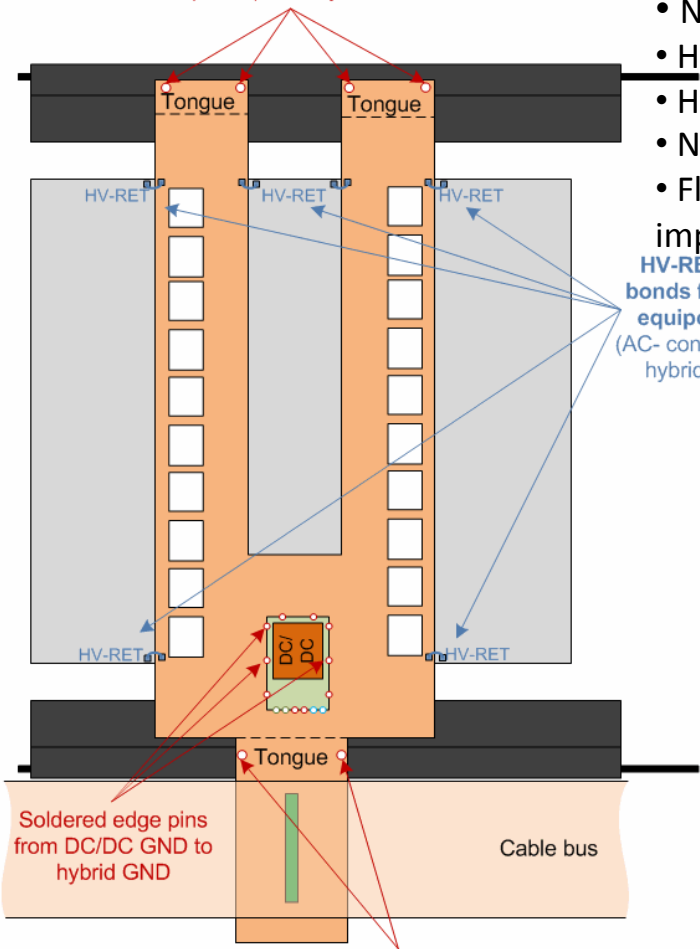
On-detector noise due to local DC-DC converters and digital activities need to be considered when designing the module and the super-module

This has been investigated for the super-module prototype with success and some anticipations for grounding the hybrid, module and super-module to the surrounding is proposed:

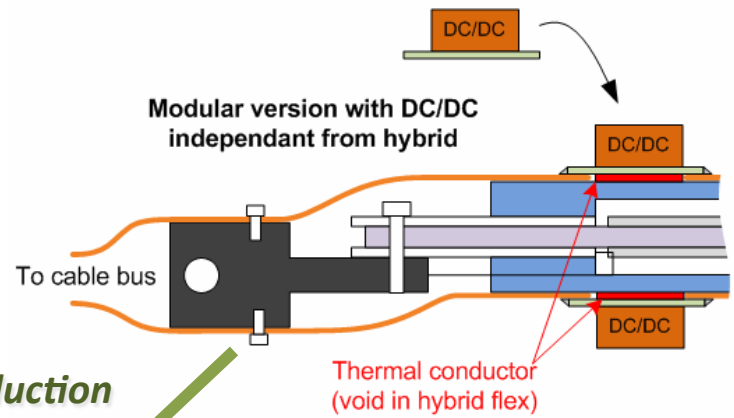
Connection (screw) from hybrid GND to CC conductor

- Need good shielding of DC-DC (noise source)
- HV return to be connected in AC to hybrid GND (several points)
- Hybrid GND to be connected to cooling plates (several points)
- Need to check the HF impedance of the cooling plate
- Flanges to be coupled to the ATLAS star point GND with very low HF impedance

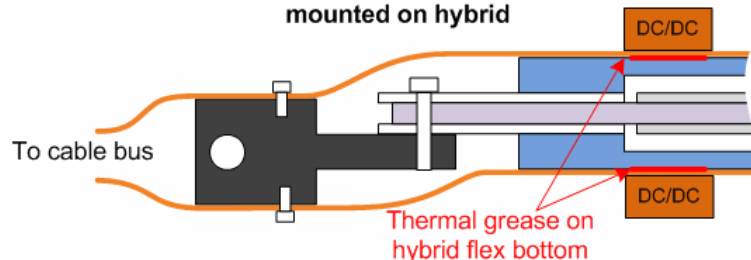
HV-RET wire bonds for good equipotential (AC- connection to hybrid GND)



Towards production



Final version with DC/DC mounted on hybrid



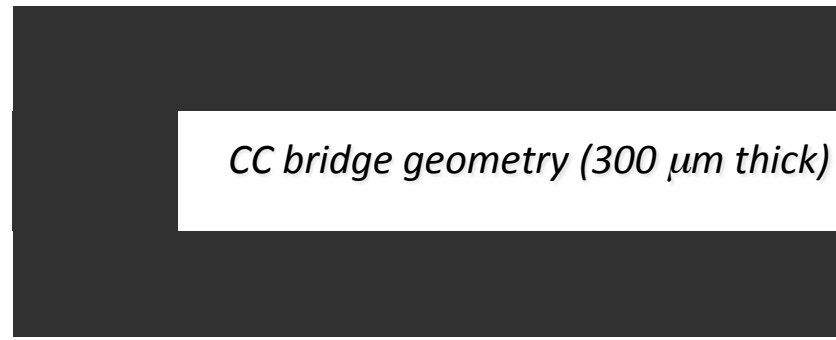
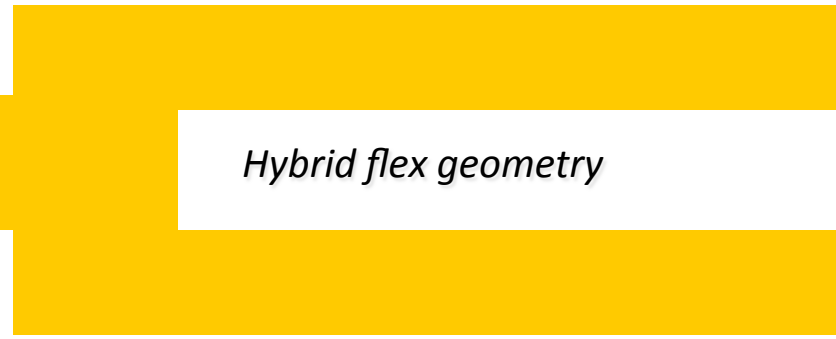
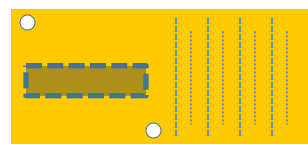
Other Adv : Stress relief (CTE mismatch with cable bus flex)

Hybrid:

- Technology: same as for current ABCN250
- Same for the two module sides

AXT Panasonic connector:

- Same as for IBL PPO
- From 10 to 80 pin contacts in 2 rows
- Pitch 0.4mm → 19.5mm width for 80 pins.
- 0.3A per contact
- 1kV ok with 2 interleaved missing contact pins
- Insertion/removal 50 times guaranteed



Socket



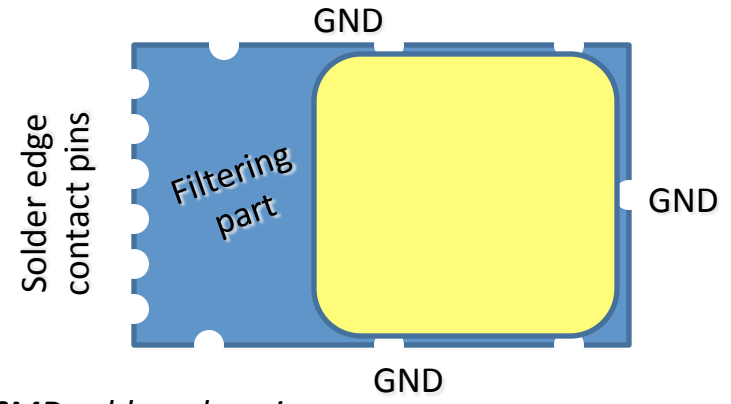
Header

DC-DC layout

- Targeting for future DC-DC converter board
- Estimated size: 20x13.5mm
- Height: should be reduced and hope for 5mm max
- Current estimates for 2 rows of 10 chips ABCN130: ~2.5A
- Local power dissipation due to inefficiency: 0.6 to 0.8W

NB:

- For prototype version: DC-DC board should be dismantable using SMD solder edge pins
- In production version: DC-DC should be integrated into the hybrid flex design (same GND, bias planes)

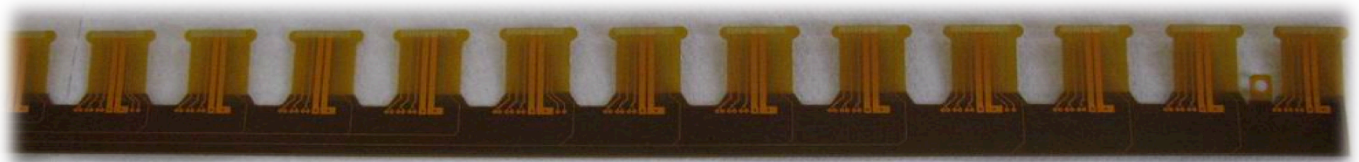


Alco flex made in fabrication for IBL (Genova – design, CERN – Fabrication)

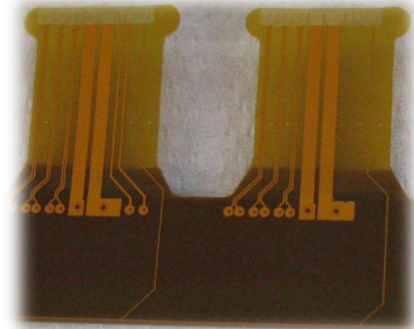
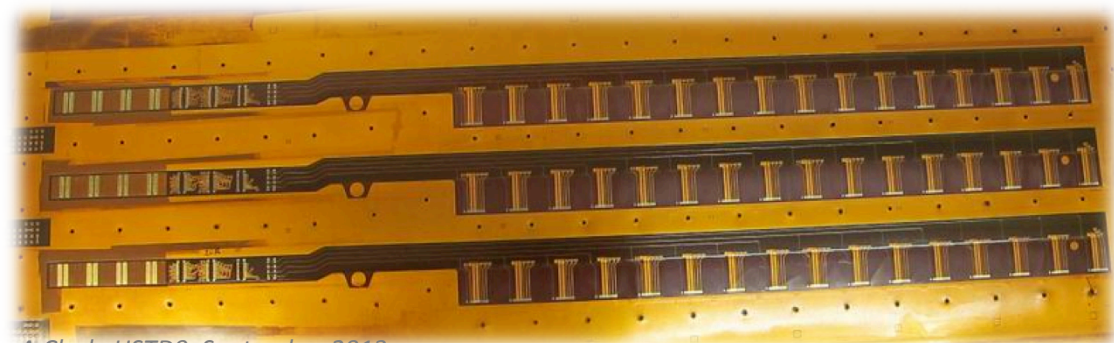
- 4 Cu layers (50 μm): 15 μm for HV, 15 μm LVDS1, 5 μm for GND ref, 15 μm LVDS2
- 2 Al layers (100 μm): 50 μm per power layer
- Multilayer of dielectric kapton/Pyralux (212.5 μm)
- Glue layers (85 microns)

From D. Ferrere (*in discussion with Rui and in perspective of the Upgrade*):

- *The 4 Cu-layers are standard process that could be outsourced*
- *The 2 Al-layers needs to be processed with CVD for Chrome and Copper (vias)*
- *Maximum length that could be processed by Rui's workshop 1.5m (not an issue / Super module)*
- *Flex production simpler than for IBL's (no special cutting for some layers like the wings...)*
- *Wavy flex for CTE mismatch with local support.
Could be thermally formed in a press!*



IBL production batch



**Wing part
(1 layer)**