Monolithic Detectors for High Energy Physics

Walter Snoeys

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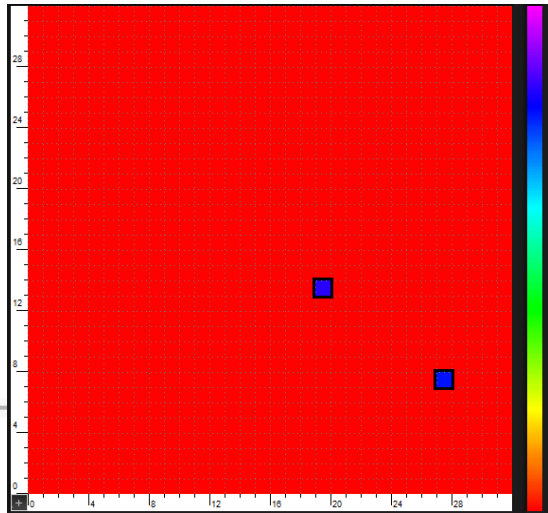
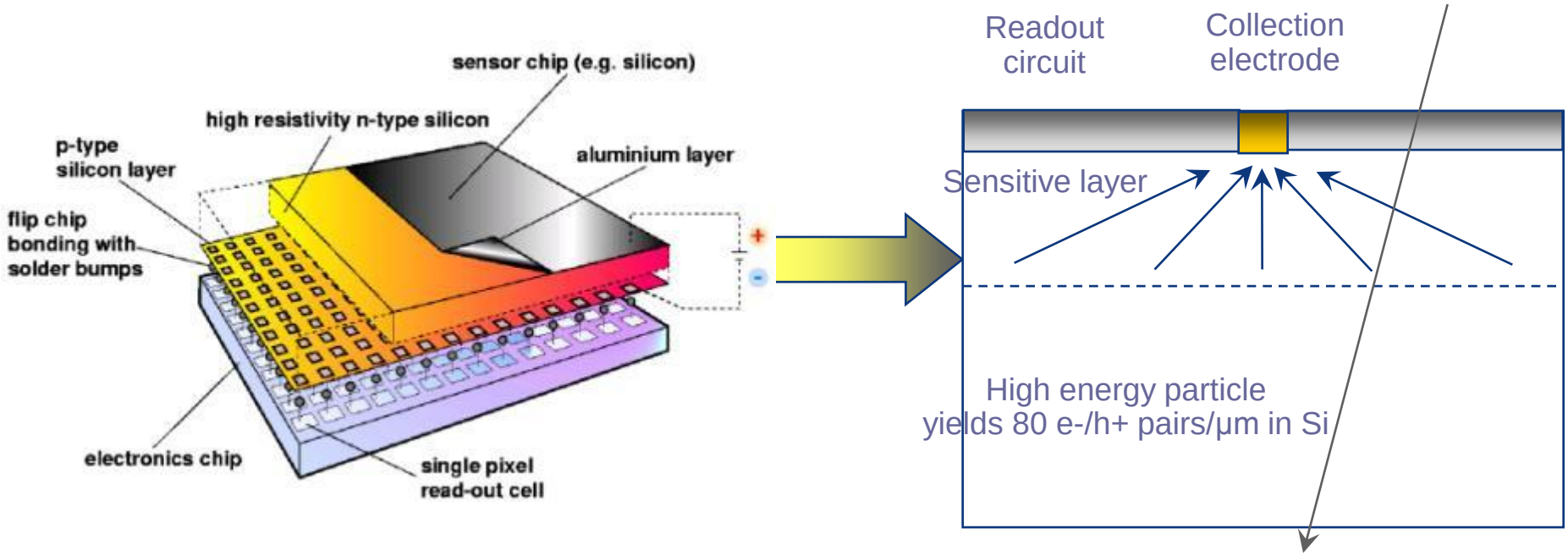
- A. Dorokhov, C. Hu, C. Colledani, M. Winter

- The conference organizers



MONOLITHIC DETECTORS : definition



Integrate the readout circuitry – or at least the front end – together with the detector in one piece of silicon

The charge generated by ionizing particle is collected on a designated collection electrode

MONOLITHIC DETECTORS

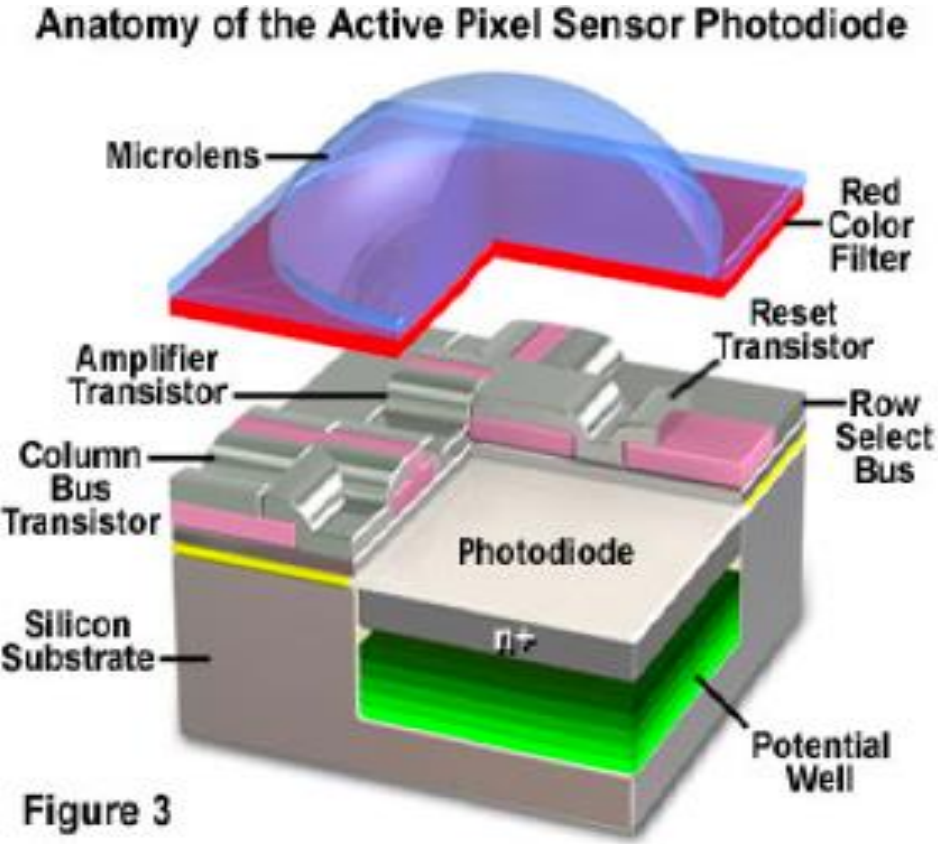
- Easier integration, lower cost, possibly better power-performance ratio
- Promising not only for pixel detectors, but also for full trackers
- Potential of strong impact on power consumption and hence on material in high energy physics experiments

- In two experiments
  - DEPFET pixels in Belle-II (see S. Tanaka presentation this session)
  - MAPS in STAR experiment

    both relatively slow (row by row) readout, not always applicable
- Not yet in LHC, considered for upgrades (eg Alice) and for CLIC/ILC

- Will concentrate on CMOS monolithic detectors

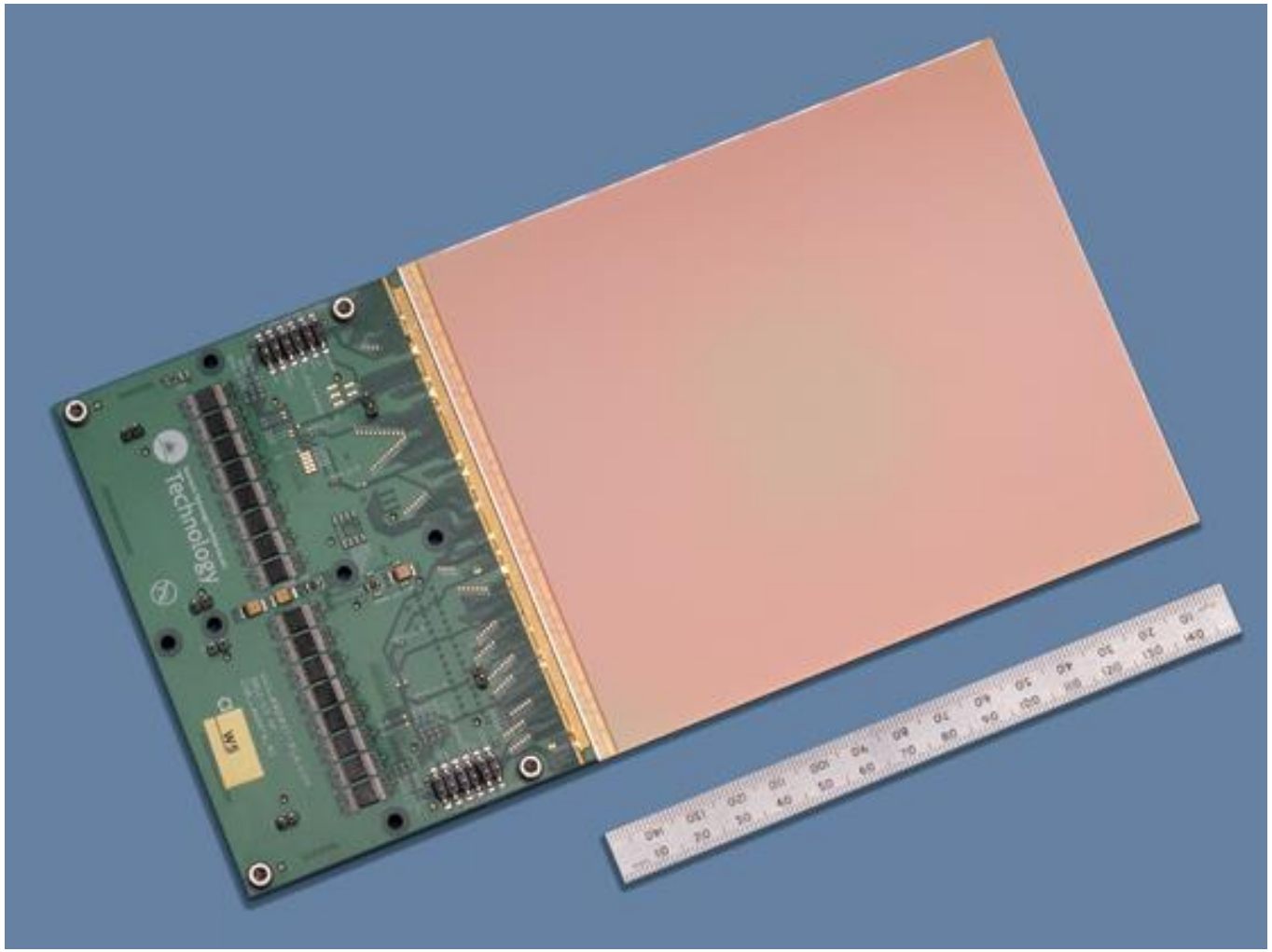
CMOS Monolithic Active Pixel Sensors



olympusmicro.com

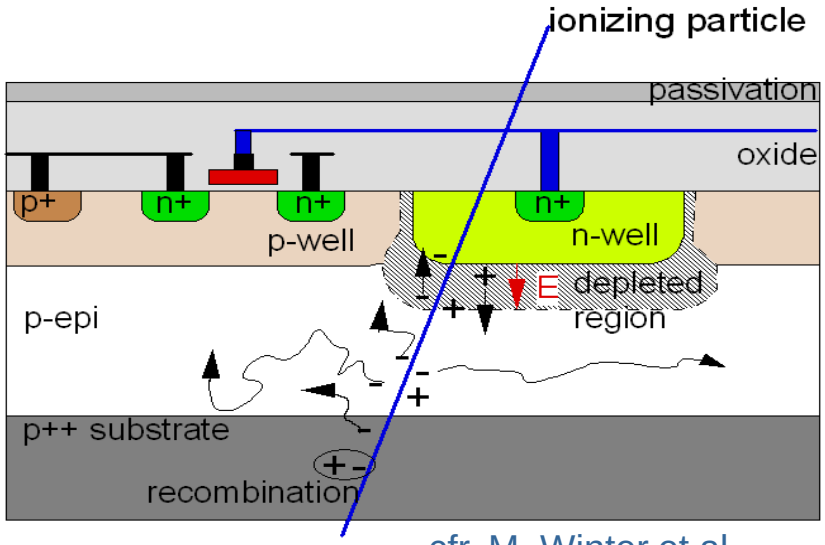
- Have changed the imaging world
- Reaching:
  - less than 1 e^- noise
    (cfr S. Kawahito, pixel 2012)
  - > 40 Mpixels
  - Wafer scale integration
  - …

WAFER SCALE INTEGRATION by STITCHING



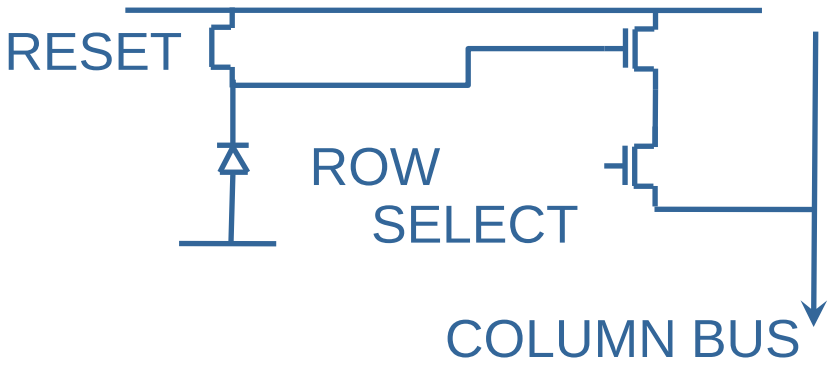
Courtesy: N. Guerrini, Rutherford Appleton Laboratory
Vth School on detectors and electronics for high energy physics, astrophysics, and space and medical physics applications, Legnaro, April 2013

Traditional Monolithic Active Pixel Sensors (MAPS)



cfr. M. Winter et al

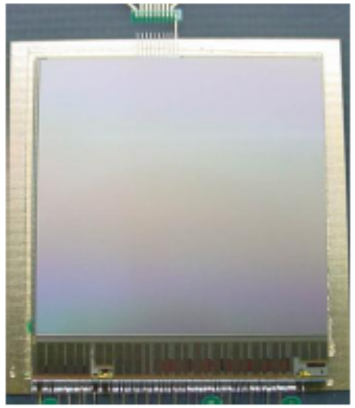
Example: three transistor cell



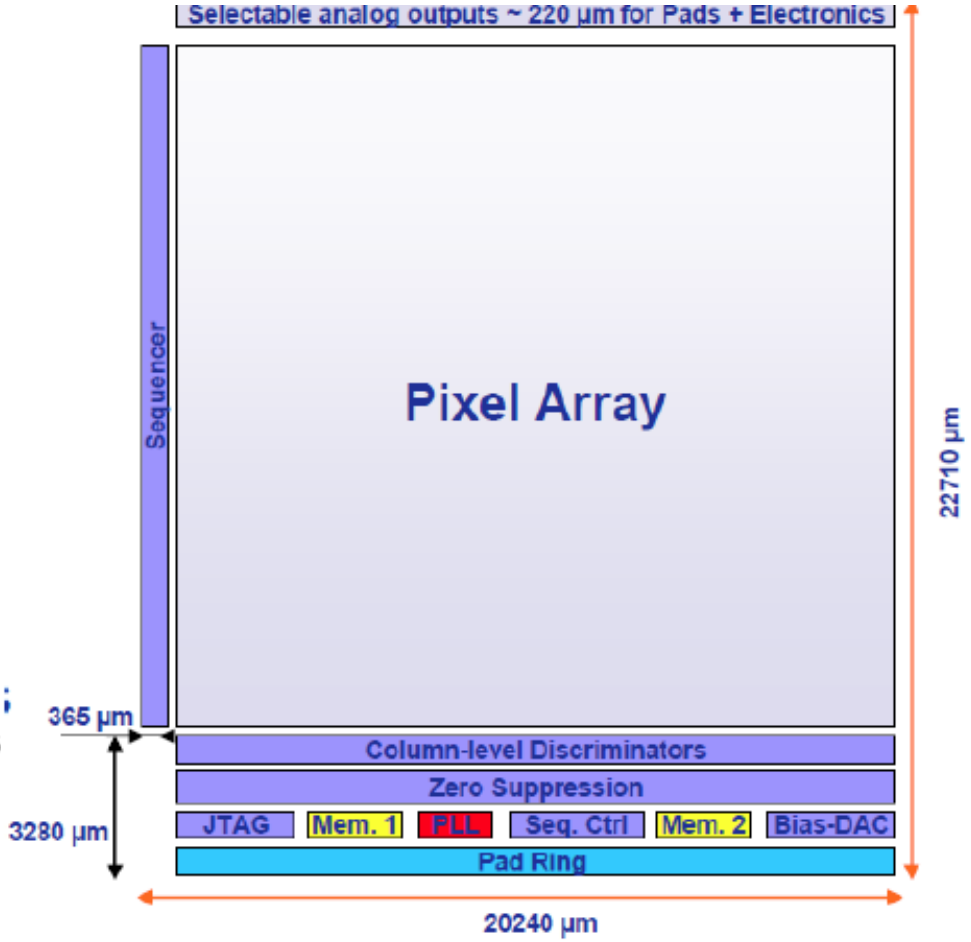
- Commercial CMOS technologies
- Very few transistors per cell
- Pixel size : 20 x 20 micron or lower

- Traditionally:
  - No back bias:
    - charge collection by diffusion
    - more sensitive to displacement damage in epitaxial layer/bulk
  - Only one type of transistor in pixel (unless triple well or transistors in collection electrode)
  - Rolling shutter readout
    - Very simple in-pixel circuit (3 or 4 transistors)
    - Serially, row-by-row, not very fast

ULTIMATE in STAR



- Reticle size (~ 4 cm²)
  - Pixel pitch 20.7 µm
  - 928 x 960 array ~890 k pixels
- Power dissipation ~170 mW/cm² @ 3.3V
- Short integration time 185.6 µs
- on-chip CDS, column level discriminators and zero suppression
- 2 LVDS data outputs @ 160 MHz
- Run length encoding on rows with up to 9 hits/row.
- Ping-pong memory for frame readout (~1000 hits deep)
- High Res Si option – significantly increases S/N and radiation tolerance.



Developed by IPHC, Strasbourg France

What does high energy physics need ?

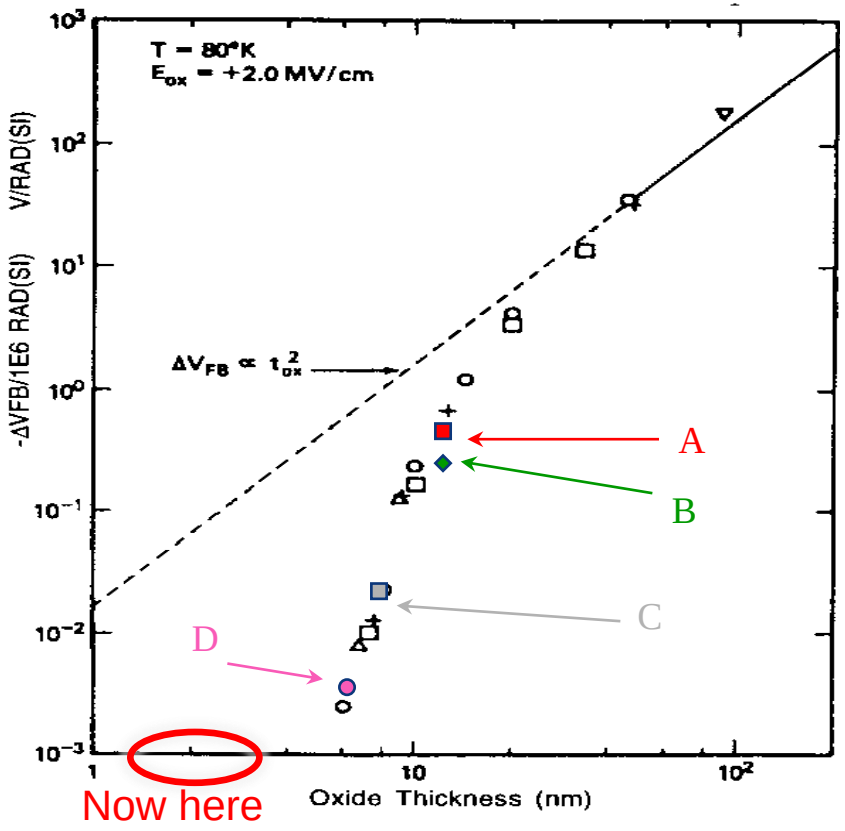
- Radiation tolerance of circuit and sensor
  - Ionizing radiation up to ~10^8 Mrad
  - Non-ionizing (displacement damage) up to ~10^{16} n_{eq}/cm^2
  - Circuit typically more sensitive to ionizing radiation, Sensor to non-ionizing radiation

- Single particle hits instead of continuously collected signal
  - 100% efficiency or close (fill factor close to 1)
  - Time stamping
  - Often more complex in-pixel circuit, full CMOS in-pixel desirable

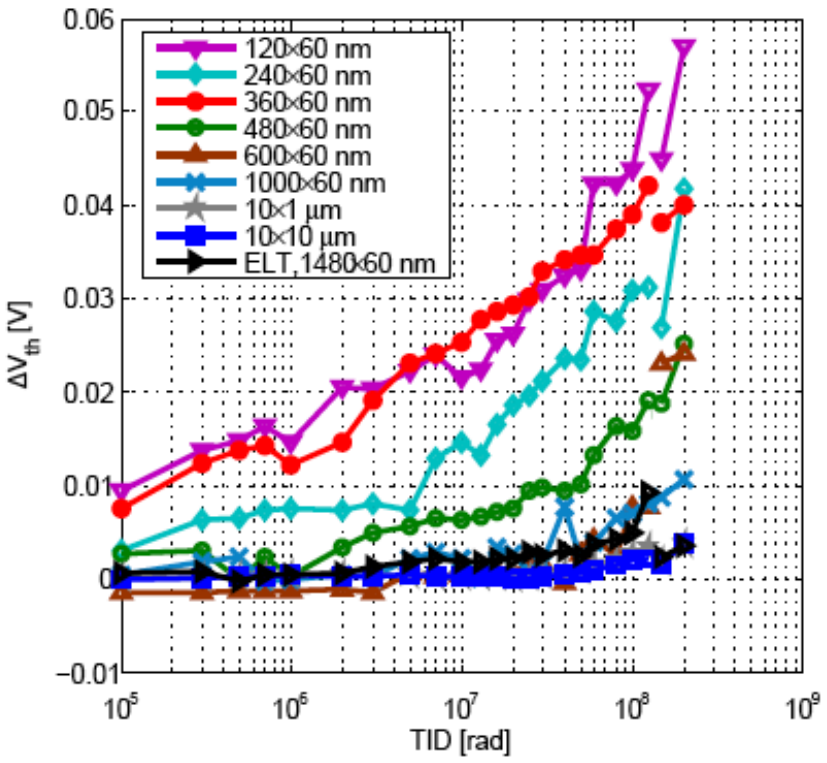
- Low power consumption as the key for low mass
  - Now ~ 20 mW/cm^2 for silicon trackers and > 200 mW/cm^2 for pixels
  - Even with enhanced detector functionality for upgrades, power consumption cannot increase because of the material penalty

CMOS and Ionizing Radiation Tolerance

- The industry standard for high volume low cost circuit manufacturing
- Transistor radiation tolerance comes for free :

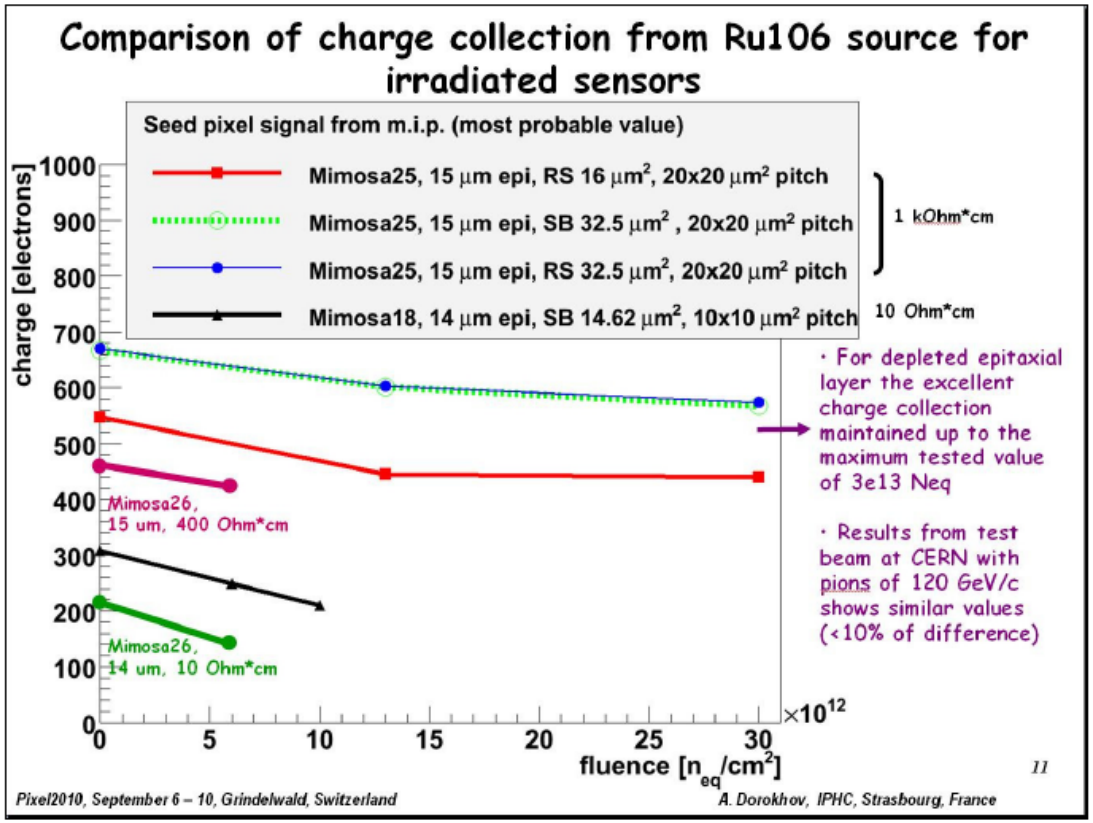


After N.S. Saks, M.G. Ancona, and J.A. Modolo, IEEE TNS, Vol. NS-31 (1984) 1249
Present day transistors fall on the curve measured in 1984 on oxide capacitors



For example: transistors in 65nm CMOS
After S. Bonacini et al.
If minimum size devices are avoided, small radiation induced shift even after extreme doses

Collection by diffusion and radiation tolerance



(A. Dorokhov et al., IPHC, France)

Collection by drift for radiation tolerance beyond $10^{13} n_{eq}/cm^2$!

=> need depletion and (some) back bias, for instance using HV CMOS (see next presentation)

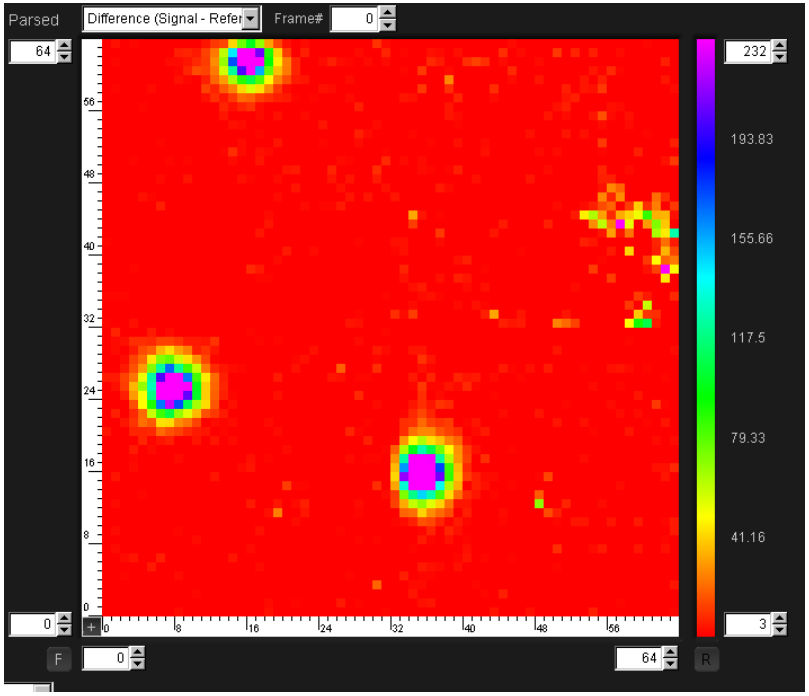
Tolerance against displacement damage

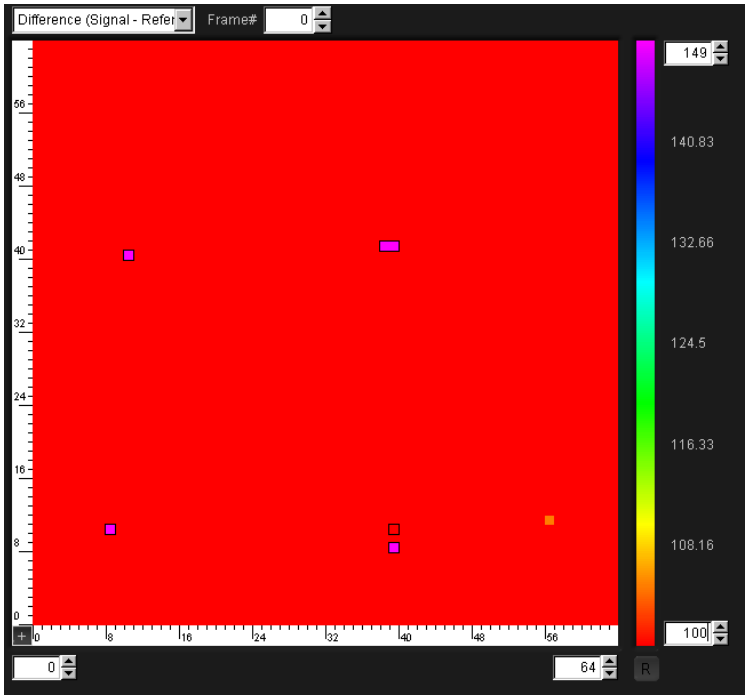
- Reverse bias to obtain collection by drift in a depleted region is essential for tolerance to fluences beyond 10^{13} n_{eq}/cm^2
- Reverse bias also helps:
  - Signal-to-Noise (see C. Cavicchioli's presentation)
    - Lower capacitance
    - Often larger collection depth (larger depletion)

    (but not necessarily if epitaxial layer over highly doped substrate)
  - Lower cluster size (see next slide), very important for architecture
  - Lower collection time
- Can also work on other parameters to ease/enhance depletion depth:
  - Higher resistivity and thickness of the epitaxial layer

DRIFT vs DIFFUSION – influence on cluster size

Measurement on LePIX prototypes (50x50 micron pixels !)



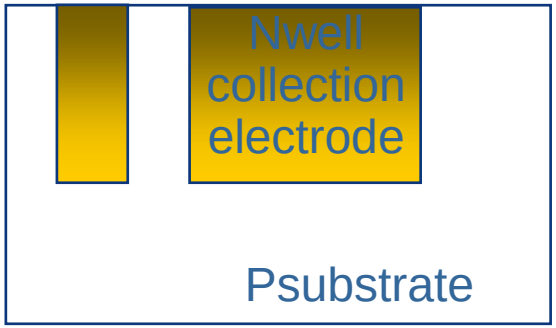


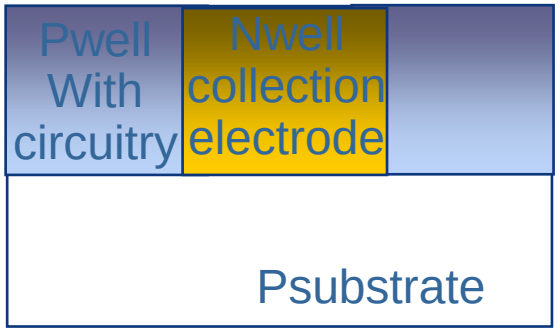
0 Volts bias

60 Volts bias

- *Diffusion:* at zero bias, incident protons generate on average clusters of more than 30 50x50 micron pixels.
- *Drift:* for significant reverse bias (60V) cluster reduced to a few pixels only

MORE COMPLEX CIRCUITRY: device solutions





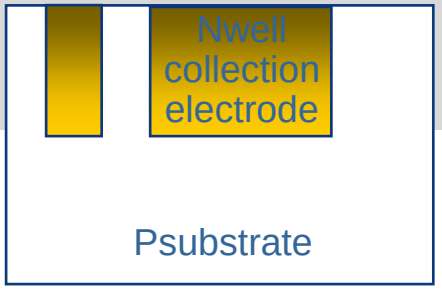
- Additional N-diffusion will collect and cause loss of signal charge
- → Need wells to shield circuitry and guide charge to the collection electrode for full efficiency

Pwell with NMOS transistors next to Nwell collection electrode

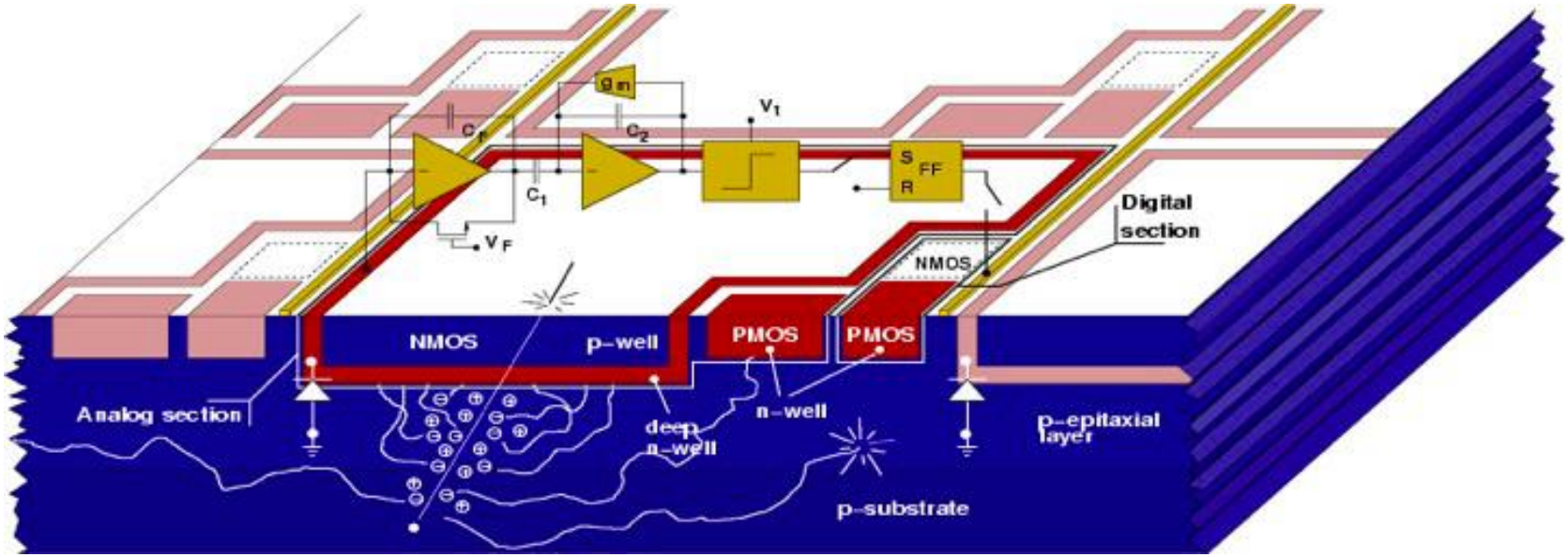
junction on the front

- Used by MAPs but important diffusion component at small bias
- Large fields for more significant reverse bias
- Uniform depletion with small Nwell and large Pwell difficult
- NMOS only in pixel

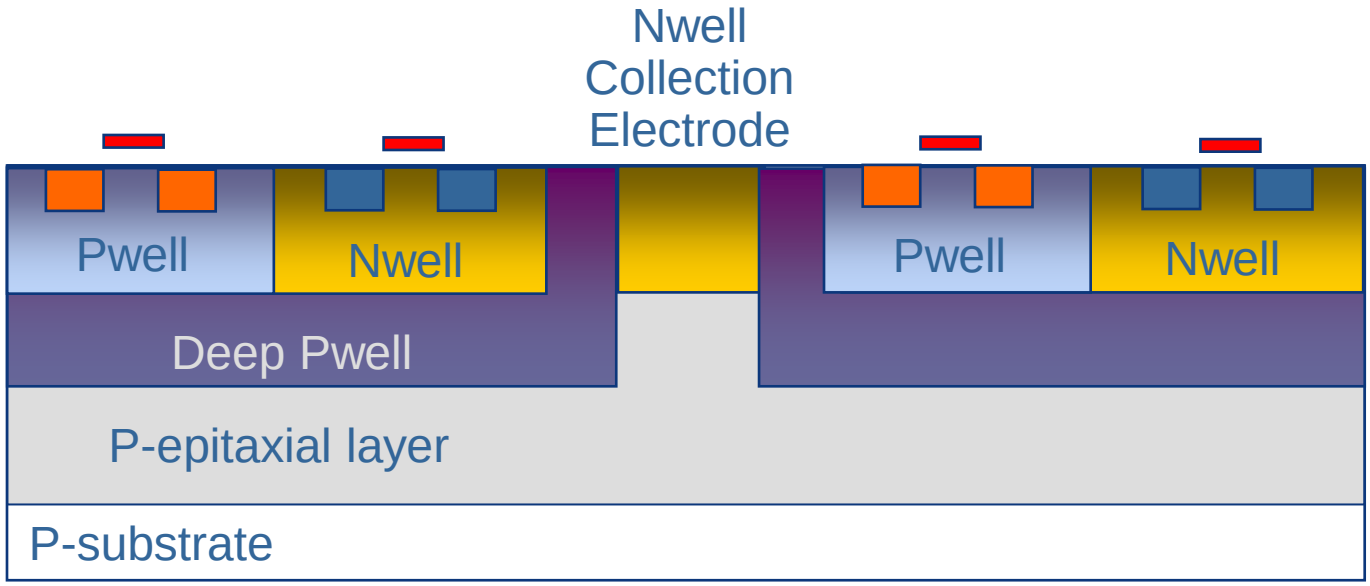
No shielding well



- G. Vanstraelen (NIMA305, pp. 541-548, 1991)
- V. Re et al., superB development: Nwell containing PMOS transistors not shielded
- Nwell much deeper than rest of circuit to limit inefficiency

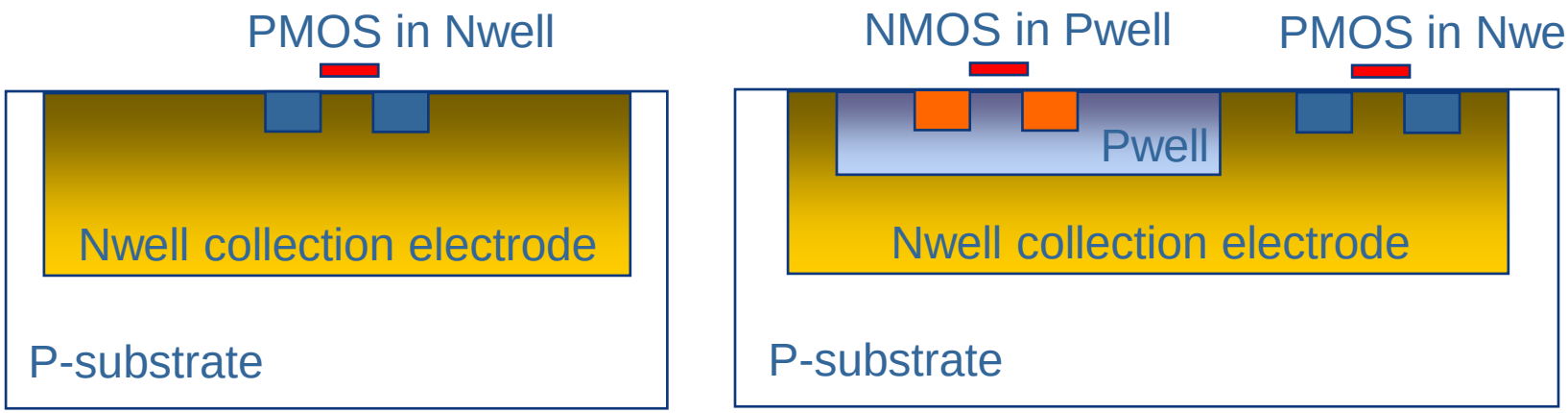


JUNCTION ON THE FRONT with DEEP PWELL



- Deep Pwell shields Nwell from the epitaxial layer
- Example: ALICE ITS upgrade (see C. Cavicchioli's presentation)
- Difficult to deplete epitaxial layer under Pwell far from Nwell collection electrode
- So, either very simple in-pixel circuit or important diffusion component in the charge collection

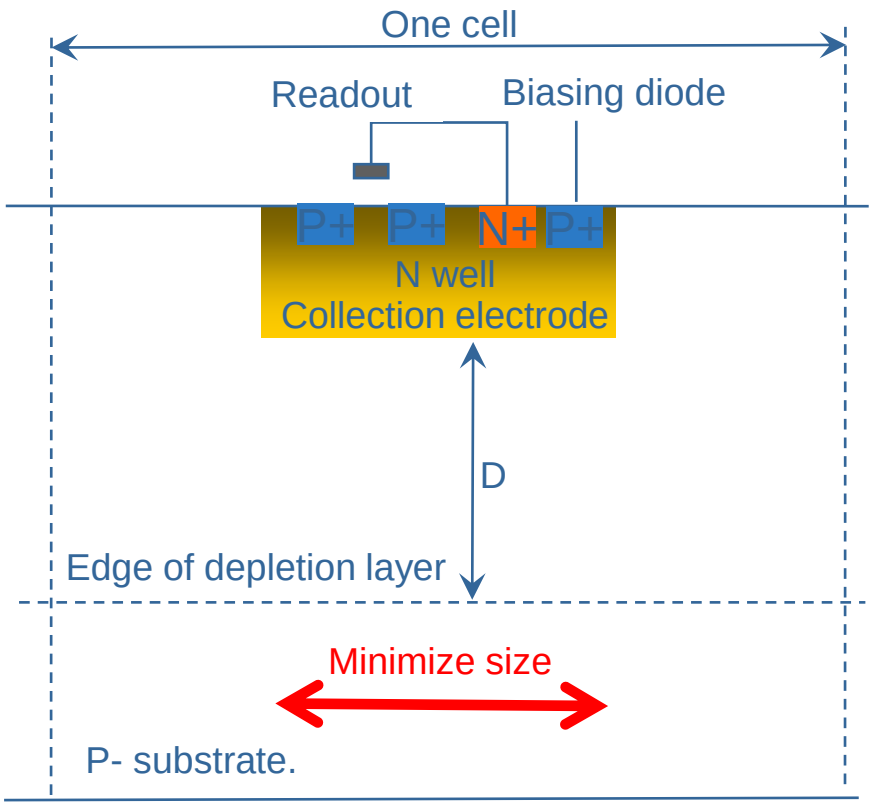
CIRCUIT INSIDE COLLECTION ELECTRODE

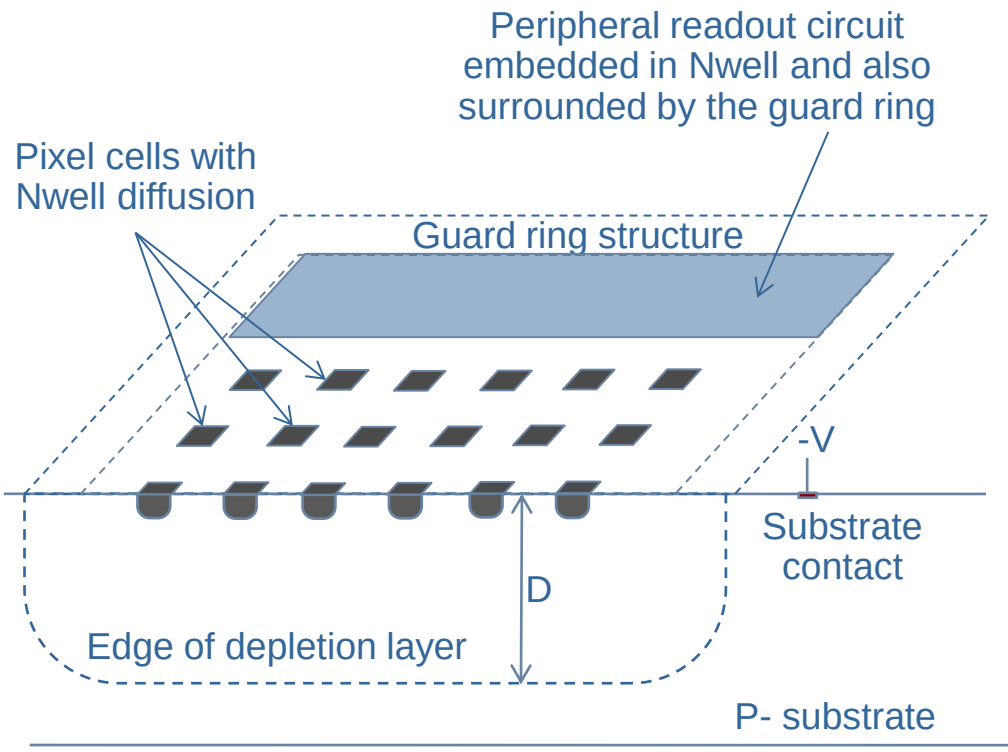


All circuitry in Nwell, with or without triple well for full CMOS or only PMOS in the pixel (eg LePix)

- Risk of coupling circuit signals into input
- In-pixel circuit simple in small collection electrode for low C by
  - 'rolling shutter' readout as in MAPS,
  - special architectures (see below), or
  - use it as smart detector in hybrid solution (cfr I. Peric)

All in NWELL: LePIX: 90nm CMOS on high resistivity

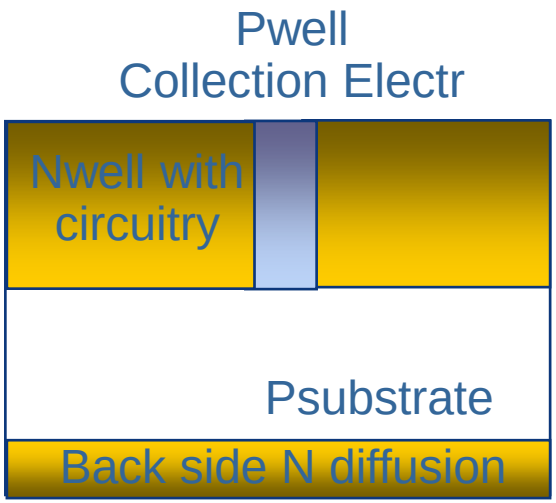


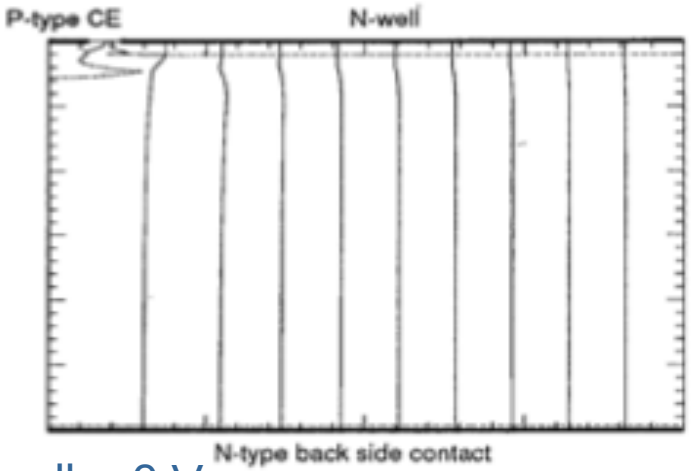


Try to maximize Q/C: small collection electrode, and high resistivity substrate of several 100 Ωcm, 40 microns depletion for ~40 V

Collection by drift for radiation tolerance

WELL WITH JUNCTION ON THE BACK

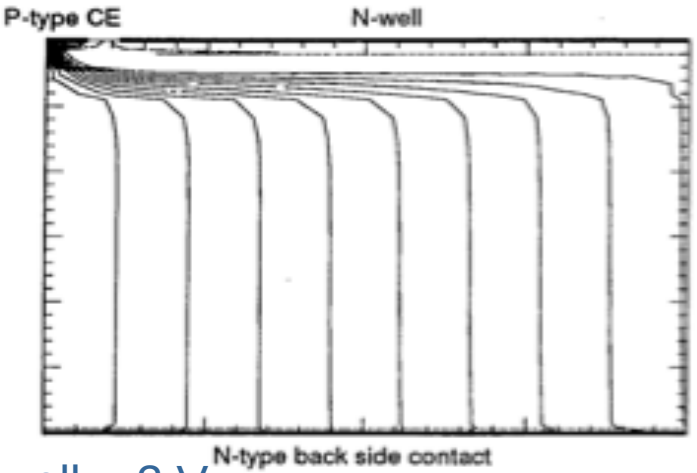




Vnwell = 0 V

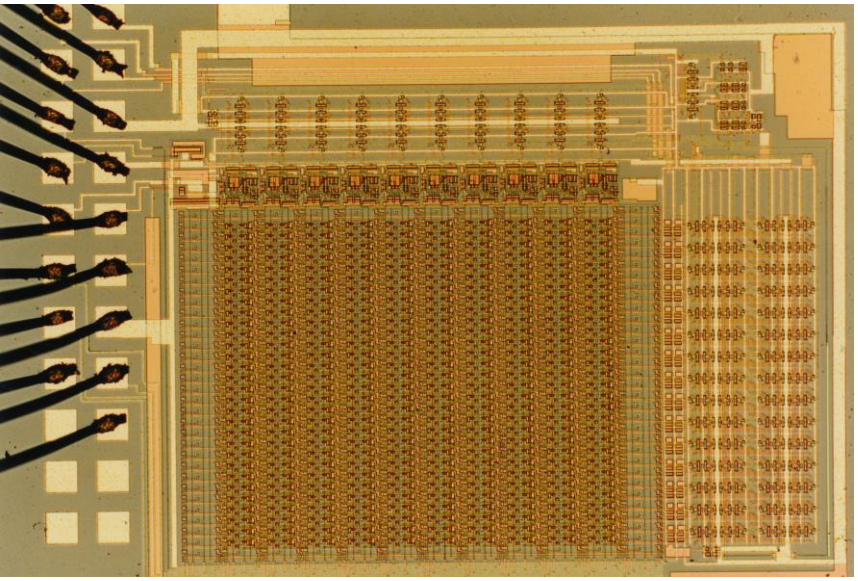
Wells with junction on the back

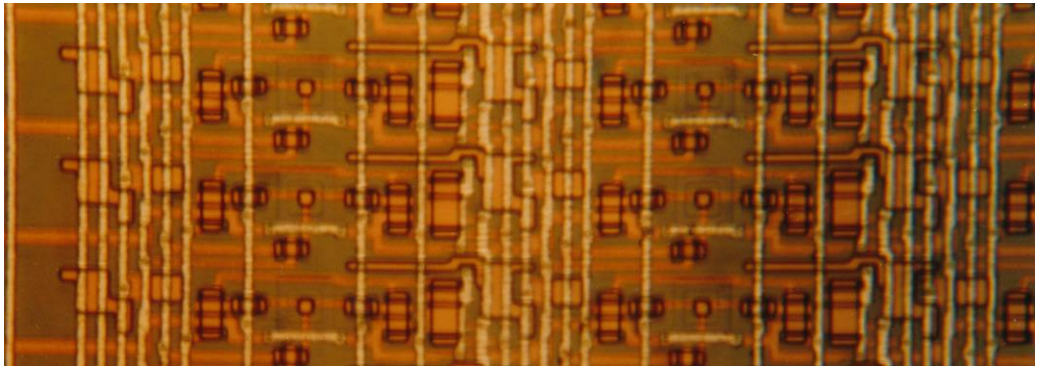
- Need full depletion
- Works well, a few V on the Nwell diverts the flow lines to the collection electrode
- Stanford-Hawaii development
- Double-sided process difficult, not really compatible with standard foundries

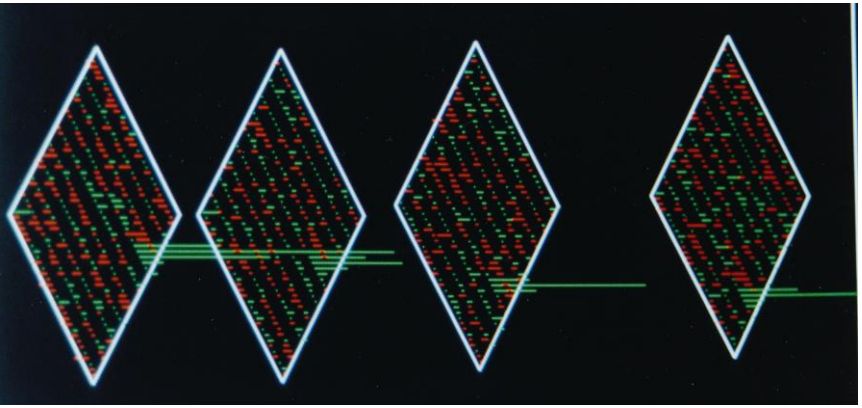


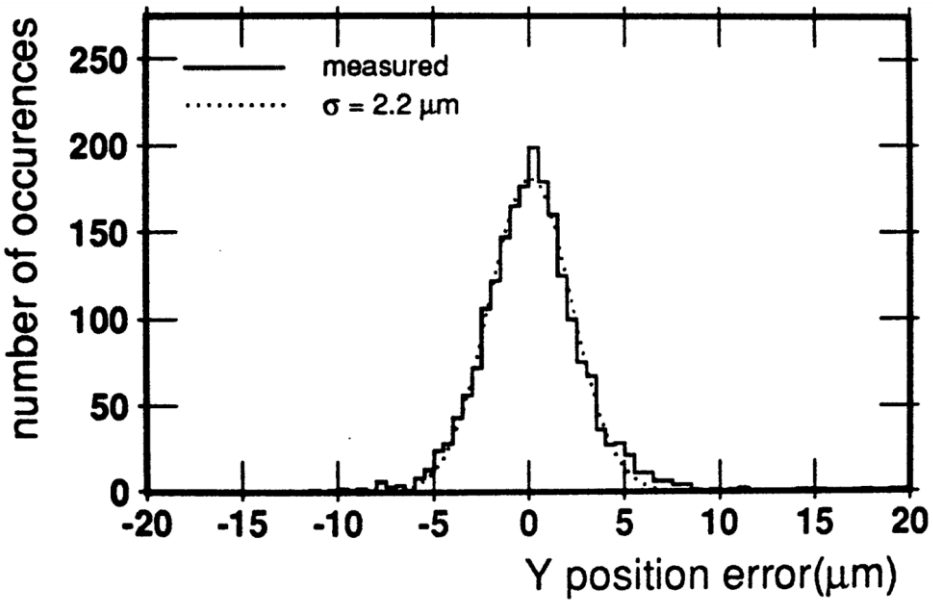
Vnwell = 2 V

WELL WITH JUNCTION ON THE BACK





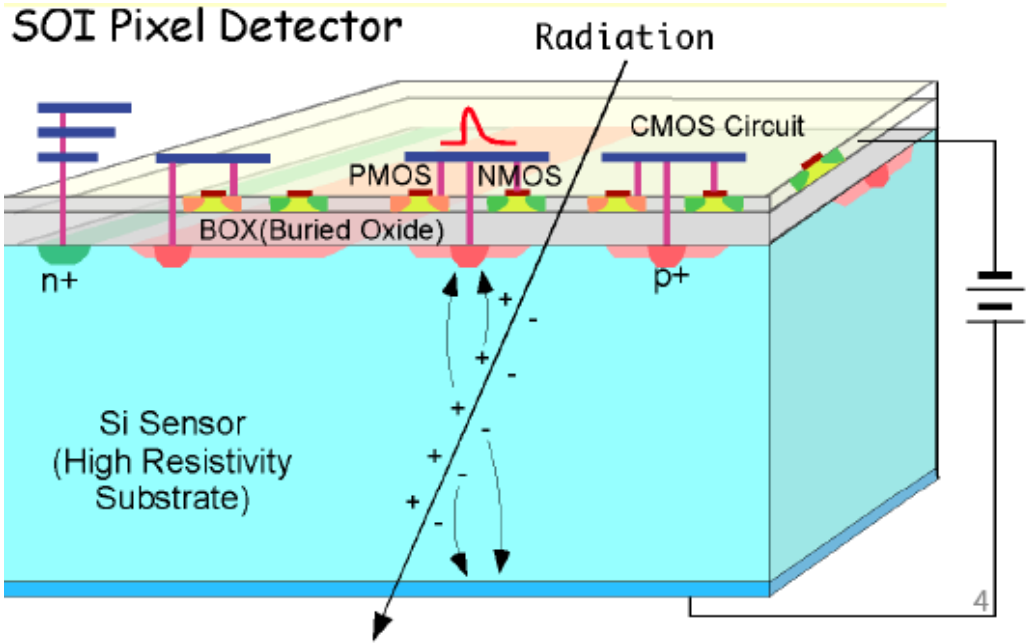




C=26fF P-type 1E12 cm^3

C. Kenney, S. Parker (U. of Hawaii), W. Snoeys, J. Plummer (Stanford U) 1992

SILICON ON INSULATOR (SOI)

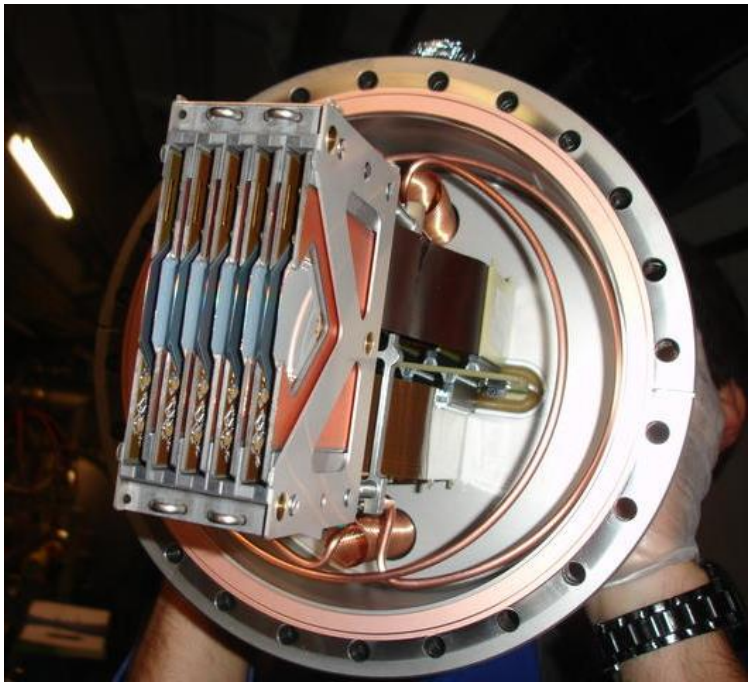


Y. Arai et al (see presentations later this session)

- Very impressive technology development … offers good Q/C
- High weak inversion slope (<70 mV/decade)
- BOX causes reduced radiation tolerance, double BOX improves this, further development in progress.
- Is one of the ways to integrate large amount of in-pixel circuitry

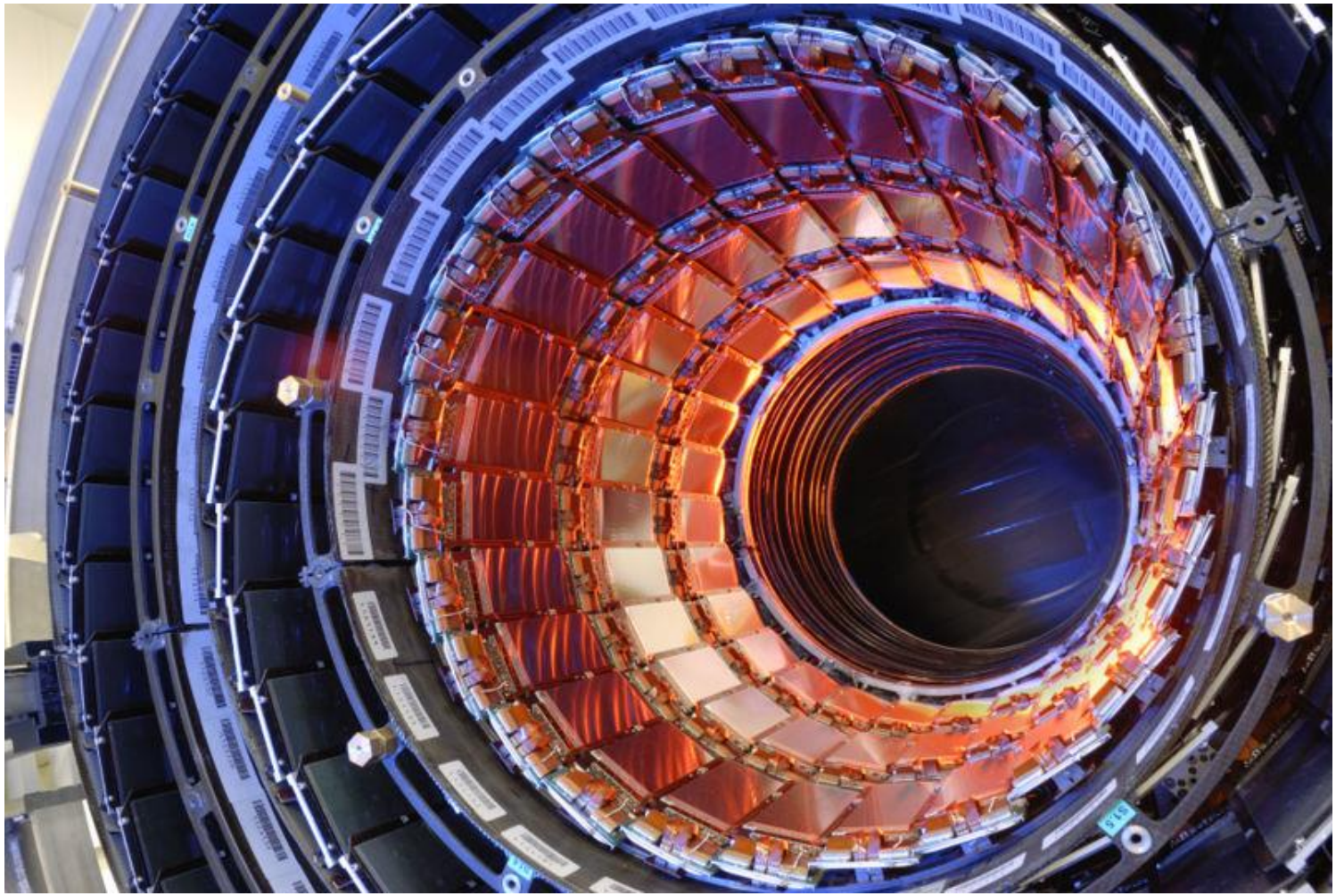
LOW POWER IS THE KEY TO LOW MASS

- Services: cables, power suppliers, cooling etc… represent signficant effort and fraction of the total budget
- Subject to severe spatial constraints, limit for future upgrades
- Power often consumed at CMOS voltages, so kWs mean kAs
- Increasing power for upgrades not really an option even if more functionality



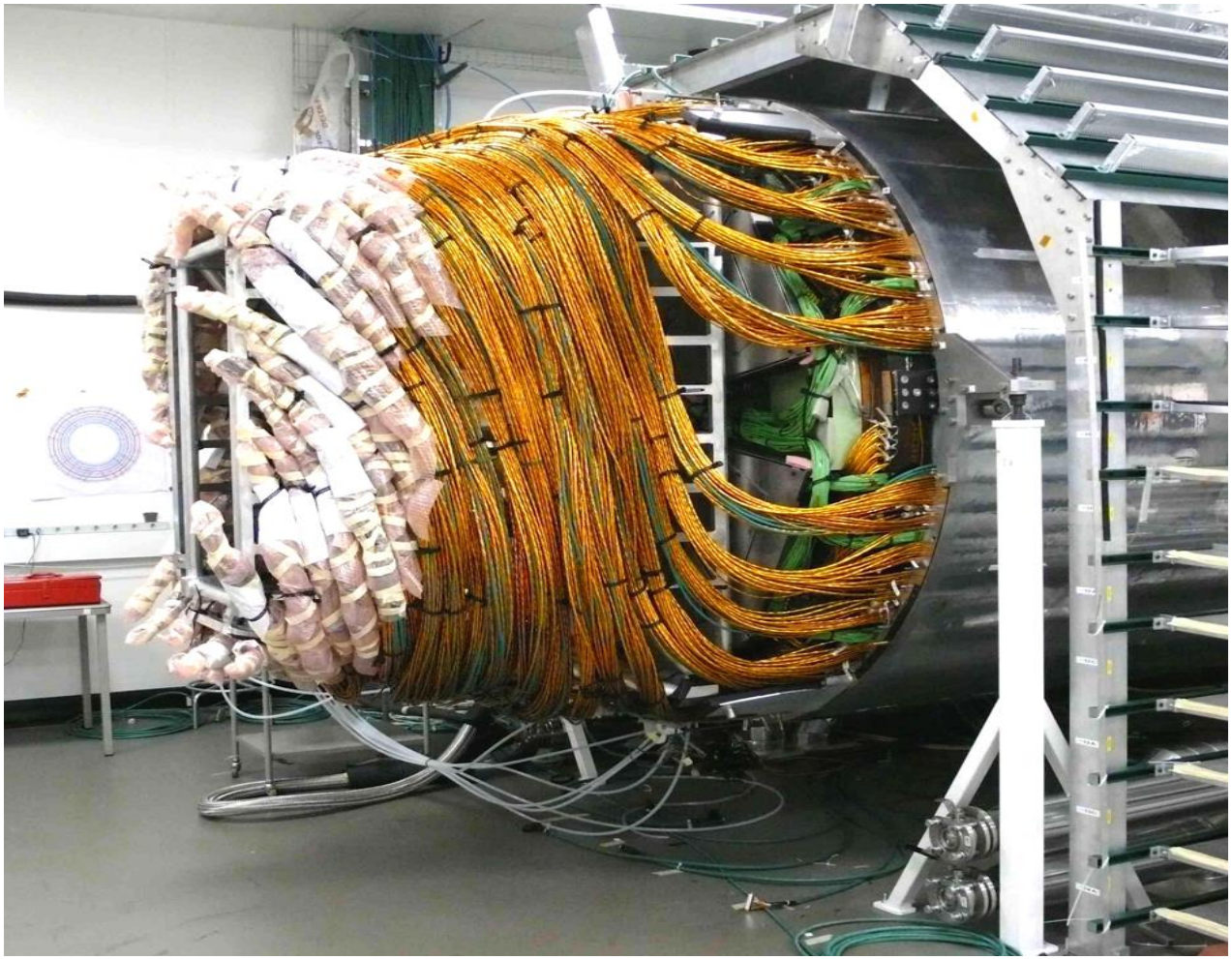
- ~ 20 mW/cm2 for silicon trackers
- ~ 2-300 mW/cm2 for silicon pixels
- Even if power for detector is low, voltage drop in the cables has to be minimized: example analog supply one TOTEM Roman Pot:
  - ~ 6A @ 2.5 V
  - ~100m 2x16mm^2 cable: 0.1 ohm or 0.6 V drop one way
  - 26kg of Copper for ~ 15 W

The CMS Tracker before dressing…



A. Marchioro / CERN

… and after



33 kW in the detector and… > 30 kW in the cables !

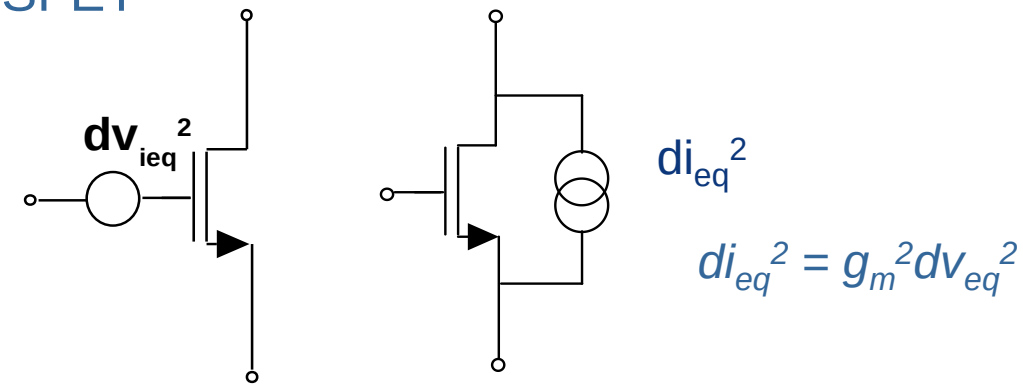
A. Marchioro / CERN

Power consumption: 3 components

- Analog:
  - Determined by collected charge over capacitance (Q/C) in the pixel => pixel sensor optimization
- Digital:
  - Determined by on-chip architecture & cluster size
  - Architecture:
    - Rolling shutter : relatively slow
    - Other architectures with in-pixel binary front-end:
      - Data driven (eg priority encoder for ALICE) (significant amount of in-pixel circuitry)
      - Projections along several axis (Y. Ono & P. Giubilato, pixel2012)
- Data transmission off-chip:
  - Determined by cluster size unless data reduction by clustering algorithm

ANALOG POWER CONSUMPTION

NOISE SOURCES IN A MOSFET EQUIVALENT WITH :



$$di_{eq}^2 = g_m^2 dv_{eq}^2$$

WHERE:

In weak inversion (WI):

$$g_m \sim I \qquad dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 2kTn/g_m)df$$

In strong inversion (SI) :

$$g_m \sim \sqrt{I} \qquad dv_{eq}^2 = (K_F/(WLCox^2 f^\alpha) + 4kT\gamma/g_m)df$$

Signal to noise ratio and analog power consumption

$$\frac{S}{N} \sim \frac{Q/C}{\sqrt{gm}} \sim \frac{Q}{C} \sqrt[m]{I} \sim \frac{Q}{C} \sqrt[m]{P} \text{ with } 2 \leq m \leq 4$$

or $$P \sim \left\{ \frac{\frac{S}{N}}{\frac{Q}{C}} \right\}^{m} \text{ with } 2 \leq m \leq 4$$

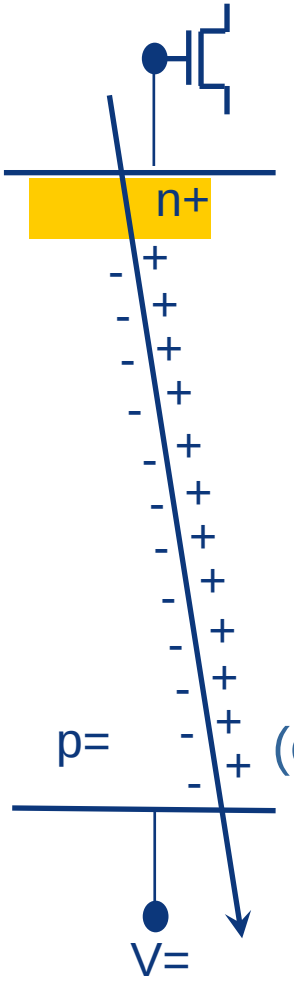
For constant S/N: $$P \sim \left[\frac{Q}{C} \right]^{-m} \text{ with } 2 \leq m \leq 4$$

Signal charge/detector capacitance (Q/C) is the figure of merit for the sensor determining the analog performance/power consumption

m = 2 for weak inversion up to 4 for strong inversion

High Q/C for low analog power

Transistor noise ≈ 0.16 mV at 40 MHz BW for 1 uA
(1uA/100x100 um pixel = 10 mW/sq cm)



$$\frac{S}{N} = 25 \Rightarrow \frac{Q}{C} = 4mV \left[= \frac{4\,fC}{1\,pF} \right] \left[= \frac{0.4\,fC}{0.1\,pF} \right] \left[= \frac{0.04\,fC}{10\,fF} \right]$$

Collection depth	300 μm	30 μm	3 μm

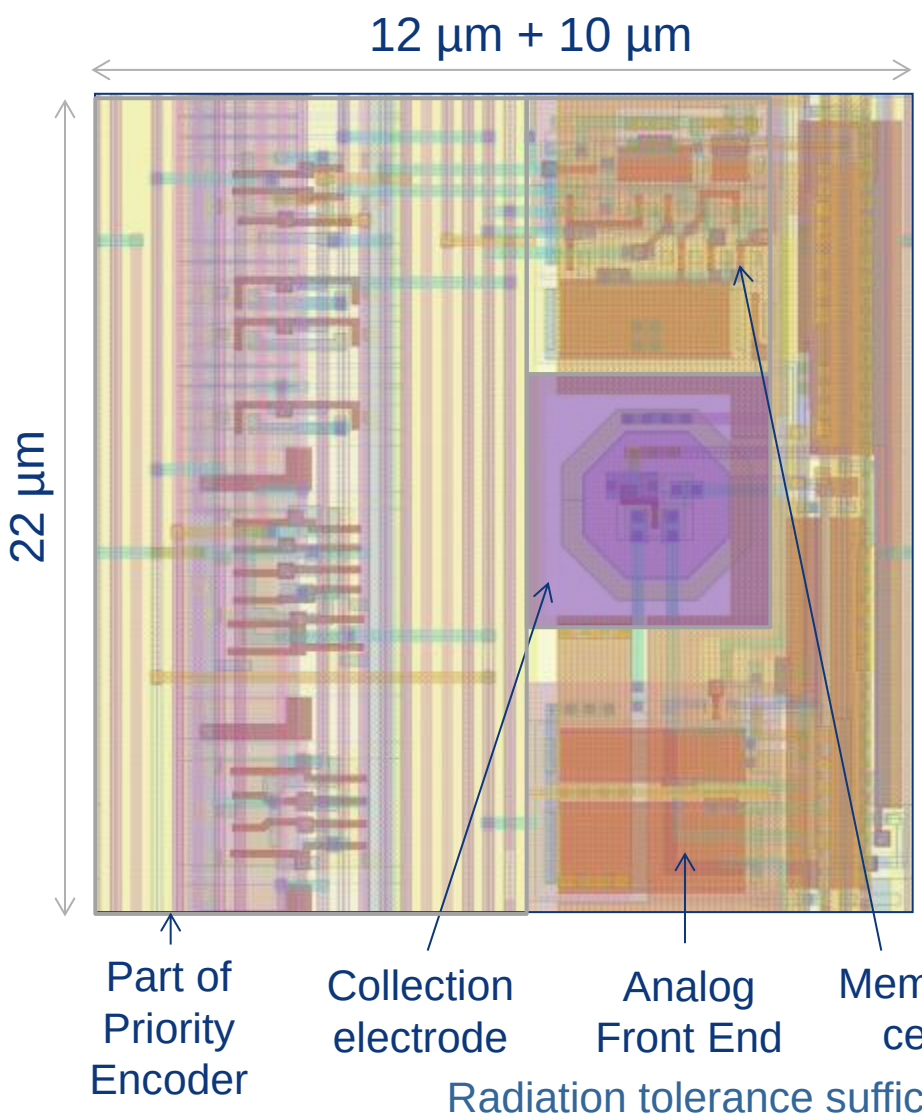
doubling Q/C allows
(at least) 4x power reduction for same S/N

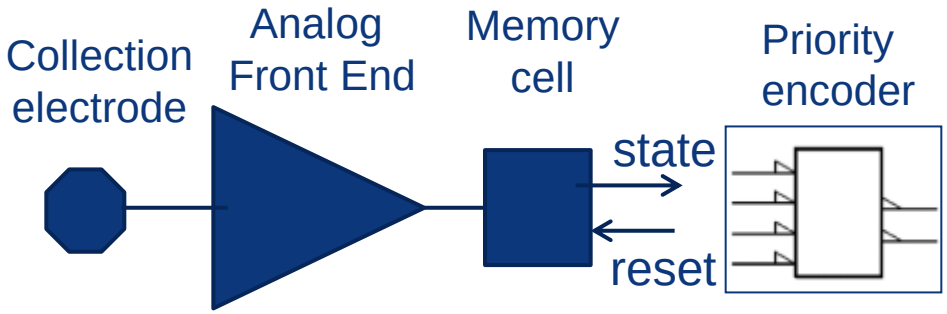
Monolithic →

Q/C = 50mV (0.25fC/5fF=50mV) can be achieved
(e.g. 20 μm collection depth and 5fF with charge on a single pixel)

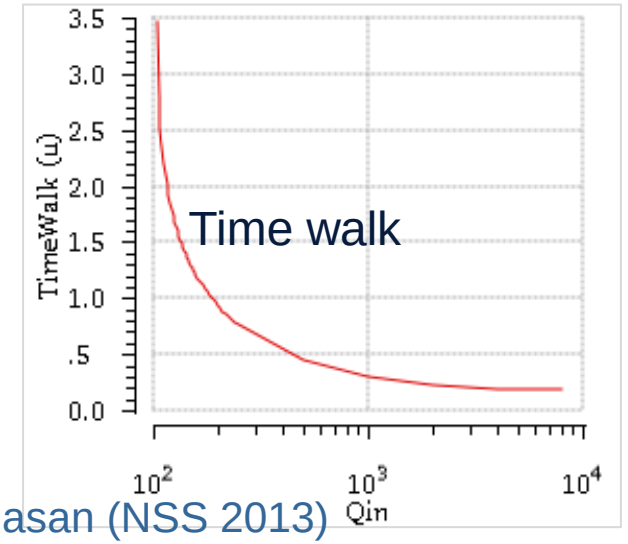
Much better than that would almost be a 'digital' signal

Binary Front End + Architecture : eg Priority Encoder





Binary Frontend (~ 40nW or ~10mW/cm^2 for 22x22 micron pixels) allows other readout architectures:



Cfr T. Kugathasan (NSS 2013)

Radiation tolerance sufficient for Alice,

expect much better if full depletion of the epitaxial layer would be reached

ALICE ITS UPGRADE PROJECT

- ALICE: Pixel sensor
  - ~ 100mV distributed over a few pixels
  - Could we get to digital signal by further optimization (almost fully eliminating power consumption)?
- Analog front end design: 40nW*250 000 pixels = 10 mW/cm^2
- Digital: looking at solution with similar power consumption
- If analog front end – architecture combination successful, power for data transmission off-chip may very well be dominant

Trying to approach strip level power consumption per unit area and definitely stay below 100mW/cm^2

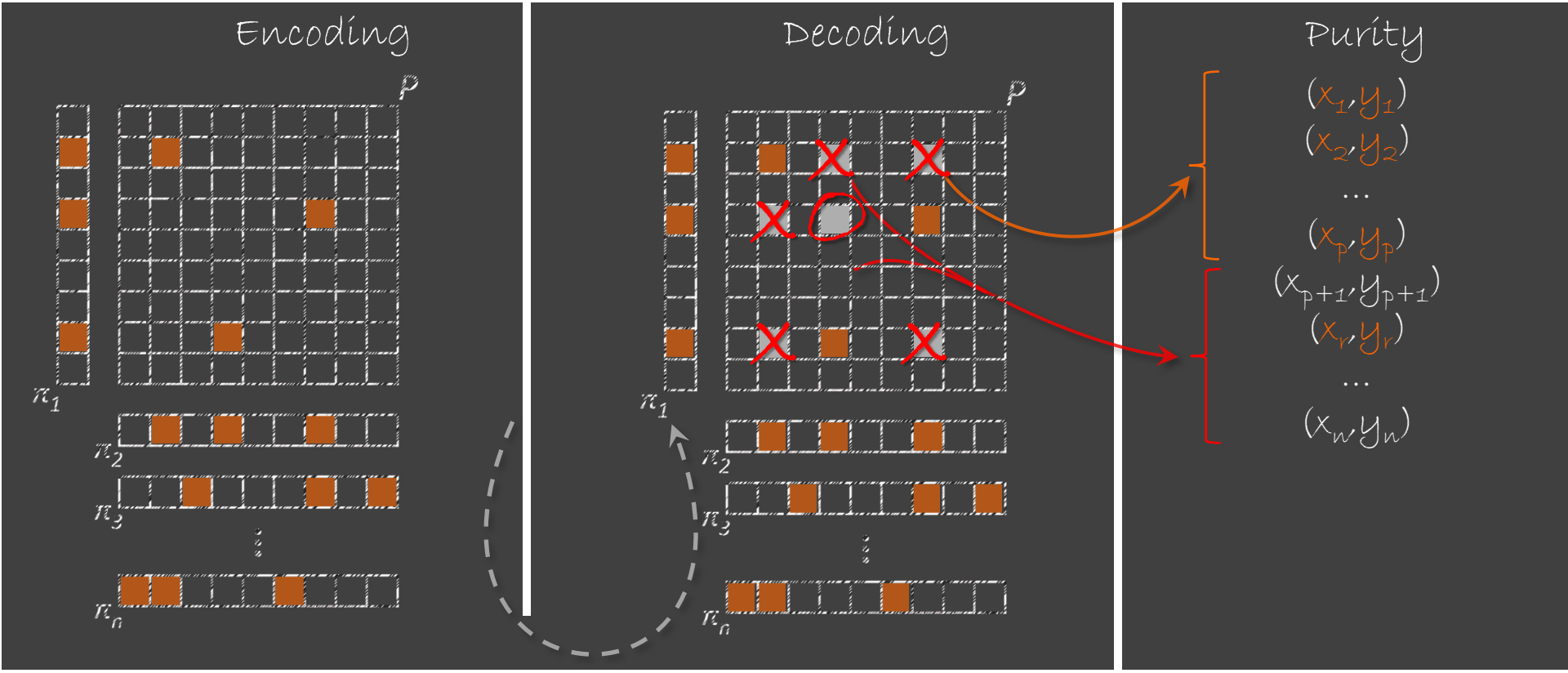
- Radiation tolerance sufficient for Alice, expect much better if full depletion of the epitaxial layer would be reached

ARCHITECTURE FOR SIMPLE IN-PIXEL CIRCUIT

P. Giubilato Pixel 2012 : Orthopix

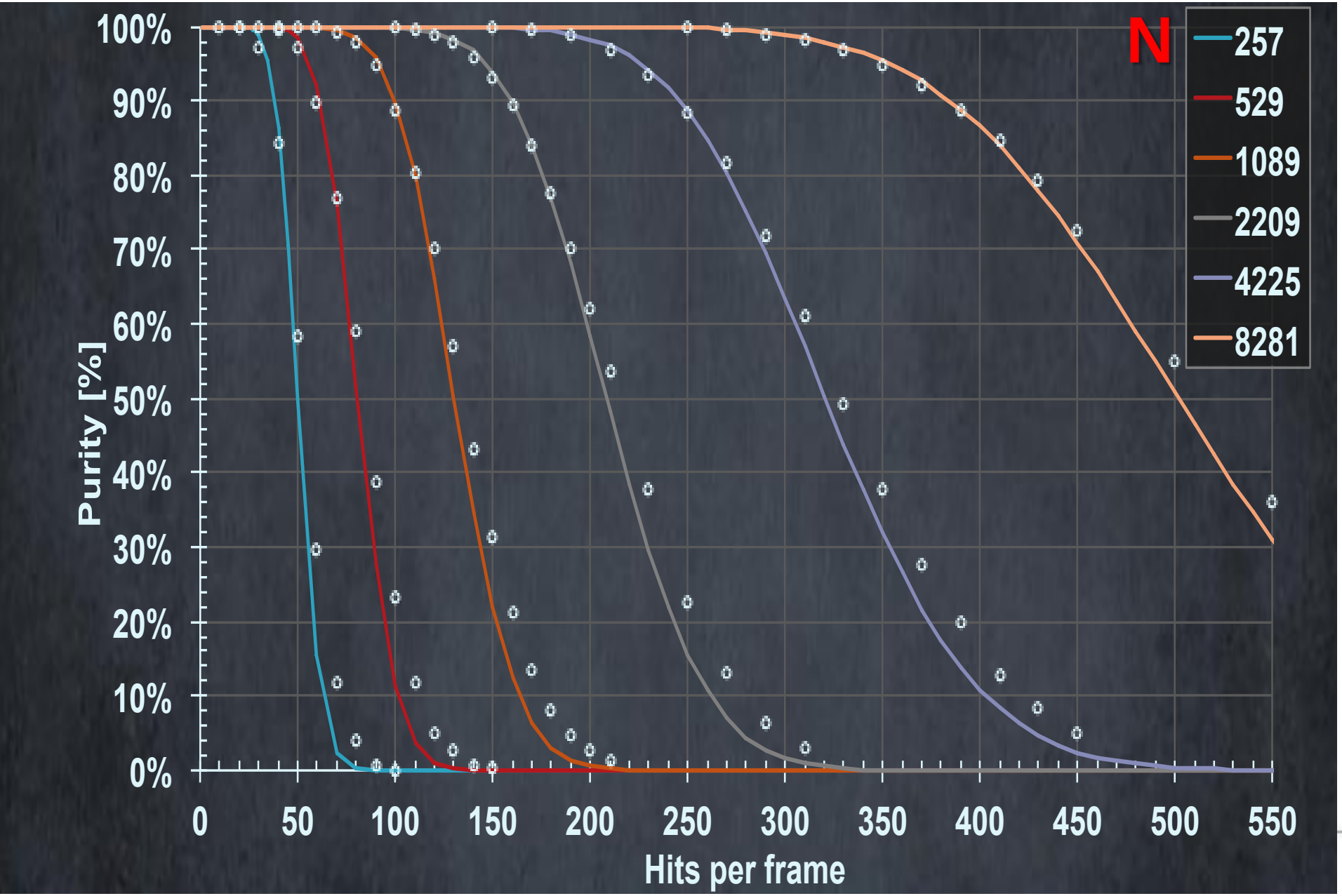
Reduce number of signals using projections (also reduce power that way !)

Minimize ambiguities by requiring orthogonal projections



For 4 projections reduction from N^2 to 4N

PURITY OF RECONSTRUCTION



CONCLUSIONS

- Monolithic detectors have revolutionized imaging in general
- High Energy Physics requires:
  - Radiation tolerance of circuit and sensor, need thin sensors and charge collection by drift
  - 100% efficiency, often more complex in-pixel circuit
  - Low power consumption => low C, or small collection electrode
- Combining complex in-pixel circuitry and radiation tolerance to extreme levels still a challenge in commercial processes, but progress is being made
  - All in nwell: simple in-pixel circuit otherwise higher C
  - Junction on the front: simple in-pixel circuit otherwise full depletion difficult or high C
  - Junction on the back: back side processing
  - SOI: radiation tolerance
- Special architectures could provide a way out

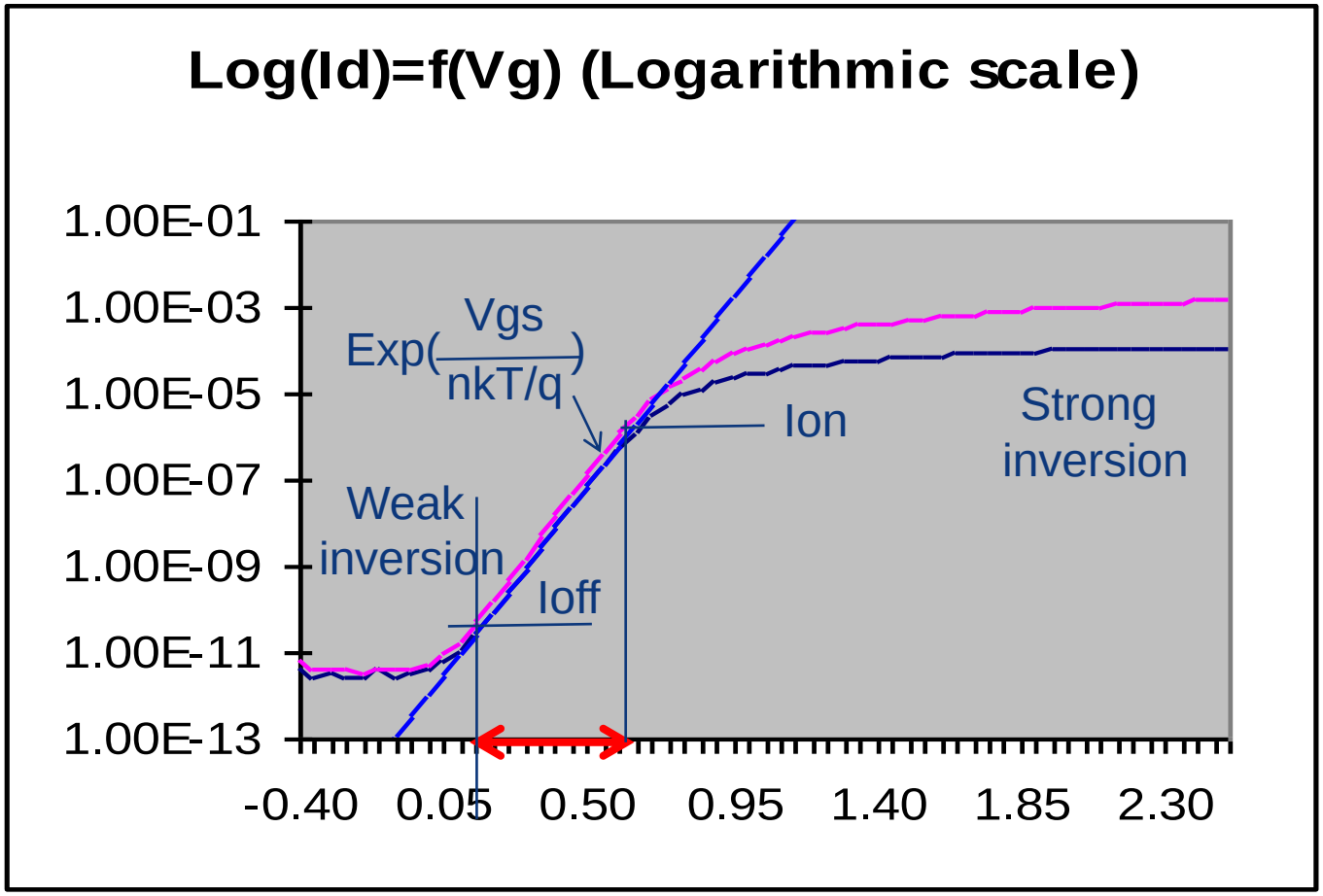
CONCLUSIONS

- Low power consumption
  - Analog : low Q/C essential
  - Digital : architecture and small cluster size
  - Data transmission off-chip or off-detector may very well be dominant

- Monolithic detectors slowly make their way in HEP

- Have not mentioned SPADs, CCDs, and some other developments

DIGITAL SIGNAL by further optimization ?



Slope in weak inversion 60-90 mV/decade,

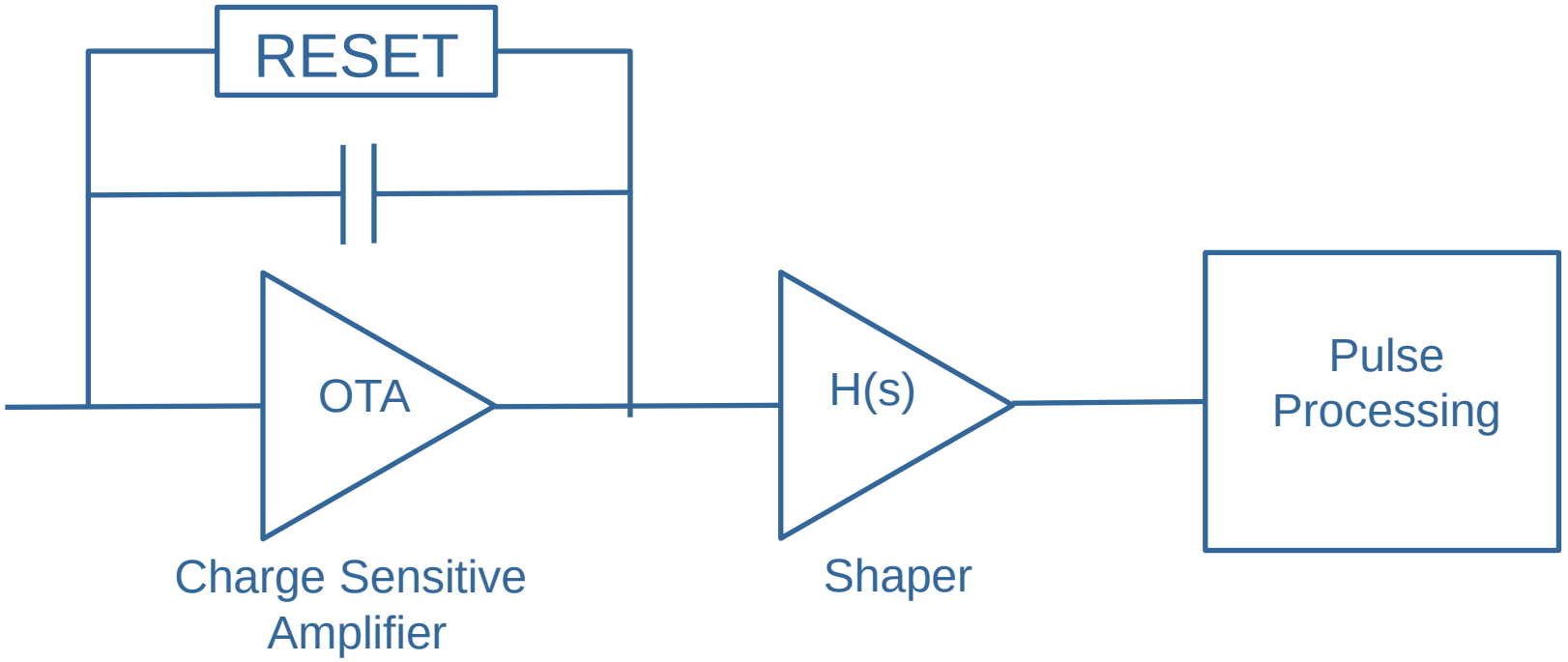
for Ion/Ioff=10^4 on a single pixel => 250-360mV

Would practically eliminate analog power consumption

THANK YOU !

BACKUP SLIDES

STANDARD PULSE PROCESSING FRONT END



ENC: total integrated noise at the output of the pulse shaper with respect to the output signal which would be produced by an input signal of 1 electron. The units normally used are rms electrons.

RESET: switch or high valve resistive element

ANALOG POWER

‘standard’ front end noise equations

$$ENC_{TOT}^2 = ENC_d^2 + ENC_f^2 + ENC_0^2$$

where

Transconductance gm related to power consumption

thermal

$$ENC_d^2 = \frac{4\gamma kTC_t^2}{gmq^2\tau_s}.X(n) \qquad X(n) = \frac{B(\frac{3}{2}, n-\frac{1}{2})n}{4\pi}\left(\frac{n!^2\, e^{2n}}{n^{2n}}\right)$$

1/fnoise

$$ENC_f^2 = \frac{KF_F}{C_{ox}^2 WL}\frac{C_t^2}{q^2}.Y(n) \qquad Y(n) = \frac{1}{2n}\left(\frac{n!^2\, e^{2n}}{n^{2n}}\right)$$

shot noise

$$ENC_o^2 = \frac{2qI_o\tau_s}{q^2}.Z(n) \qquad Z(n) = \frac{B(\frac{1}{2}, n+\frac{1}{2})}{4\pi n}\left(\frac{n!^2\, e^{2n}}{n^{2n}}\right)$$

INFLUENCE OF SHAPER ORDER n

n	1.00	2.00	3.00	4.00	5.00	6.00	7.00
X(n)	0.92	0.85	0.95	1.00	1.11	1.17	1.28
Y(n)	3.70	3.41	3.32	3.28	3.25	3.23	3.22
Z(n)	0.92	0.63	0.52	0.45	0.40	0.36	0.34

- Ref.: Z.Y. Chang and W.M.C. Sansen : ISBN 0-7923-9096-2, Kluwer Academic Publishers, 1991
- Ref. 2 : V. Radeka “Low-noise techniques in detectors” Ann. Rev. Nucl. Sci. 1988, 38, 217-77
- Ref. 3 : E. Nygard et al. NIM A 301 (1991) 506-516