

Scribe-Cleave-Passivate (SCP) Slim Edge Technology



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with

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Acknowledgements:

*1) Technical Guidance and Support by
Marc Christophersen*, Bernard F. Philips**

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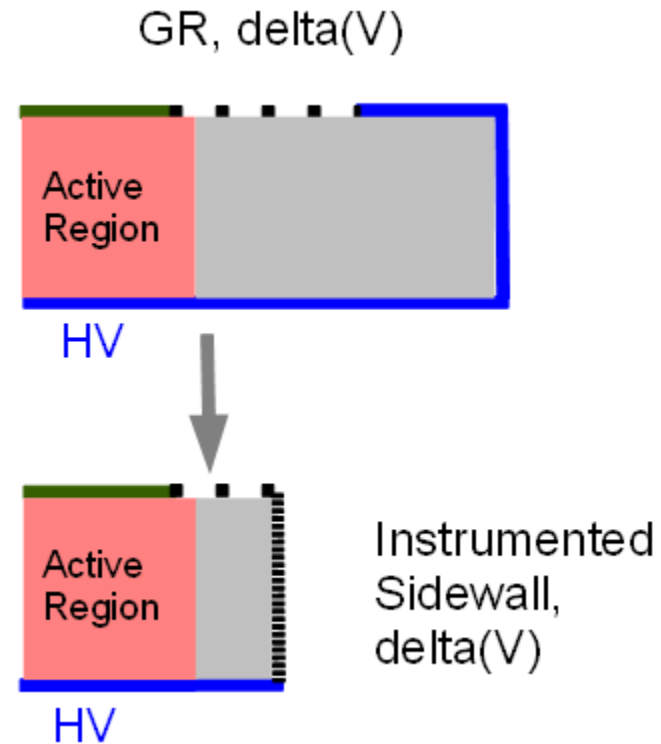
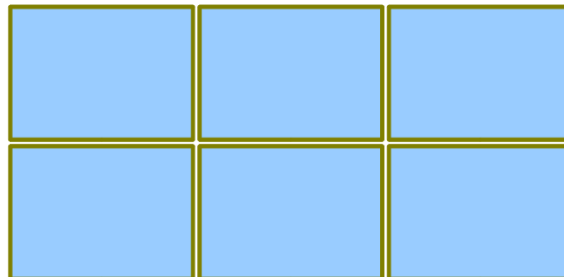
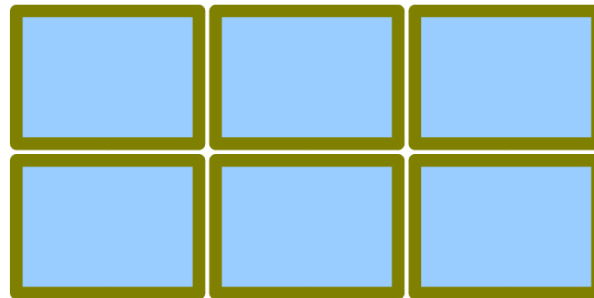
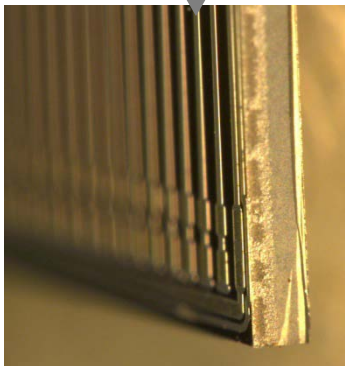
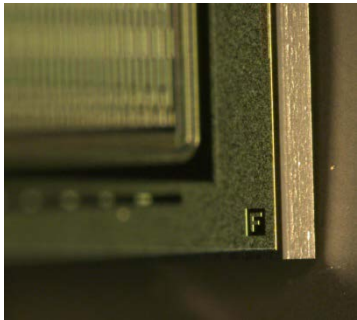
2) Our numerous collaborators from ATLAS and RD50

Slim Edges -- Motivation



Basic Idea: To minimize ~1 mm wide inactive peripheral region. This is relevant for “tiling” (as opposed to “shingling”) of large-area detector composed of small sensors.

Method: To instrument the sidewall in a close proximity to active area, such that it's resistive.

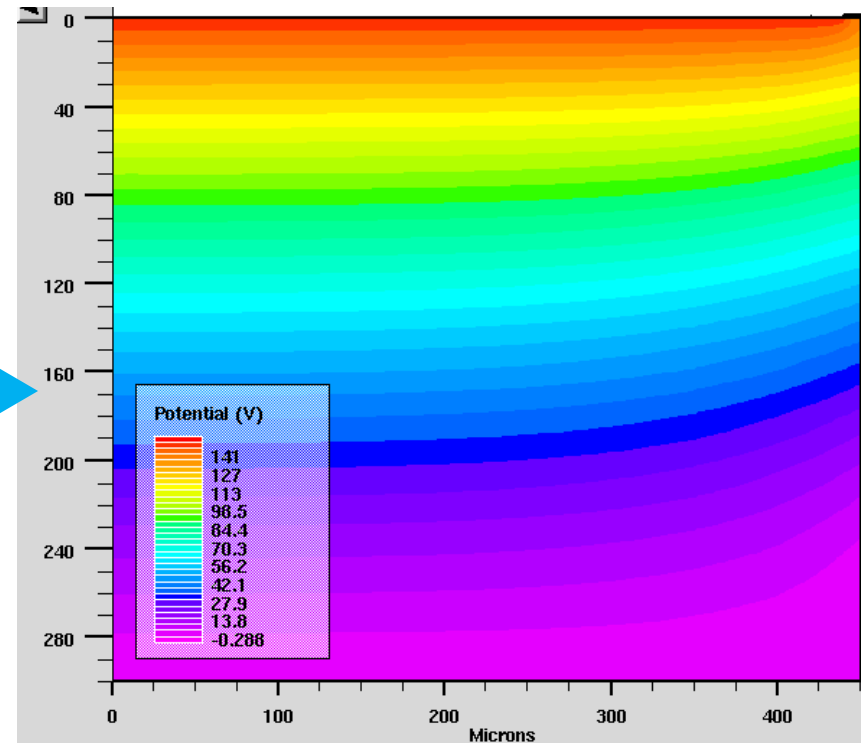
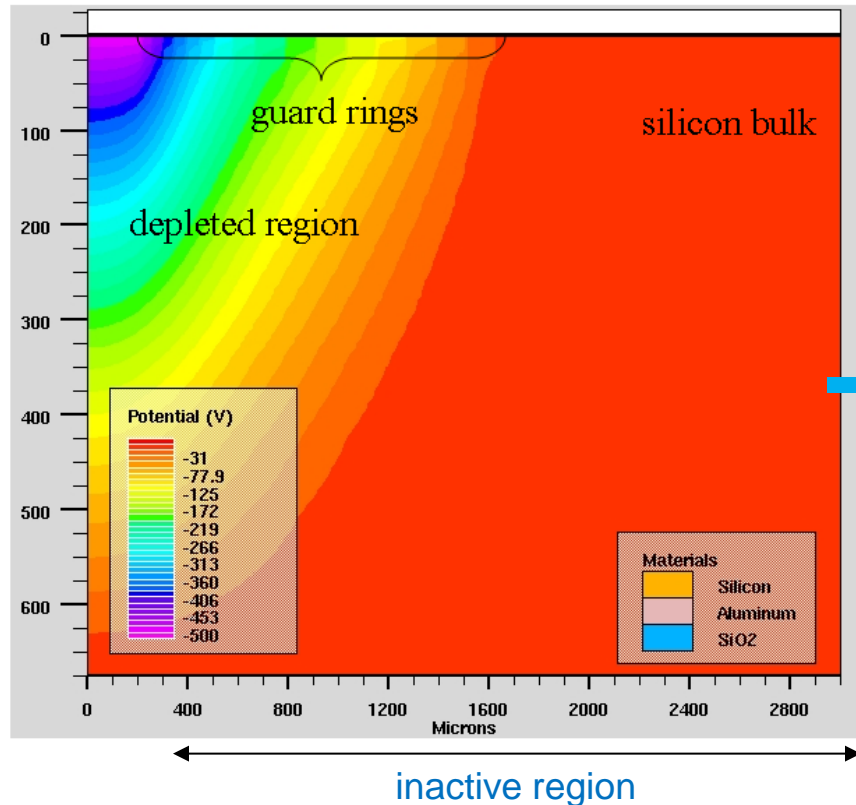


Slim Edges – Surface Quality



Conventional sensors have the bias voltage gradient in the guard rings region. To implement slim edges, we'd like to have the gradient on the sidewall => similar surface quality and passivation requirements.

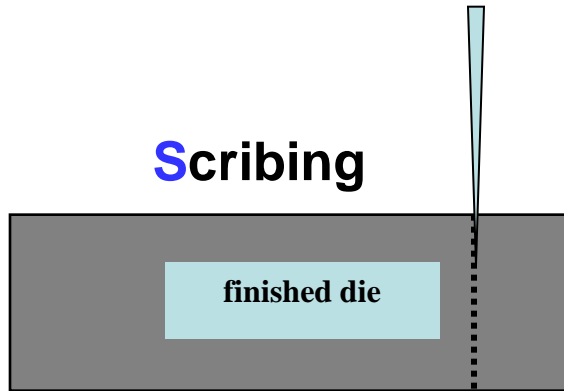
Surface imperfections lead to additional current consumption => IV test as a measure of performance.



Method -- SCP Treatment

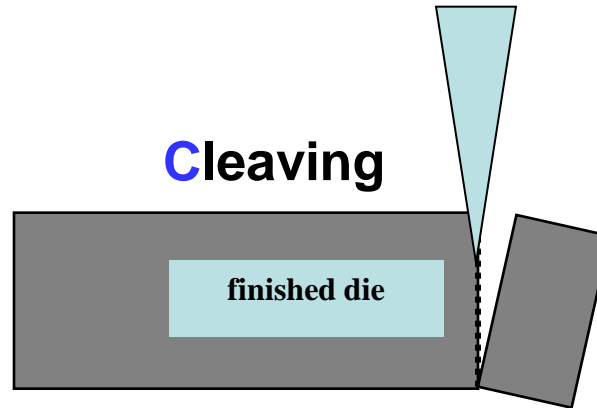


Scribing



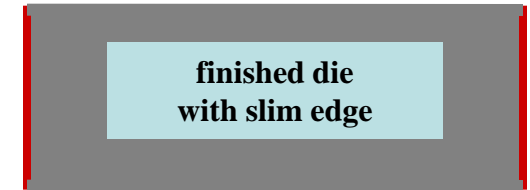
- Diamond stylus
- Laser
- XeF₂ Etch
- DRIE Etch
- Saw cut
(with cleanup step)

Cleaving



- Tweezers (manual)
- Loomis Industries, LSD-100
- Dynatex, GTS-150

Passivation



Native Oxide
+ Radiation
or:

N-type
($Q_f > 0$)

P-type
($Q_f < 0$)

- Native SiO₂ + UV light or high T
- ALD of Al₂O₃
- PECVD SiO₂
- PECVD Si₃N₄
- ALD “nanostack” of SiO₂ and Al₂O₃

All Treatment is post-processing & low-temp
(Etch-scribing can be done during fabrication)

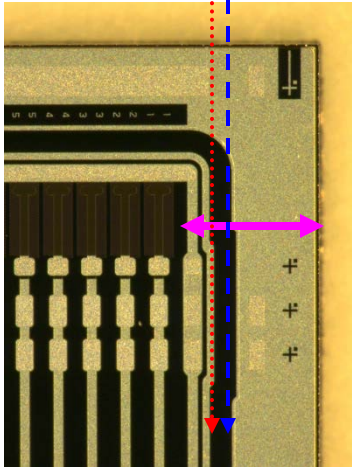
Basic requirement: 100 wafers (for rectangular side cleaving) with reasonably good alignment between sensor and lattice.

Examples with N-type Sensors

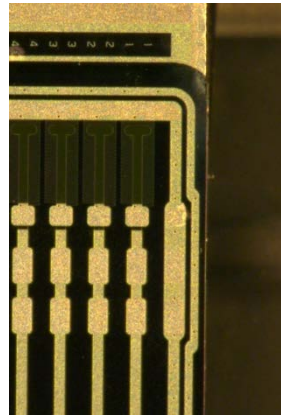


XeF2 scribing + Nitride PECVD

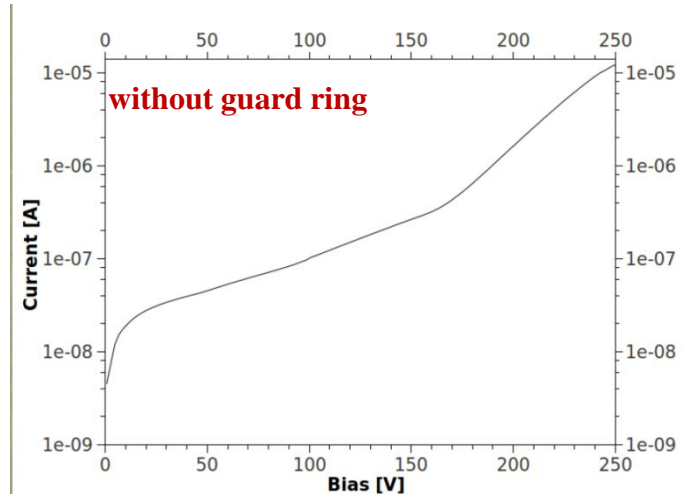
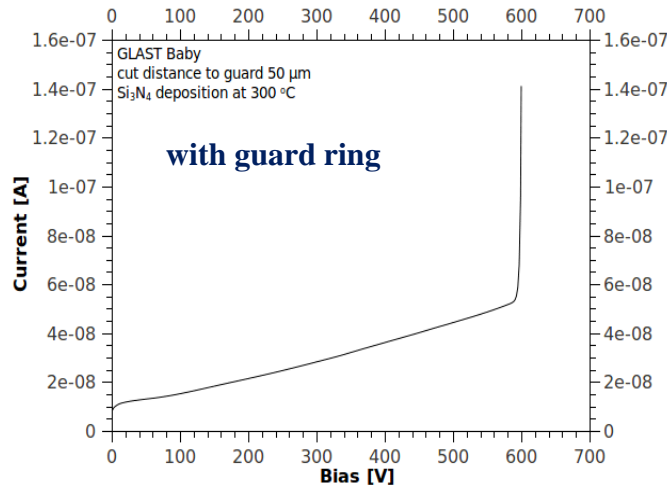
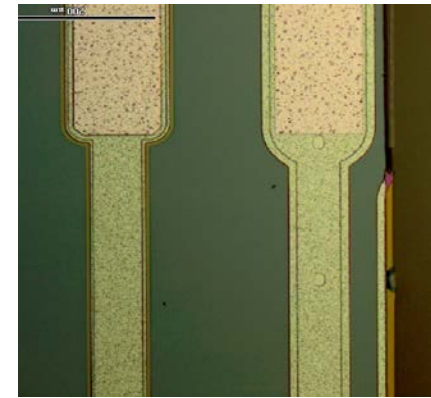
Si SSD with
900 μ m dead edge



Cut within 50 μ m
of Guard Ring



Guard Ring Cut (!)
0 μ m to Guard Ring



RD50 Activity Matrix



SCP originated as a part of ATLAS PPS project. It also became an RD50 project.
Ongoing Activities within RD50 Collaboration:

Institute	Contact Person	Sensors	Status
CNM Barcelona	G. Pellegrini	3D diodes, strips, pixels	2 nd round of tests (FEI3 and FEI4 pixel)
FBK Trento	G.-F. Dalla Betta	3D diodes, strips	2 nd round of tests ongoing
MPI Muenchen	A. Macchiolo	P-type planar pixels	P-type strip devices sent; in progress
UNFN Bari	D. Creanza	N-type “SMART” detectors	First processed devices sent for evaluation; in progress
Ljubljana U.	G. Kramberger	P- and N- type	Devices sent; used in laser TCT studies of the field profile
Glasgow U.	R. Bates	P- and N- type	Sensors with SCP used in a precision X-ray scan of charge collection efficiency
TU Dortmund	T. Wittig	IBL-style n-on-n sensors	Initial tests done, Iterations with IBL sensors
Vilnius U.	J. Vaitkus	P- and N-type for passivation quality studies.	P- and N-type diodes sent; irradiated p-type strip devices to be sent.

Current Efforts



We had a lot of technical development, with different fabrication options explored. For details, see recent publications:

- M. Christophersen et al., "Alumina and Silicon Oxide/Nitride Sidewall Passivation for P- and N-Type Sensors", NIM A 699 (2013) 14
- M. Christophersen et al, "The effect of different dicing methods on the leakage currents of n-type silicon diodes and strip sensors", Solid-State Electronics 81 (2013) 8.
- M. Christophersen et al, "Scribing-Cleaving-Passivation for High Energy Physics Silicon Sensors", Proceedings of Science, accepted for publication.
- V. Fadeyev et al, "Scribe-cleave-passivate (SCP) slim edge technology for silicon sensors", NIM A (2013) – in press. DOI: <http://dx.doi.org/10.1016/j.nima.2013.03.046>

Recent work is focused on:

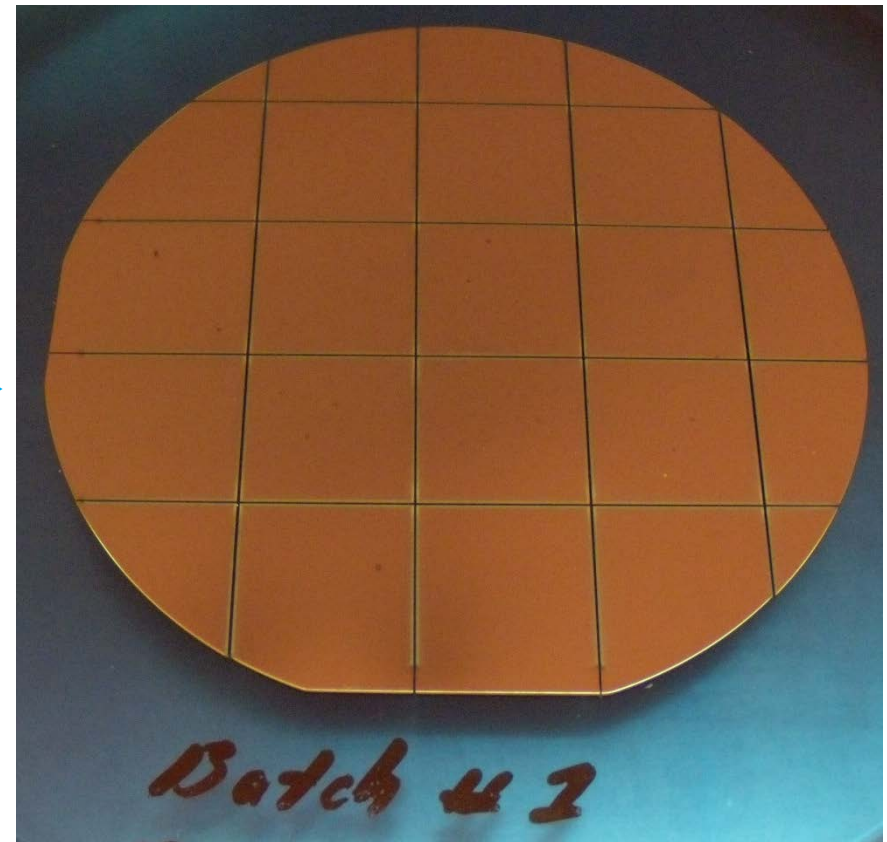
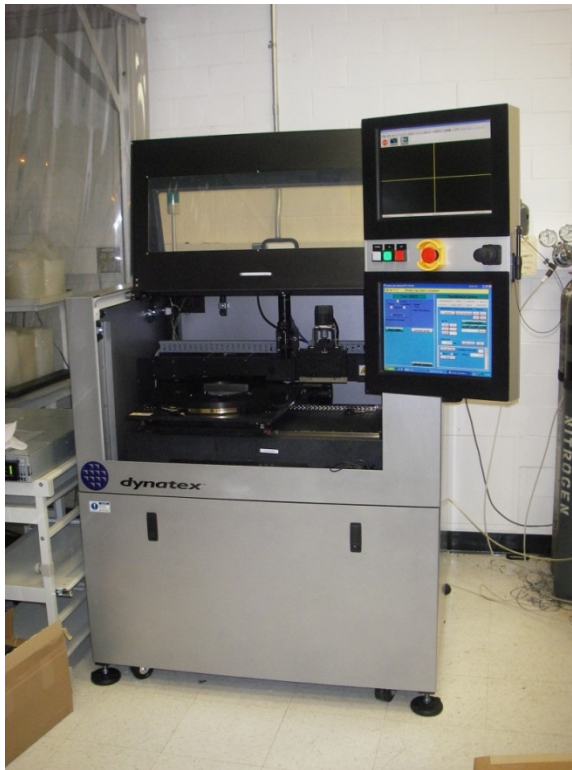
- Technical development:
 - Wafer-level processing
- Device performance:
 - CCE near the edge
 - Radiation hardness

Wafer-based Processing



A lot of processing steps are easily amenable to automation due to processing technology/machines. A key manual step we used so far is cleaving. It was done manually, with 2 tweezers.

In parallel with making and evaluating test samples, we explored machine-based cleaving options for mass-production.



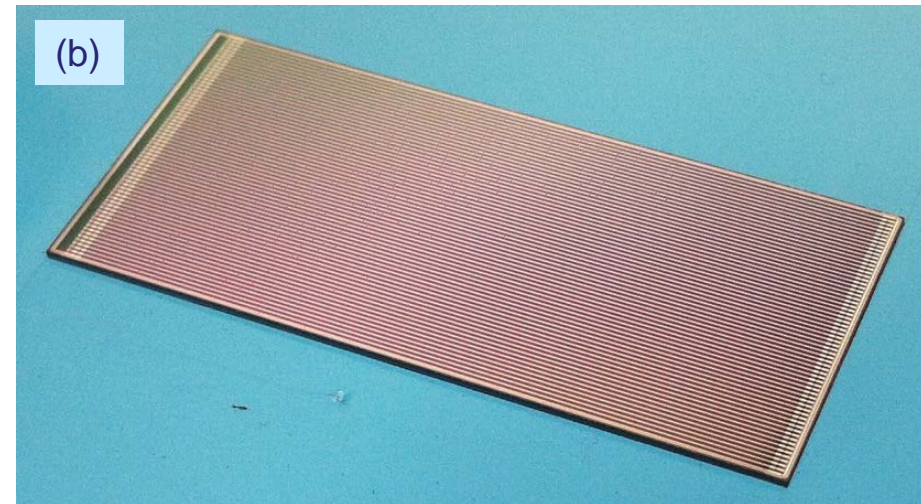
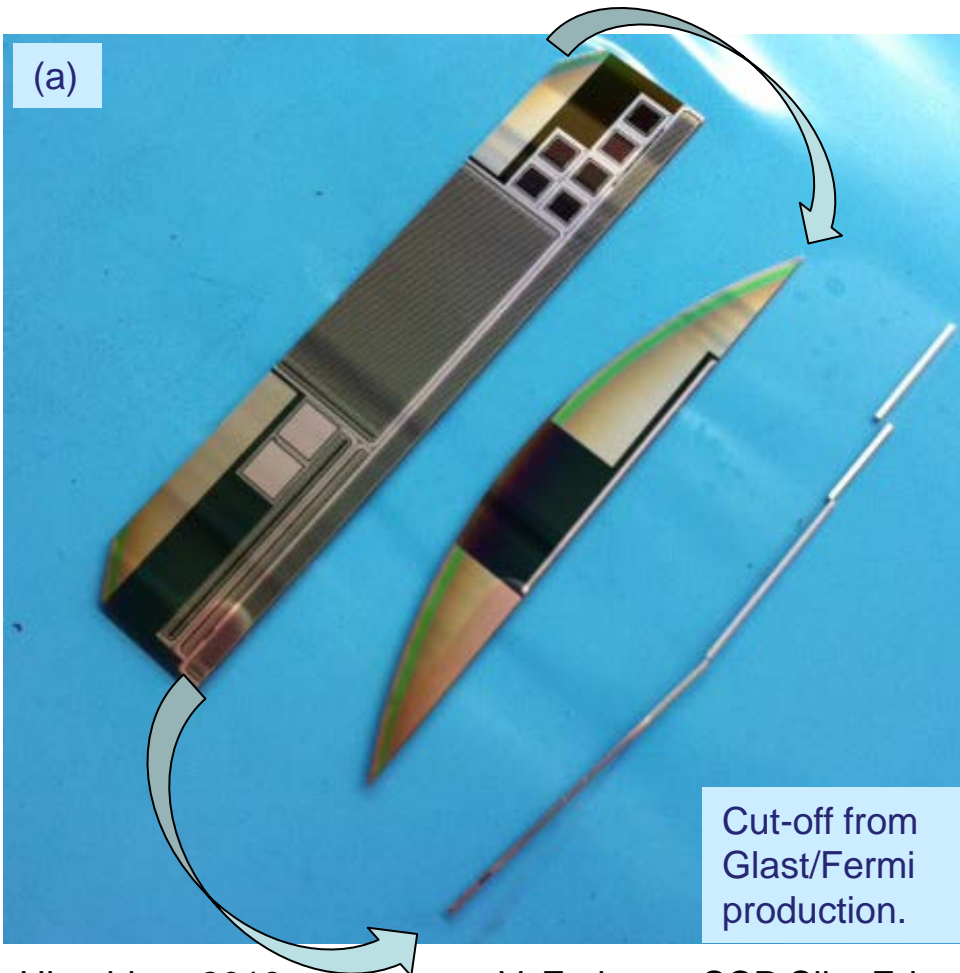
4-inch wafer broken along the scribe lines in a test.

Wafer-based Processing



The latest tests with Dynatex machine are extremely promising:

- a) 9-cm long narrow section is removed intact (it broke when being peeled off the blue tape). The removed piece is 680 μm wide and 400 μm thick!
- b) 1.6 x 3.5 cm^2 sensor with slim edges on all 4 sides.



Alternative Wafer Processing

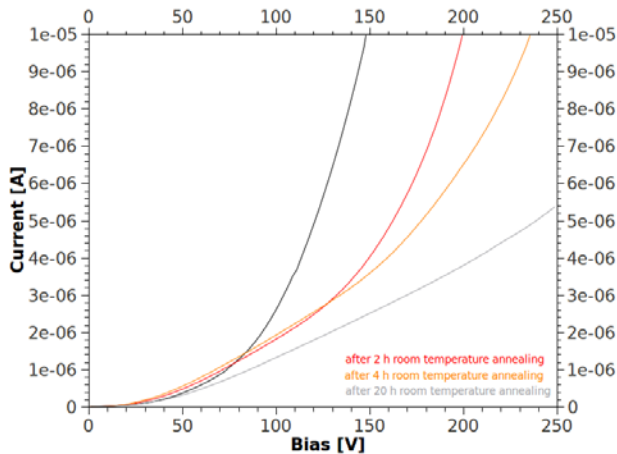
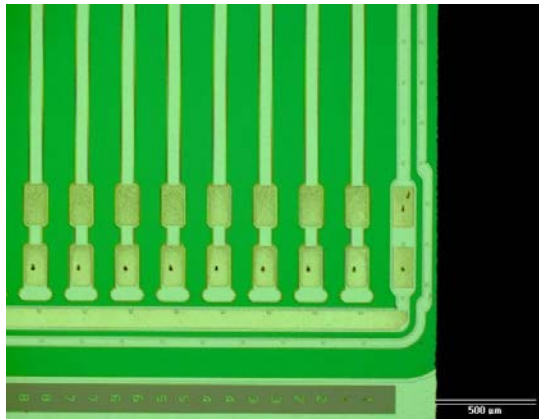


Based on our studies, wafer cleaving provides the best performance due to low defect density on the sidewall. Nonetheless, a process modification is possible:

instead of **Scribe-Cleave-Passivate**,
one can do **Cut-DamageRemoval-Passivate**.

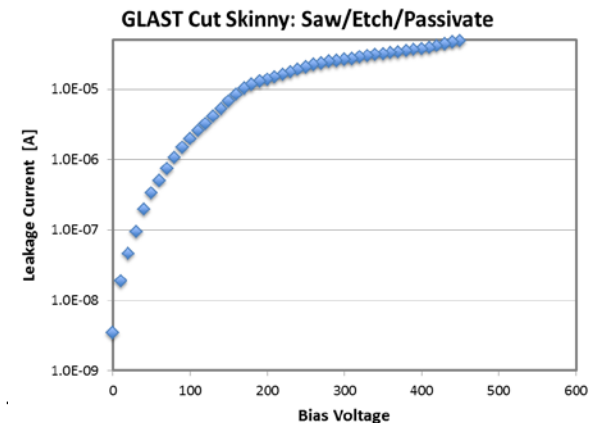
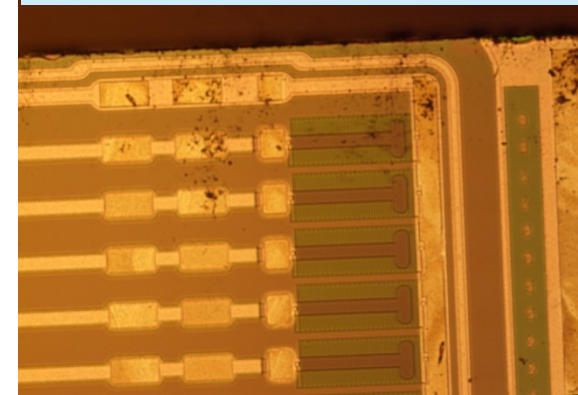
The cut here can be either laser through-cut or conventional saw cut.

This might insure reliability of the singulation process, at the price of possibly higher currents.
An option for difficult cases, e.g. with wrong lattice orientation.



NB: This process variation works for N-type sensors only, where XeF2 sidewall etch is compatible with passivation.

Post-processed by G. Pellegrini et al. at CNM



Charge Collection Testing



Sensor Type	Origin	Edge-Active area Distance [um]	Signal Readout	Beam	Ref
P-type strips	PPS (CIS)	~200	Binary (PTSM)	⁹⁰ Sr	V. Fadeyev <i>et al</i> Pixel 2012, NIM A in press
N-type strips	GLAST (HPK)	~200	Analog (ALiBaVa)	⁹⁰ Sr	R. Mori <i>et al.</i> 2012 JINST 7 P05002
P-type strips	PPS (CIS)	150	Analog (ALiBaVa)	Focused X-ray	R. Bates <i>et al.</i> , 2013 JINST 8 P01018
P-type 3D pixels	IBL (CNM)	50	FE-I3 & FE-I4	CERN Test Beam	S. Grinstein <i>et al.</i> , RESMDD12 G. Pellegrini <i>et al.</i> , Pixel 2012, NIM A in press
P-type strips	PPS (CIS)		Analog (ALiBaVa)	⁹⁰ Sr	

In all cases charge collection on the edge was within few % of other electrodes
 → Caveat: all un-irradiated devices.

New developments:

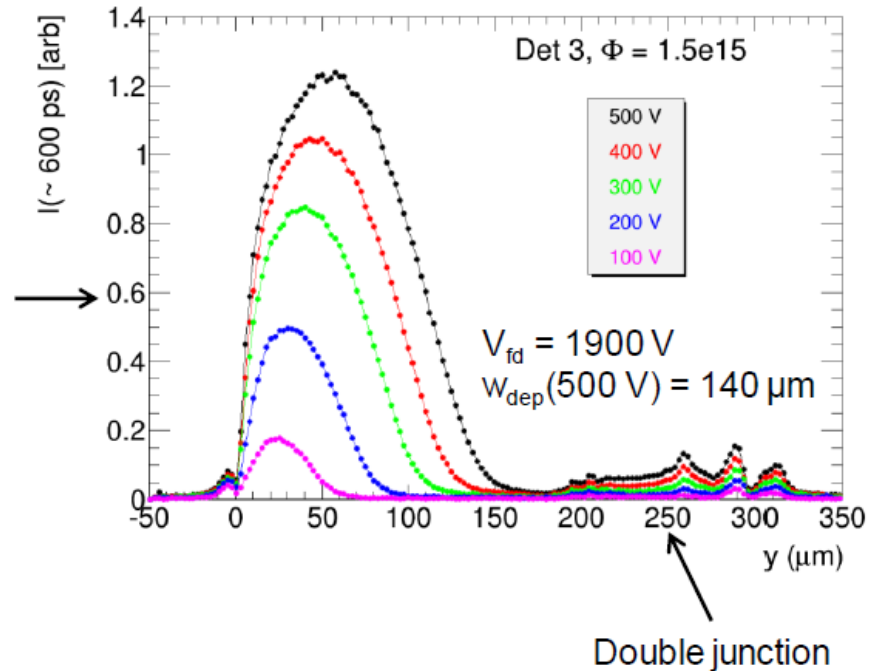
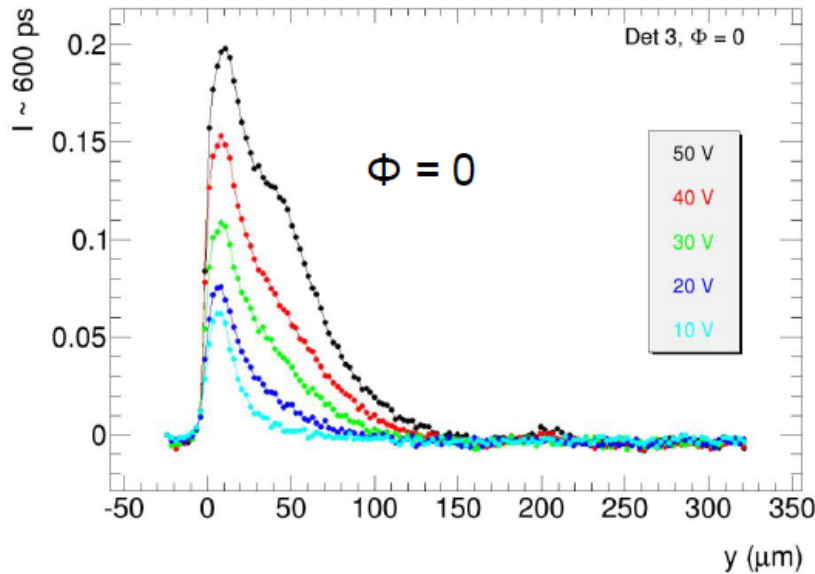
- MPI study has device irradiation in progress.
- Glasgow (R. Bates et al) are planning a follow up with irradiated devices.

Laser TCT Study of Neutron-Irradiated SCP Sensor



From I. Mandic's talk at 22nd RD50 Workshop:

Field profiles before and after irradiation



- depleted depth in planar diode: $w_{dep} = \sqrt{\frac{2\epsilon_0 V_{bias}}{e_0 |g_c \Phi_{eq}|}}$

- after irradiation to $1.5e15 \text{ E}$ field on the edge extends closer to value of w_{dep}

2010 Proton Irradiation Studies @LANL



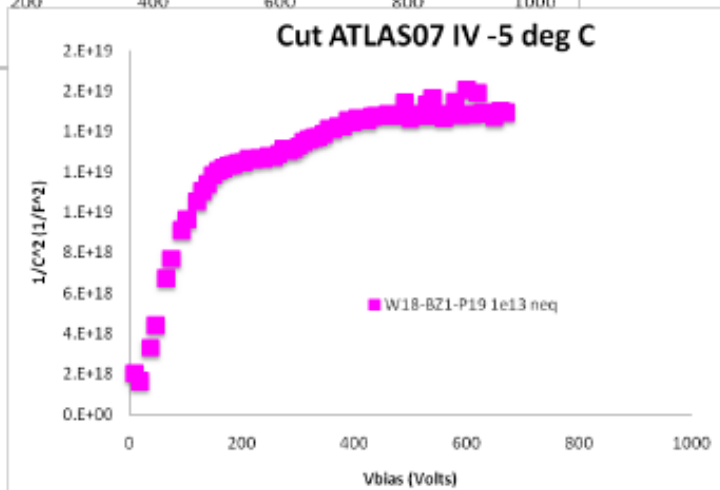
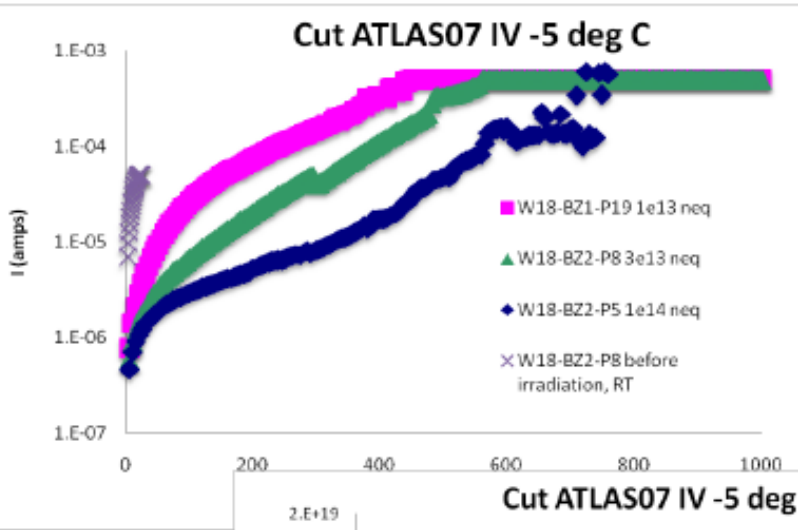
P-type “SC only”: No Passivation

P-type HPK (ATLAS07)

These sensors did not work after cleaving (initial trial without sidewall passivation). Breakdown at ~few Volts. There is an empirical evidence that the breakdown improves after irradiation.

We put these sensors in proton beam to see if they would indeed improve.

Leakage is initially dominated by the edge current, which is *reduced* with fluence. At 10^{14} neq, $I(\text{edge}) < I(\text{bulk})$.

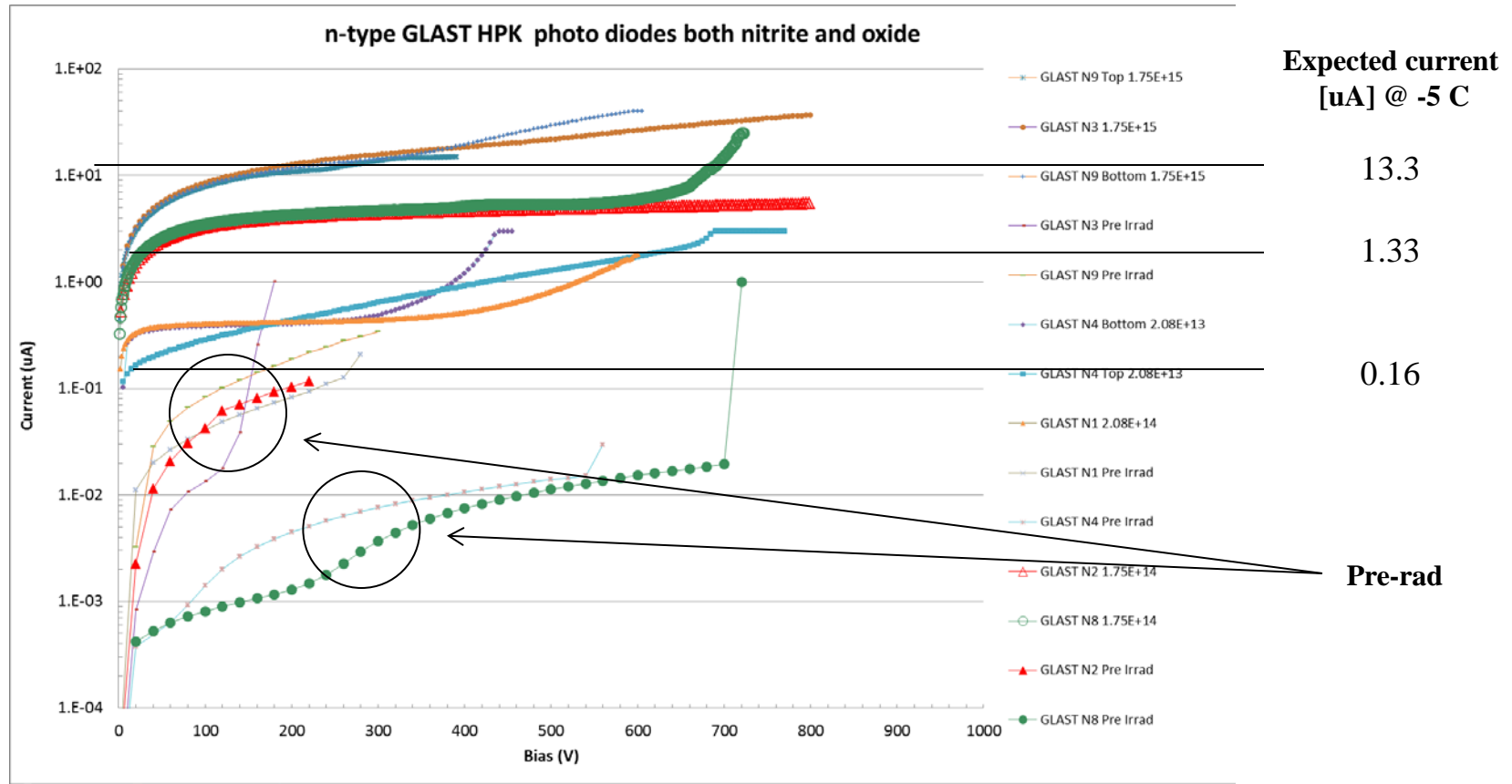


Comparison of expected and observed currents at 200 V

Area [cm ²]	1		
Alpha	4.00E-17		
Thickness [cm]	0.03		
T factor	16		
Irradiation	1.00E+13	3.00E+13	1.00E+14
I_expect (200V)	7.50E-07	2.25E-06	7.50E-06
I_observe(200V)	7.39E-05	2.02E-05	5.16E-06
observe/expect	98.57	8.99	0.69

Observation on “SC only” P-type:
High fluence irradiation -> resistive edge!

N-type GLAST HPK Diodes with SCP 2012 CERN proton beam



Observations on N-type:

Low fluence ($1e13$, < inversion) edge isolation due to passivation (Nitrite/nanostack)

High fluence ($>1e14$, > inversion): resistive edge

...No dependence on type of passivation, leakage current close to bulk expectation

P-type CIS strip devices; 2011 Proton Irradiation @LANL

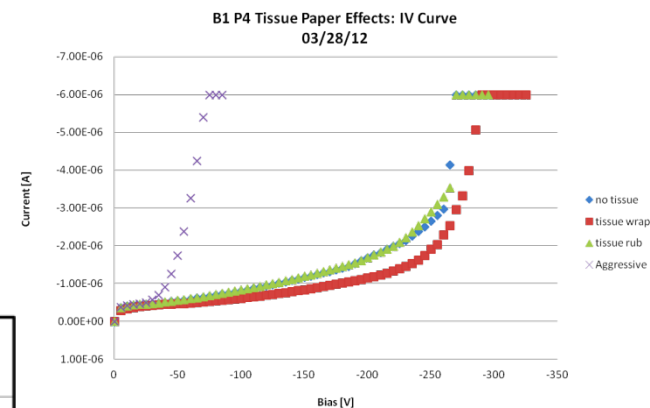


Irradiated 12 SCP processed p-type strip devices (CIS courtesy A. Macchiolo) at LANL (thanks S. Seidel). Results are in-conclusive:

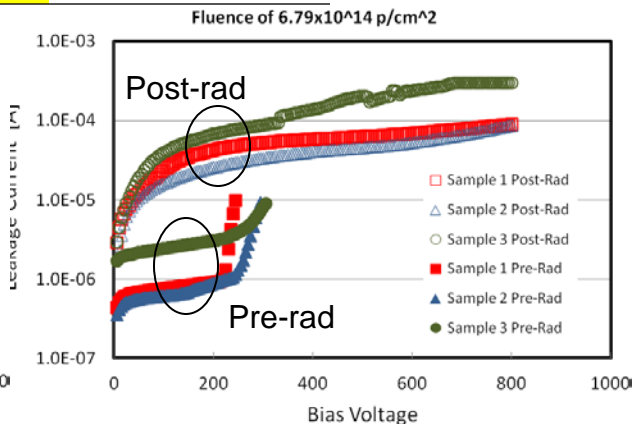
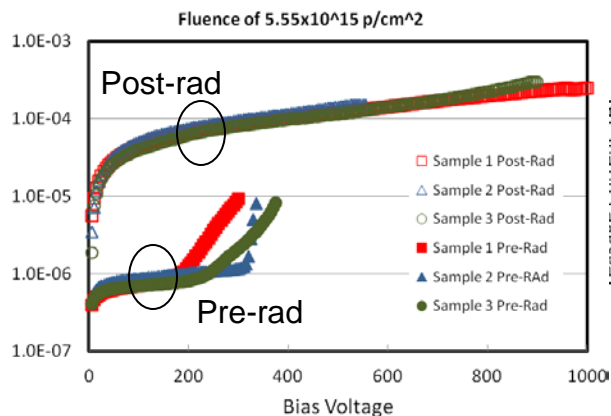
- + Breakdown voltages extended post-rad
- + High fluence devices (3/3 for $1e16\text{neq}$, 3/3 for $1e15\text{neq}$) show expected post-rad leakage current
- Lower fluence devices (1/3 for $1e13\text{neq}$ and 1/3 for $1e14\text{neq}$) show earlier breakdown!

Sensor	Before Irradiation		After Irradiation		Fluence	No Guard Rings
	V(break) at ~10 uA	V(break) at ~100 uA	V(break) at ~10 uA	V(break) at ~100 uA		
B1 P5		30		460	10^{13}	1
B1 P6		290		165	10^{13}	1
B2 P1		410		80	10^{13}	3
B1 P8		15		90	10^{14}	5
B2 P10		310		80	10^{14}	5
B2 P6		390		100	10^{14}	1
B2 P8		300		>800	10^{15}	4
B2 P9		310		335	10^{15}	5
B2 P11		250		>800	10^{15}	2
B2 P2		305		390	10^{16}	1
B2 P3		340		330	10^{16}	3
B2 P4		380		425	10^{16}	3

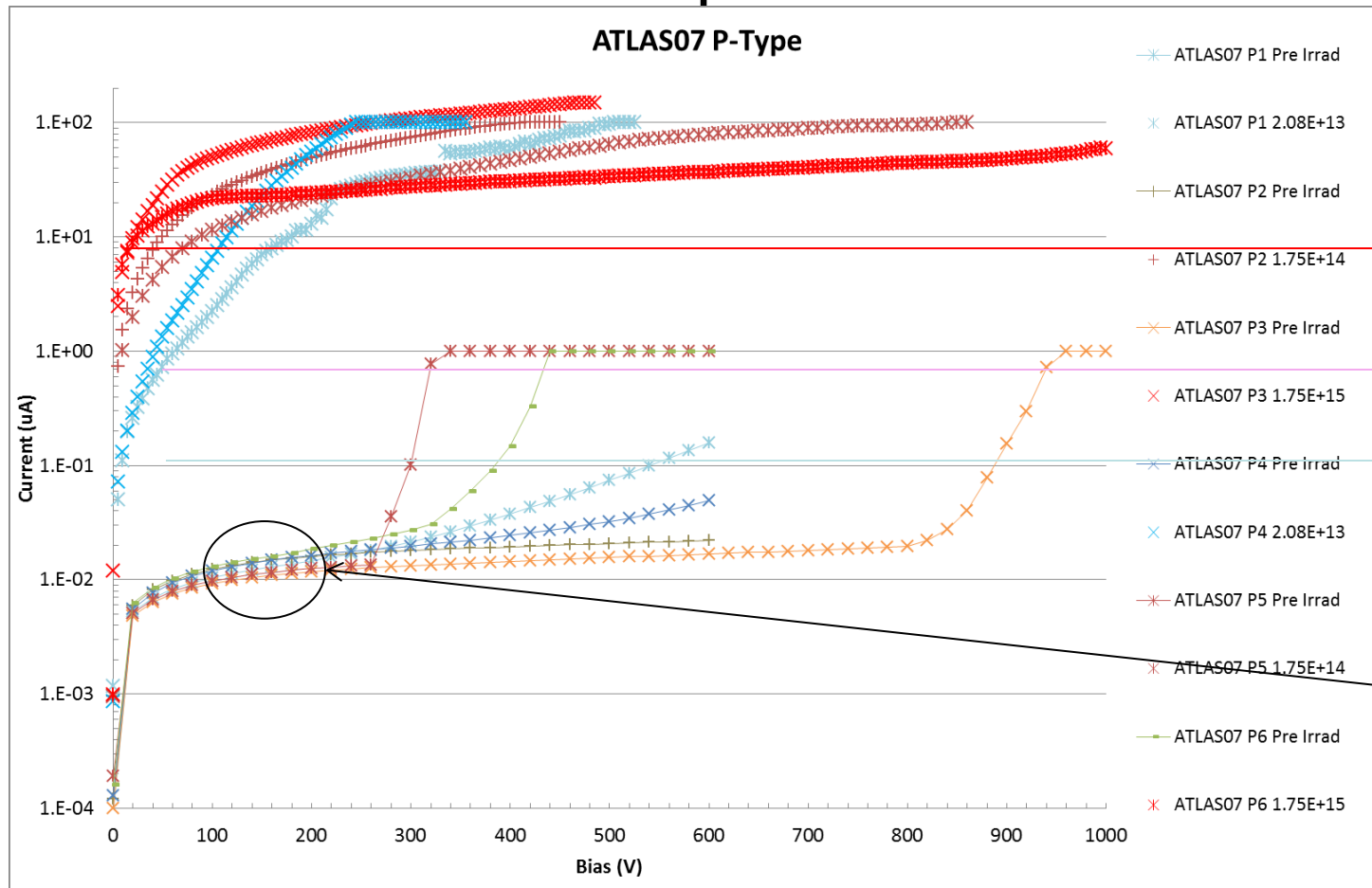
A parallel investigation of the robustness of the passivation layer revealed a possible susceptibility to rough handling. There is no proof that this has skewed the irradiation results.



... was followed up at CERN irradiation run in 2012 with protons. Results were similar, indicating either continuous packaging issues, or a real problem at low fluences.



P-type ATLAS07 HPK Diodes 2012 CERN proton beam



**Expected current
[uA] @ -5 C**

8

0.8

0.1

Pre-rad

Observation on SCP p-type:

Leakage currents do not scale with fluence

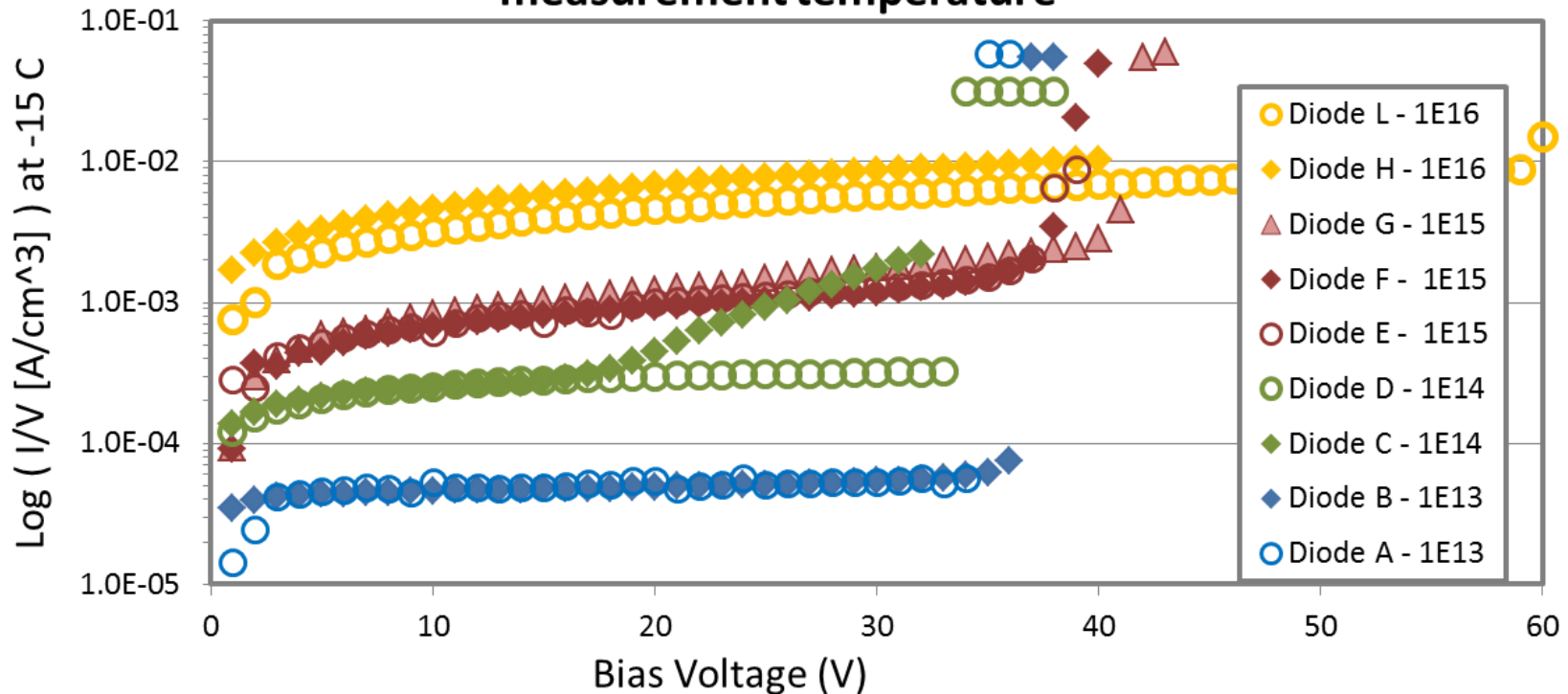
low fluence (< 1e14): reduced edge performance

high fluence (>1e14): resistive edge

P-type 3D sensors irradiated at Ljubljana, (PI G.-F. Dalla Betta)



3D Trento diodes scaled according to volume and
measurement temperature



Observation on SCP P-type with neutrons:

3D neutron-irradiate sensors show approximate scaling with fluences:

no high currents for low fluences !

=> See vastly different fluence scaling. Either due to field geometry or non-ionizing dose.

Conclusions and Future Work



- We are pursuing a method of making devices with reduced peripheral material (“slim edges”). This is an alternative to making “active edge” sensors, which typically requires very specialized processing.
- A lot of fabrication aspects are figured out. Currently focusing technical developments on wafer-level processing.
- The method rose a lot of interest in the community. We are collaborating with many RD50 groups on further development and application to their particular sensor designs.
- Sensor sensitivity near the edge:
 - Had multiple studies of CC near the edge on un-irradiated sensors. So far no issues.
 - Will be interesting to see results from irradiated devices: MPI and U. of Glasgow studies.
- Radiation hardness of the passivation:
 - N-type devices seem to be rad-hard. This is expected, since the properties of the sidewall after irradiation should be similar to the case of top surface on conventional sensors. (Same passivation, similar surface properties.)
 - There appears to be an issue with rad hardness on p-type devices for fluences $<10^{14}$ neq/cm².
 - This has to be related to properties of dielectric (alumina) after irradiation. There is a project, lead by G. Pellegrini (CNM) to fabricate MOS-like structures with alumina to find more details about it.
 - Studies of neutron-irradiated p-type 3D sensors are in progress. Preliminary data indicate no issues. This is either due to different field geometry or non-ionizing dose.

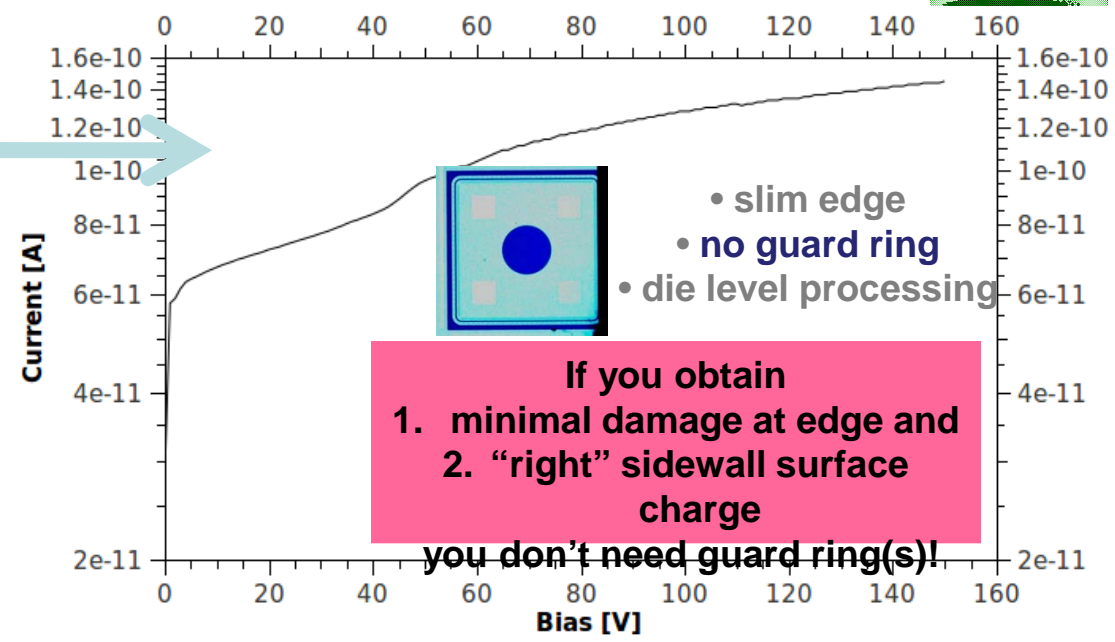
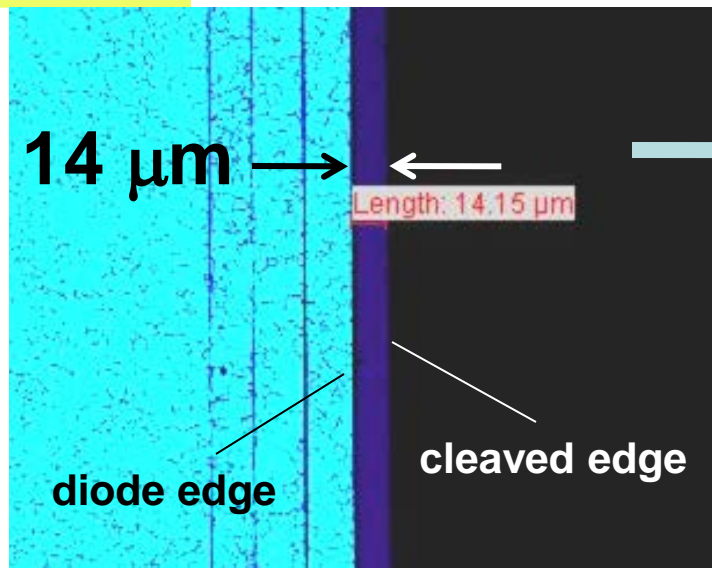


Back-Up Slides

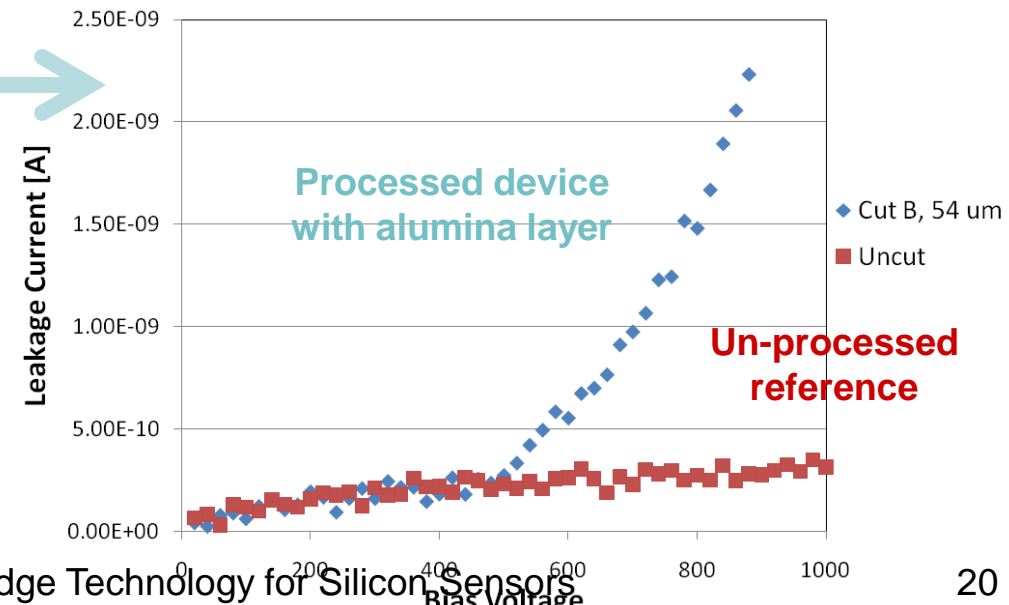
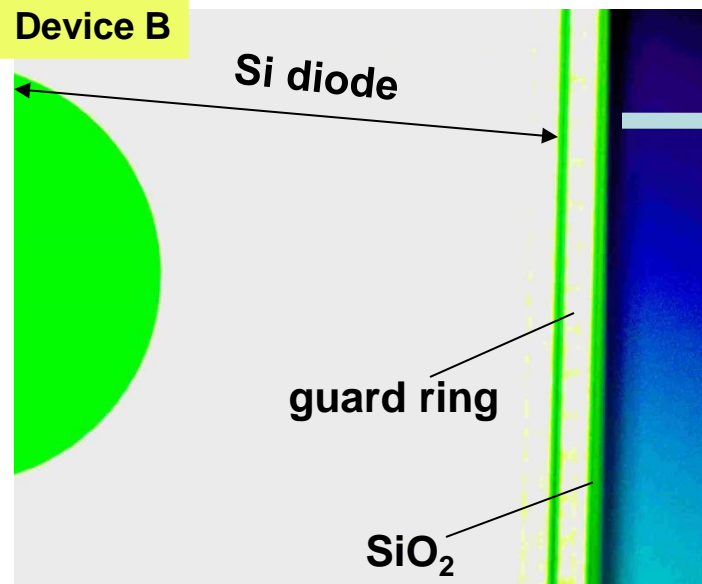
Examples with P-type Sensors



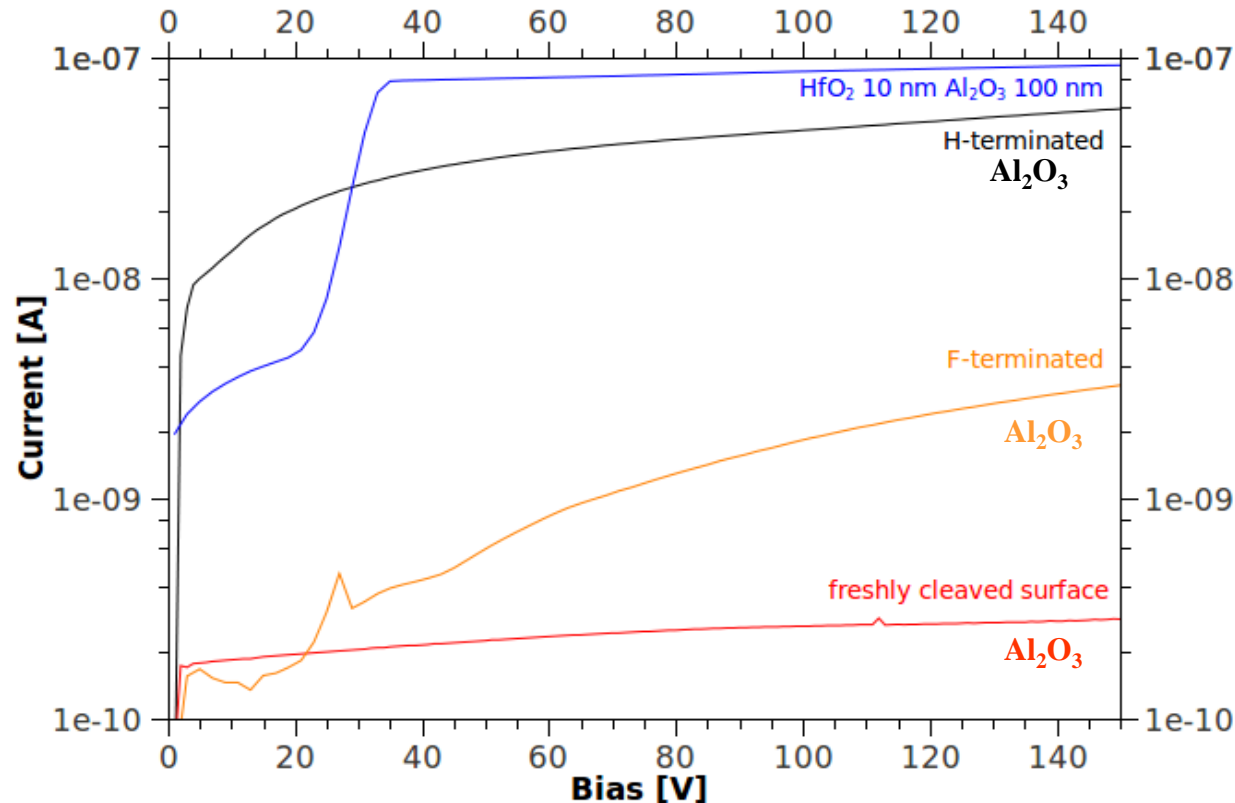
Device A



Device B



Effect of Surface Termination – P-Type Si



- After all the handling, we need to remove a native oxide. That is done w/ HF and leads to the “H-termination”, which can’t be passivated with alumina Al₂O₃.
- Need to convert the H-termination into F-termination which in combination with alumina ALD should work. Know their chemistry!
- The hunt for an ideal surface termination for p-type Si is still on.

Progress with Passivation (N-type Diodes)

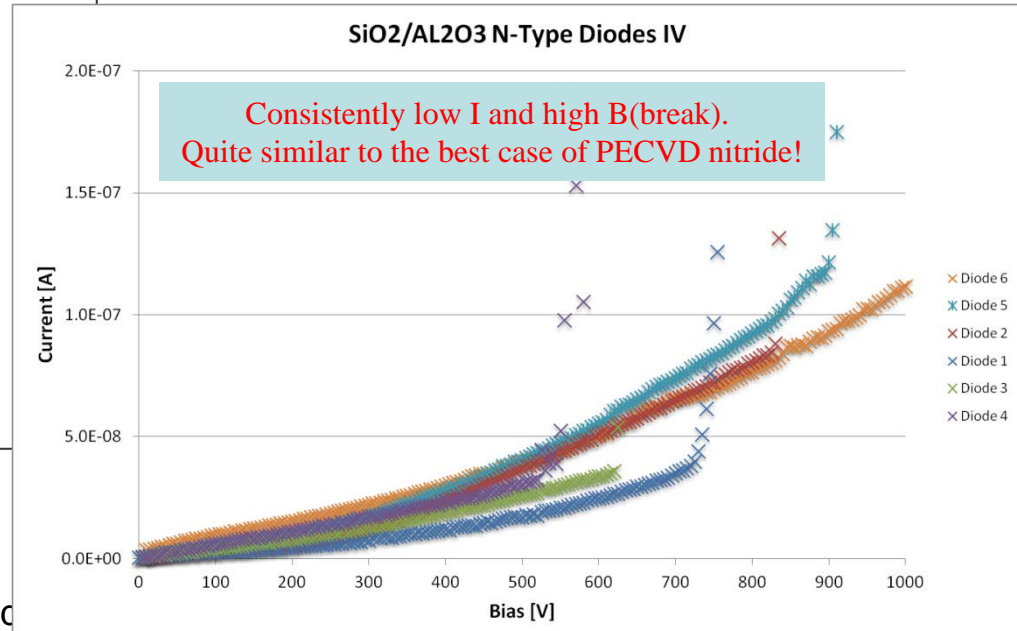
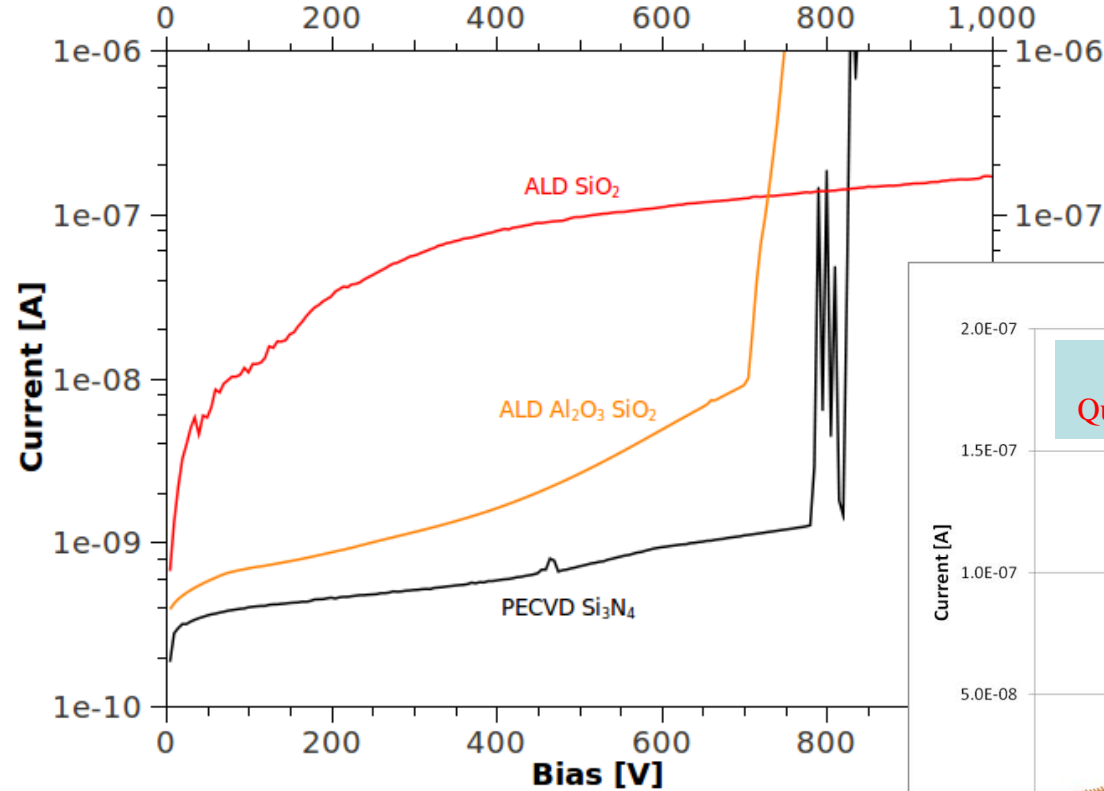


PECVD process has been developed by industry as a wafer process => Small height of the chamber in a typical machine.

This worked well for small size samples, that could be positioned vertically, or slanted. For large sensors this is not quite applicable => replace by ALD method.

Study with HPK Fermi/GLAST diodes. The plain ALD SiO₂ is worse than the best case of PECVD Si₃N₄.

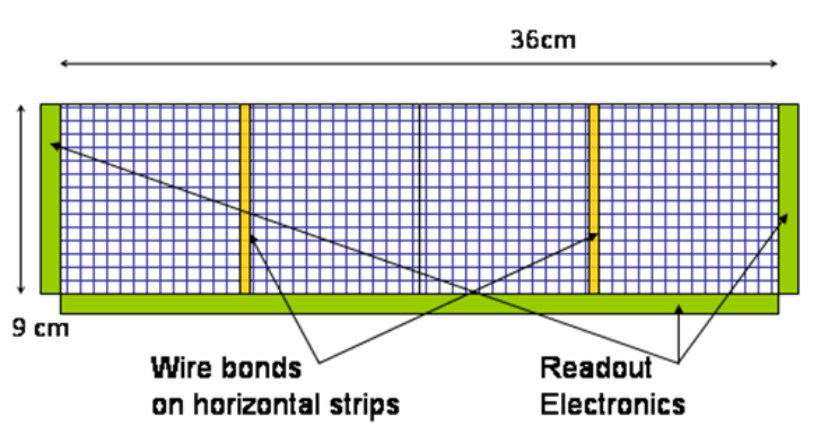
But a “nanostack” of ALD SiO₂ (10 nm) and Al₂O₃ (50 nm) works well. Parameters are from G. Dingemans et al, J. Appl. Phys. 110, 093715 (2011); doi: 10.1063/1.3658246



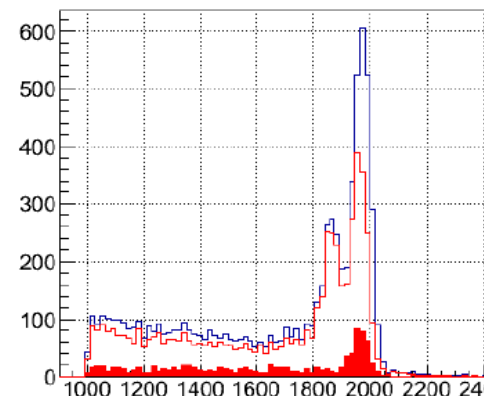
SCP-treated SSD in pCT Tracker



Large area coverage requires tiling of 4 sensors, having ~ 1mm inactive edges which create image artifacts.



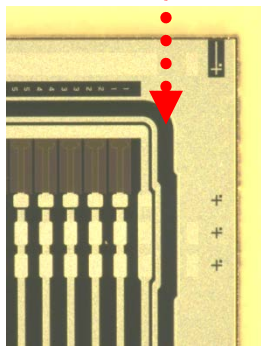
Overlapping sensors introduces artifacts requiring additional, non-uniform energy corrections



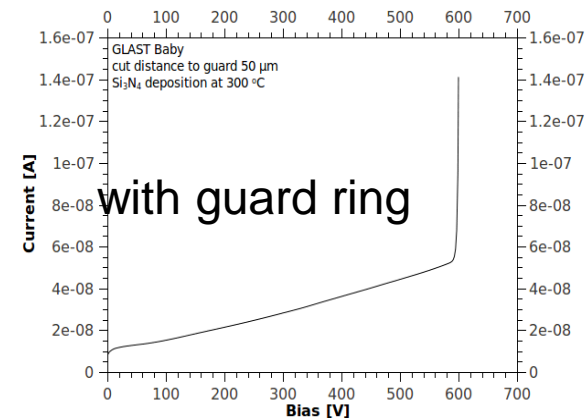
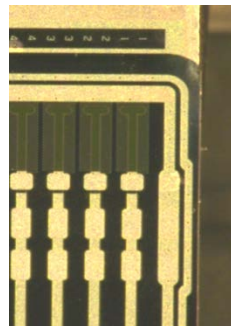
For Tiling with no Overlap: “Slim Edges”

Si SSD with 900 μ m dead edge

Cut within 50 μ m of Guard Ring



S-C-P:
Scribing (XeF_2)
+ Cleaving
+ Passivating (N_2 PECVD)



M. Christophersen et al.,
SSE 81, (2013) 8–12