Development of a High Counting Rate ASIC for Heavy-ion Beam Monitoring

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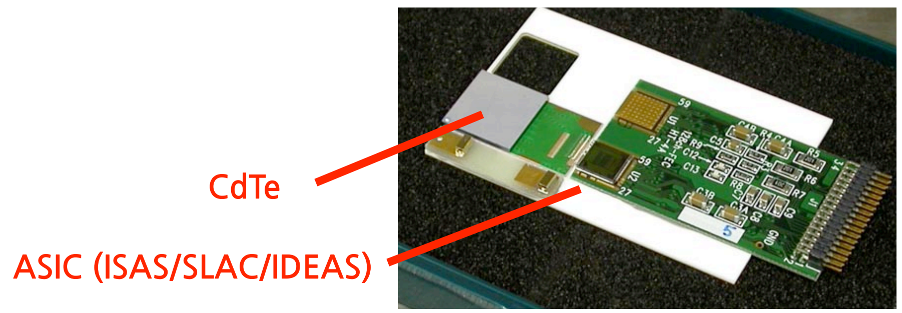
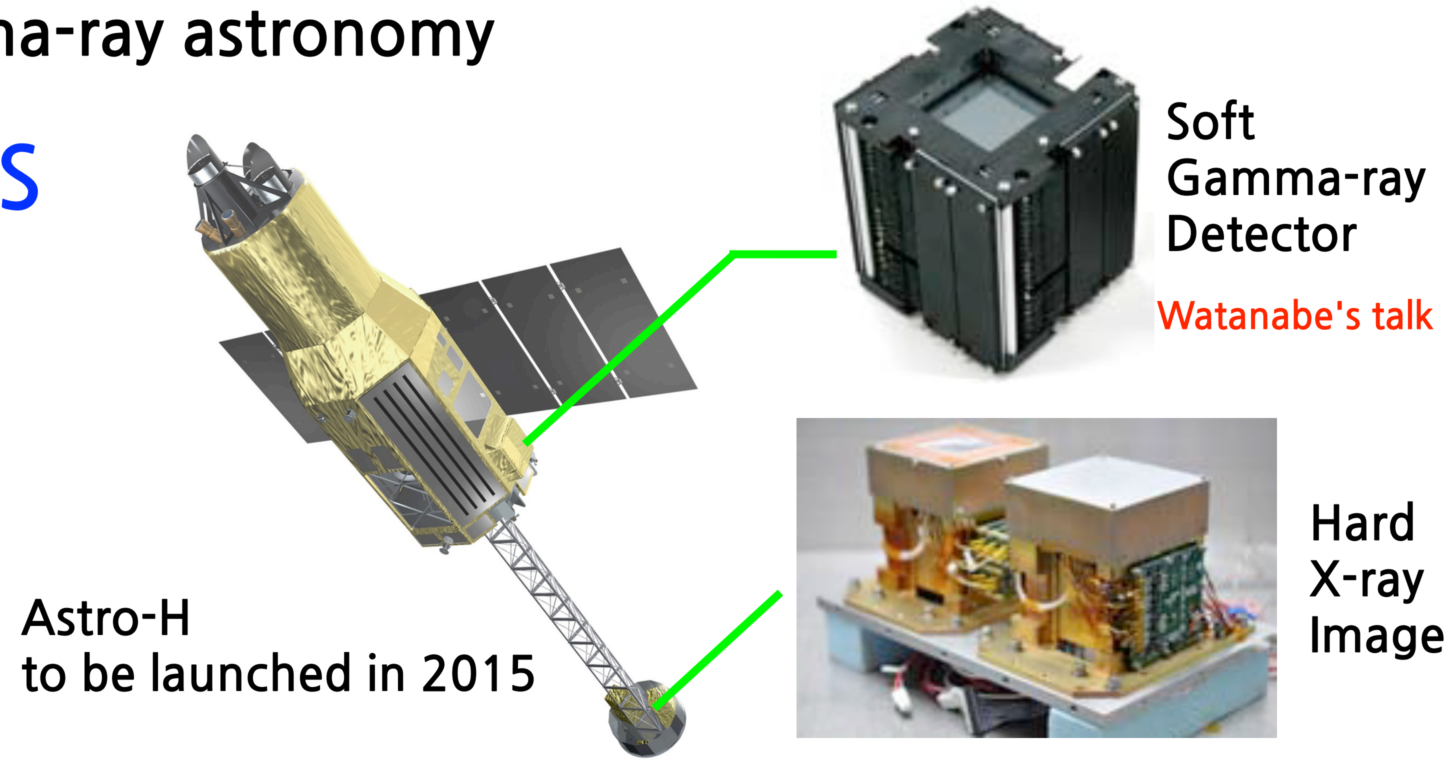
ASIC Dev. Activities at ISAS/JAXA

for X-ray & Gamma-ray astronomy

‣Collaboration with GM-IDEAS

VATA series ASICs specifically optimized
for CdTe/Si pixel/strip detectors

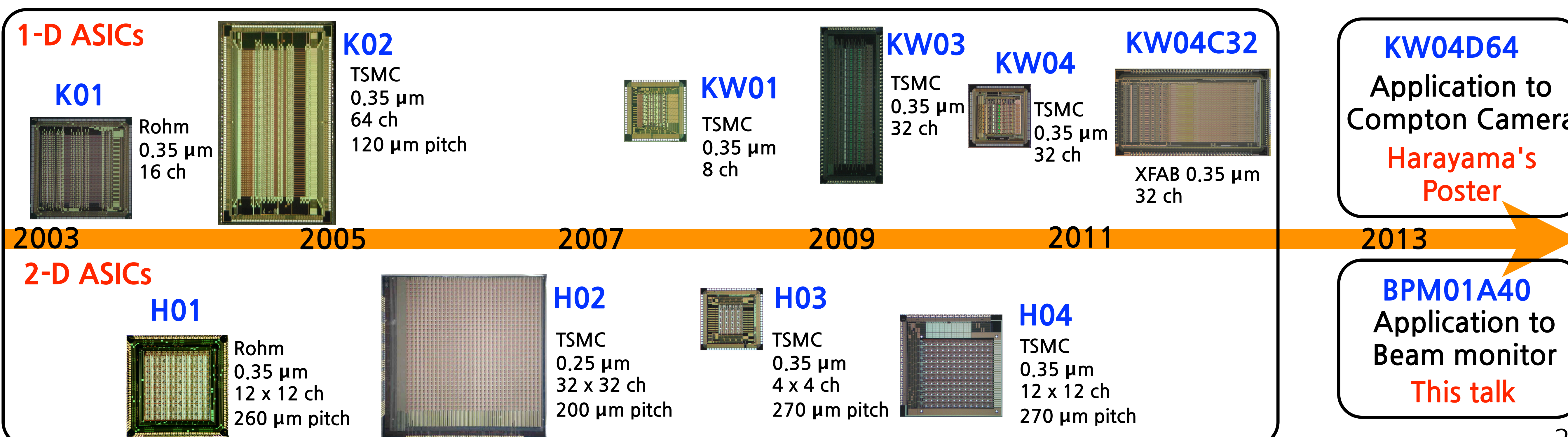




‣Original developments

Lead by Profs. Ikeda, & Takahashi

Several years of basic developments, ...
Now in the real application phase!



Spin-off Dev. for Medical application

Collaboration with Dr. Torikai (Gunma Univ.) & Dr. Yamaguchi (JAEA)

"Heavy ion radiotherapy"

At Gunma heavy ion medical center:

C^{6+} pinpoint beam
Φ ~3 mm (6σ)
$10^{5\text{-}9}$ particle/s
140-400 MeV/nucleus

accelerated by Synchrotron up to 70% of light of speed

irradiated into deep tumors within the patient

Current beam monitors:

- Fluorescent screen (not transparent)
  - Need to be removed after position adjustment

    => Takes hours for changing positions, painful for patients
- Strip line monitor
  - Works only in the current mode
  - Coarse resolution

Our plan:

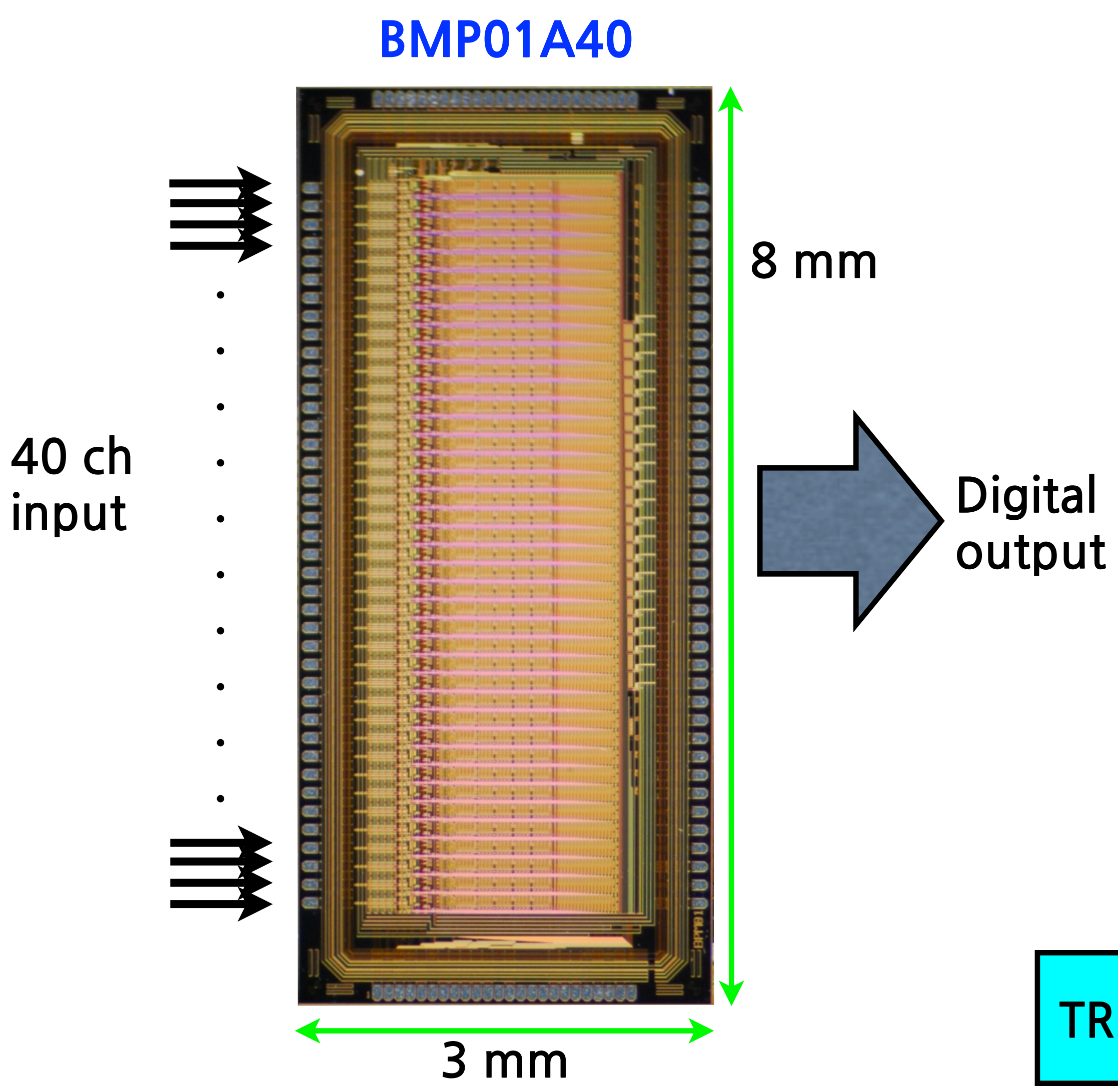
Develop a realtime beam monitor with fine pitch

Si strip detectors (mostly transparent for C^{6+} beam)

=> Precise measurement of the beam position & shape

To realize this, we need a high counting rate ASIC

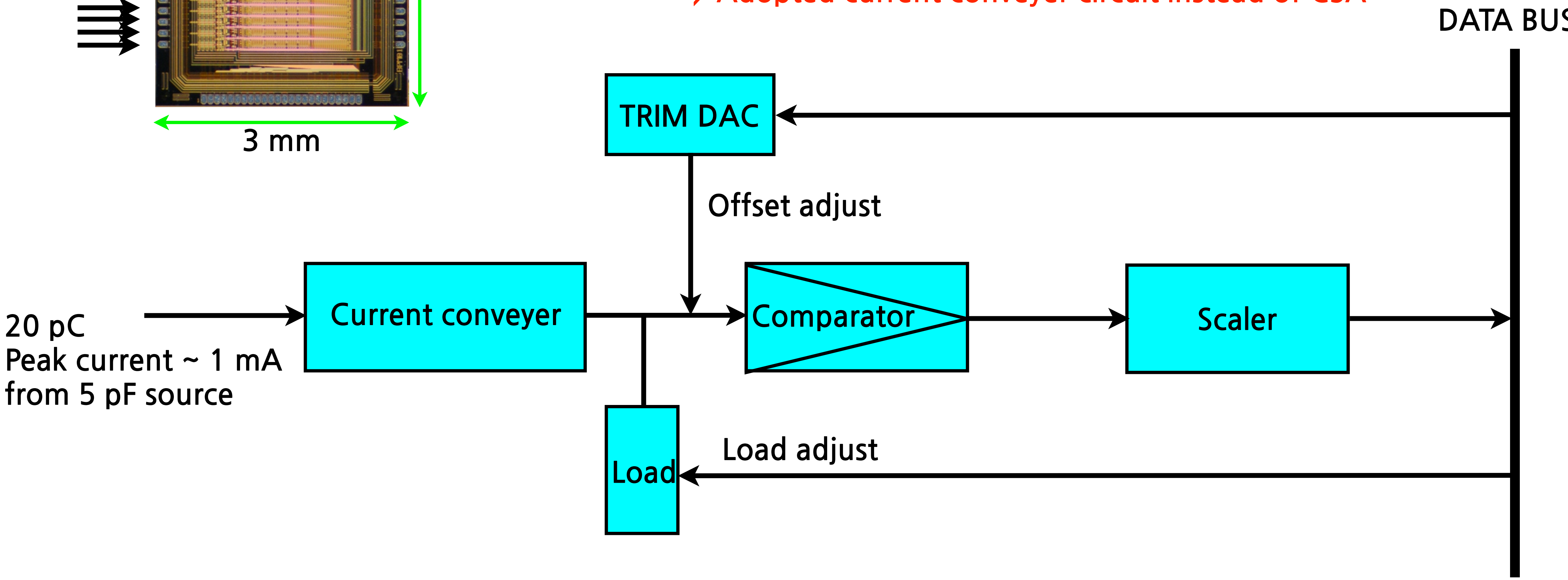
Development of a high counting rate ASIC



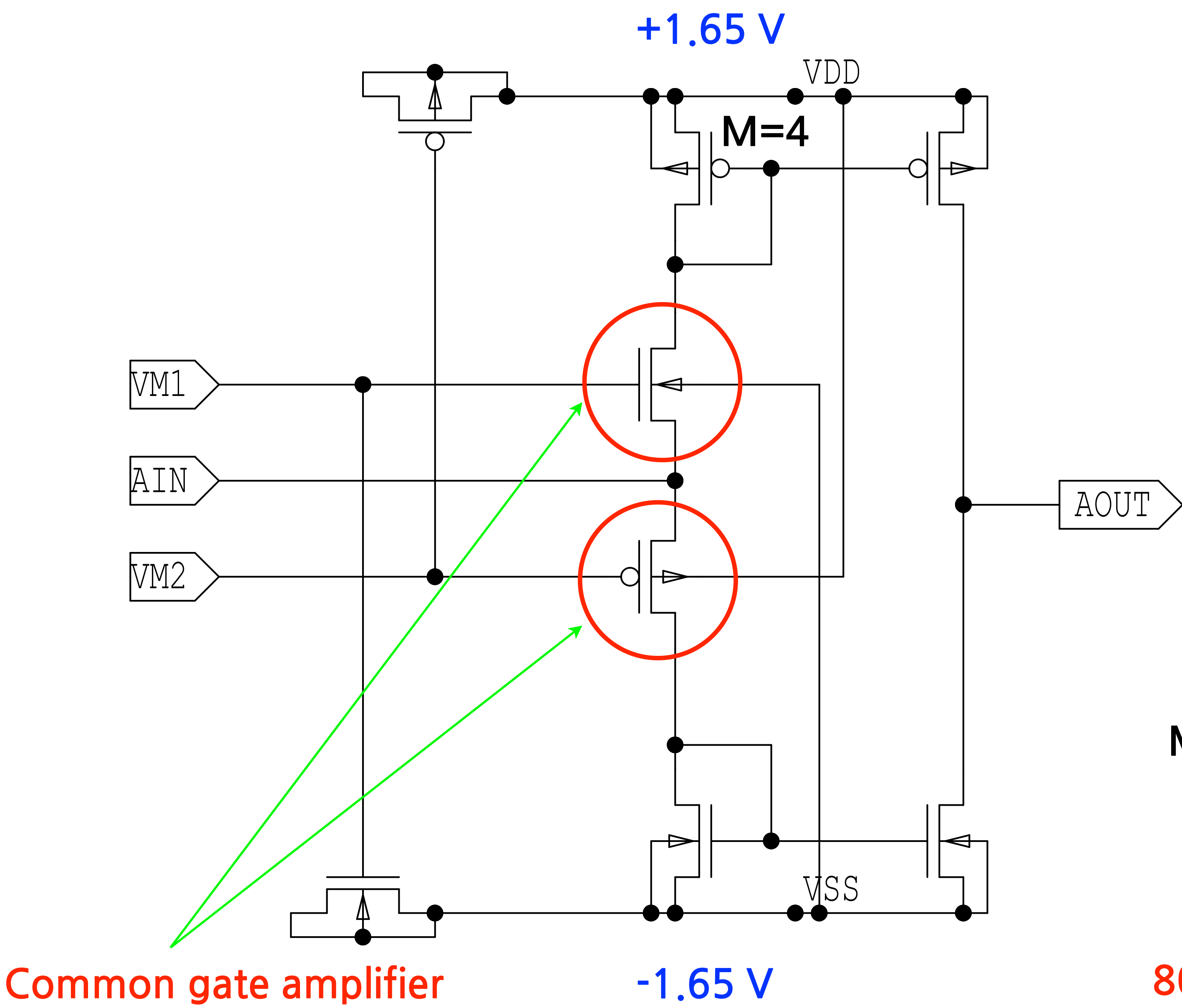
Process	XFAB 0.35 μm CMOS
Chip size	8 mm x 3 mm
Pad pitch	150 μm
Number of channels	40 ch
Counter bits	21 bits
Power supply	± 1.65 V
Power consumption	230 mW/chip

- Large input signal due to the heavy ions
- Requirement for fast signal processing

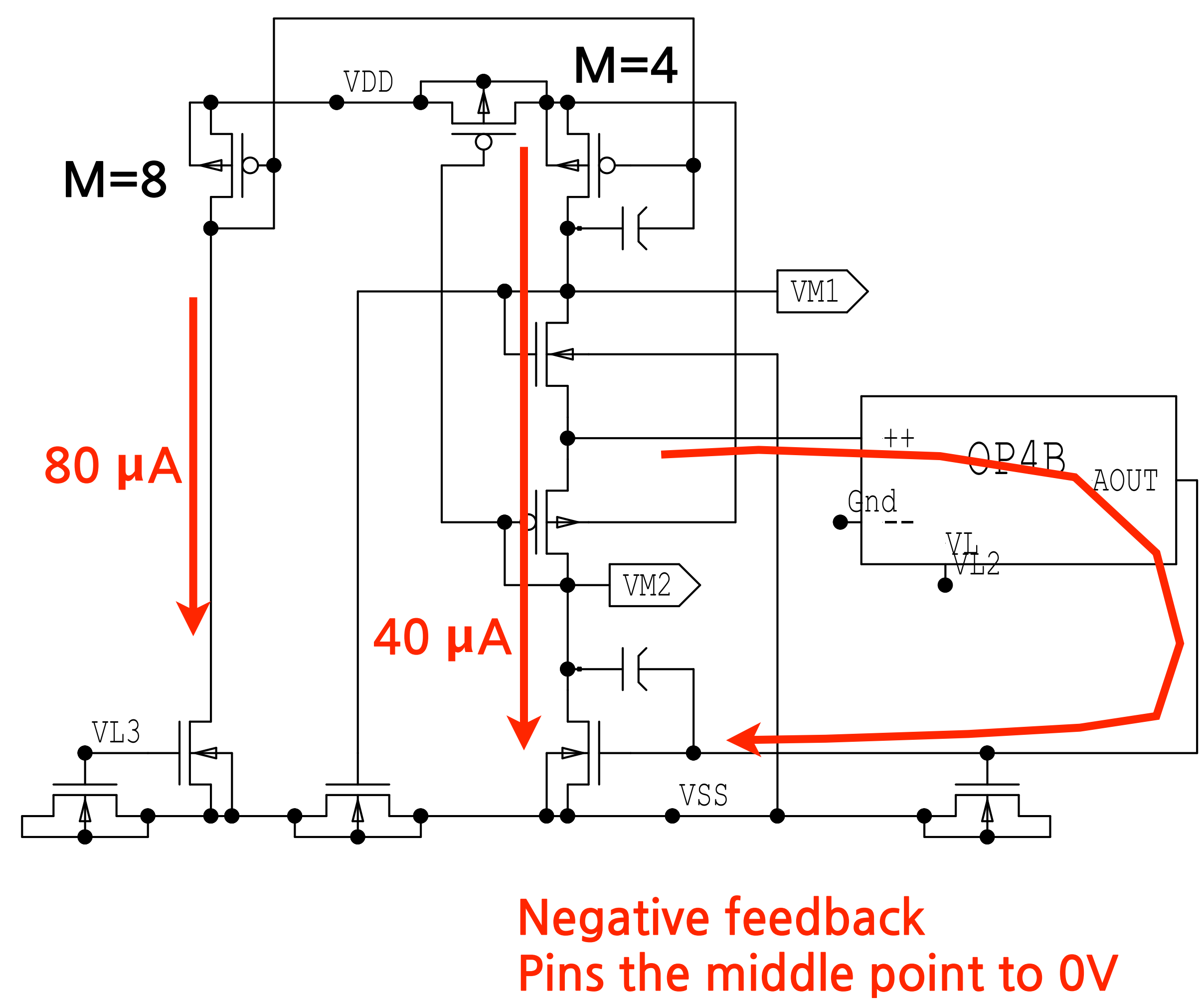
=> Adopted current conveyer circuit instead of CSA



Current conveyer circuit

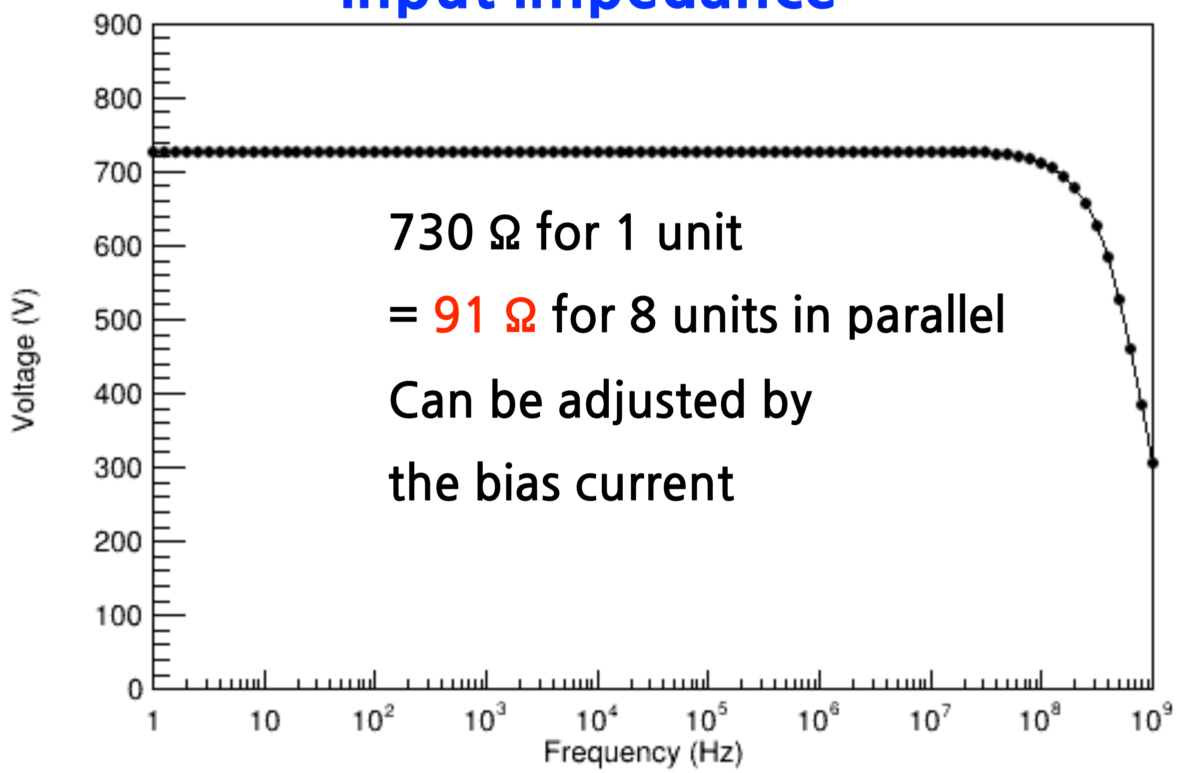


Bias circuit for VM1 &VM2

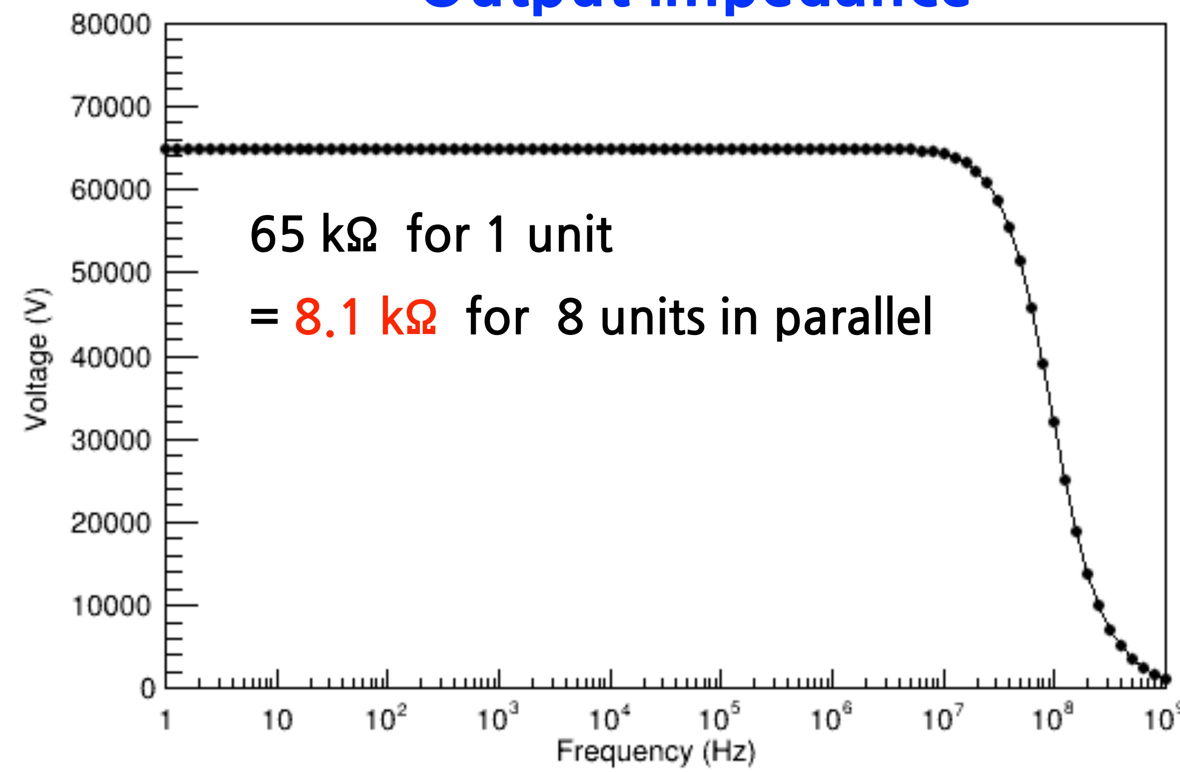


SPICE simulation

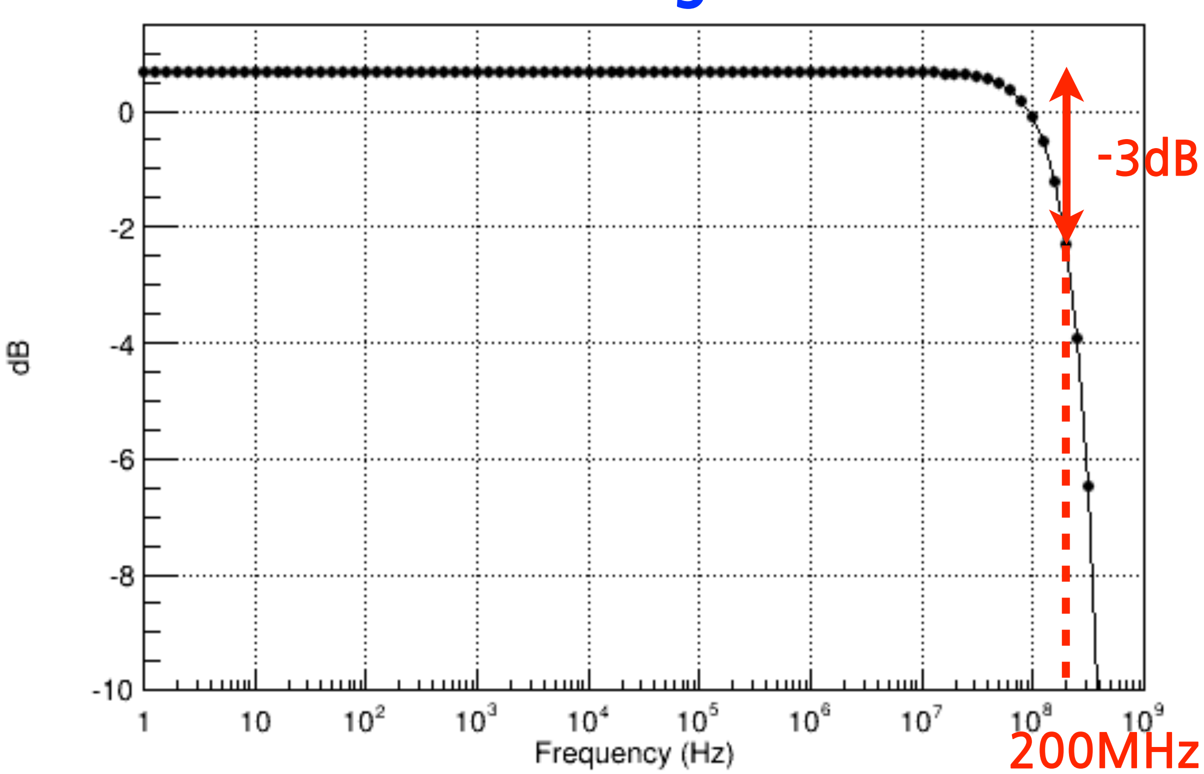
Input impedance



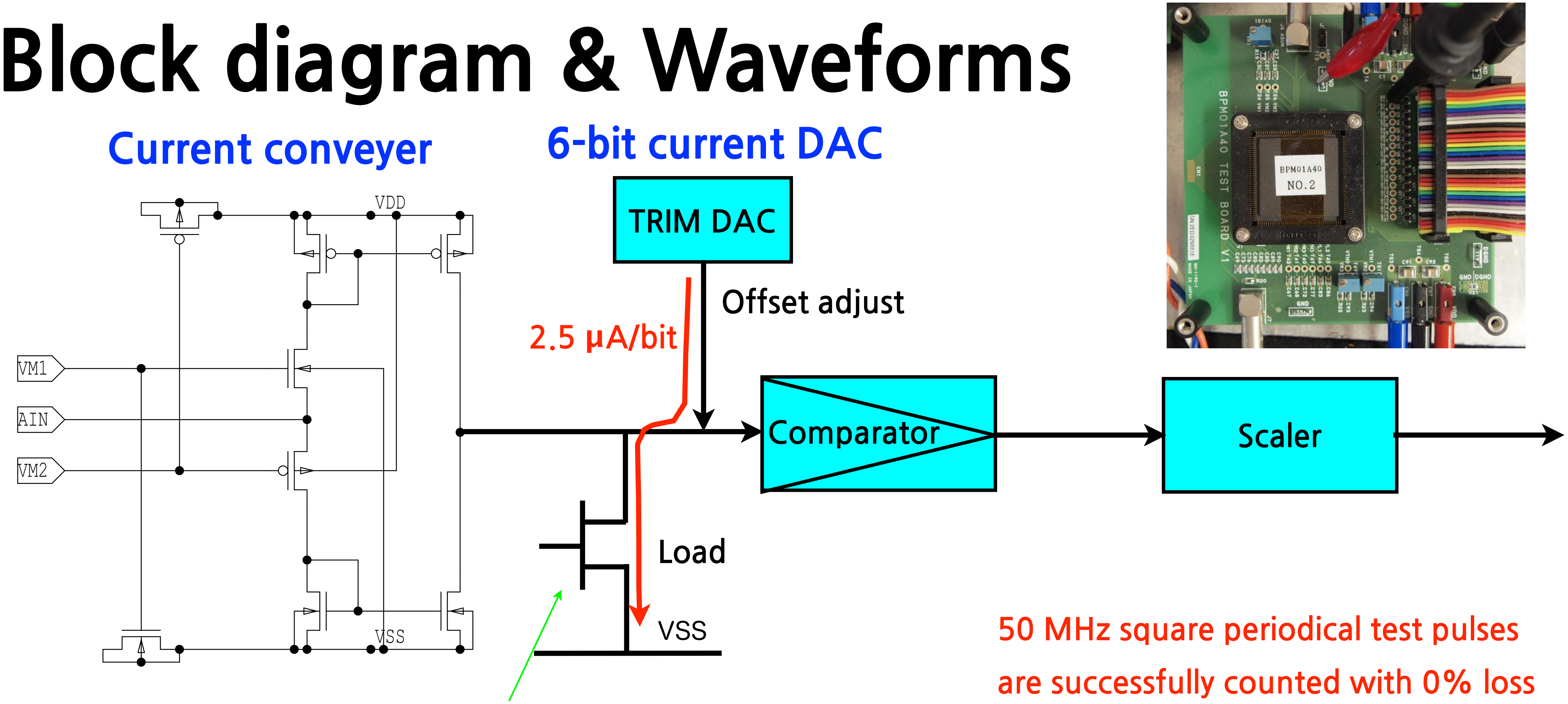
Output impedance



Transfer gain

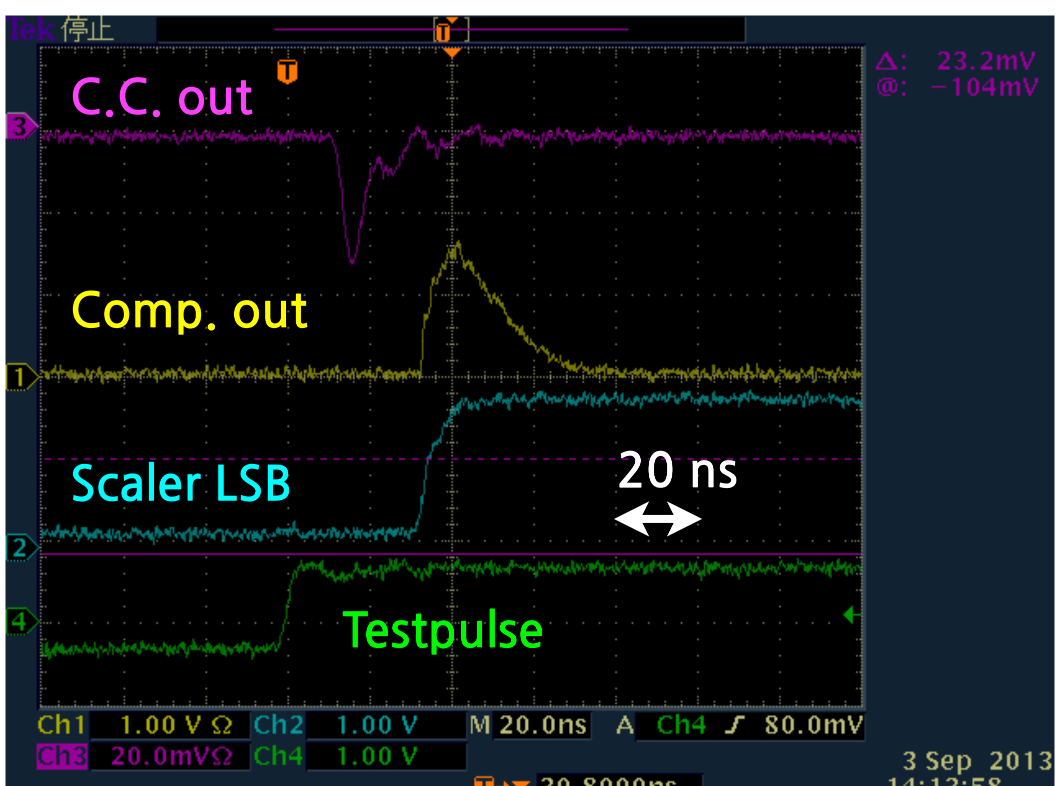


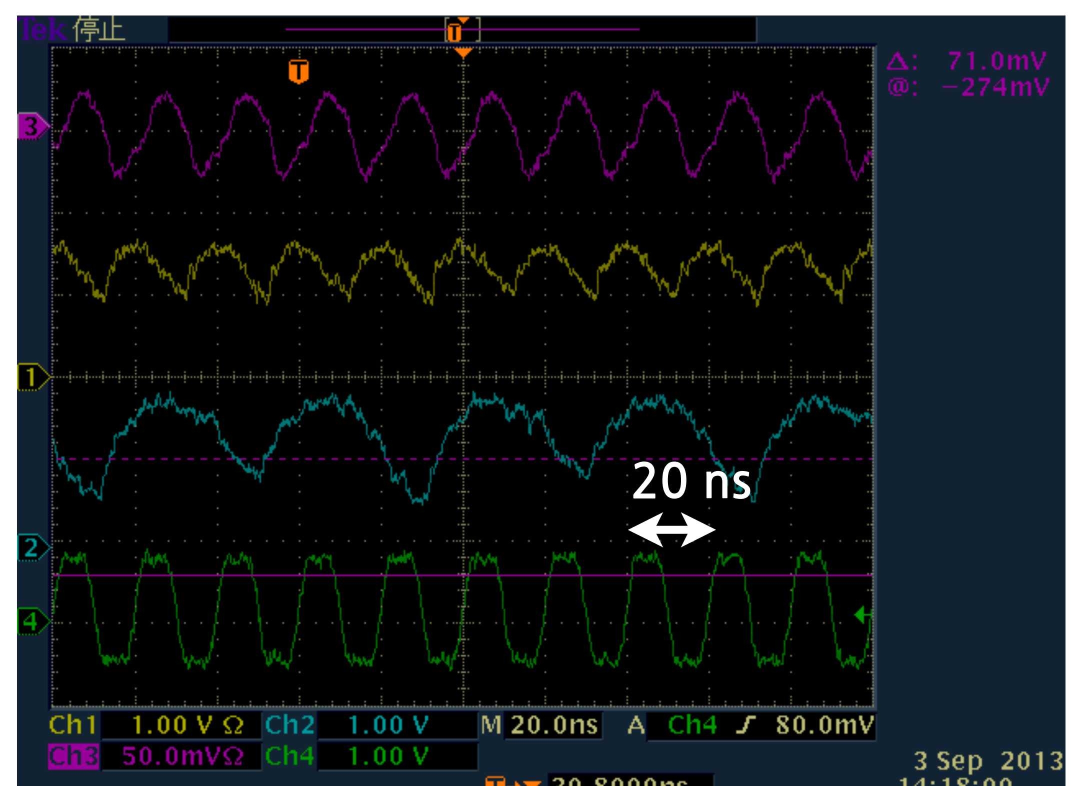
Block diagram & Waveforms



Utilize NMOS on-resistance

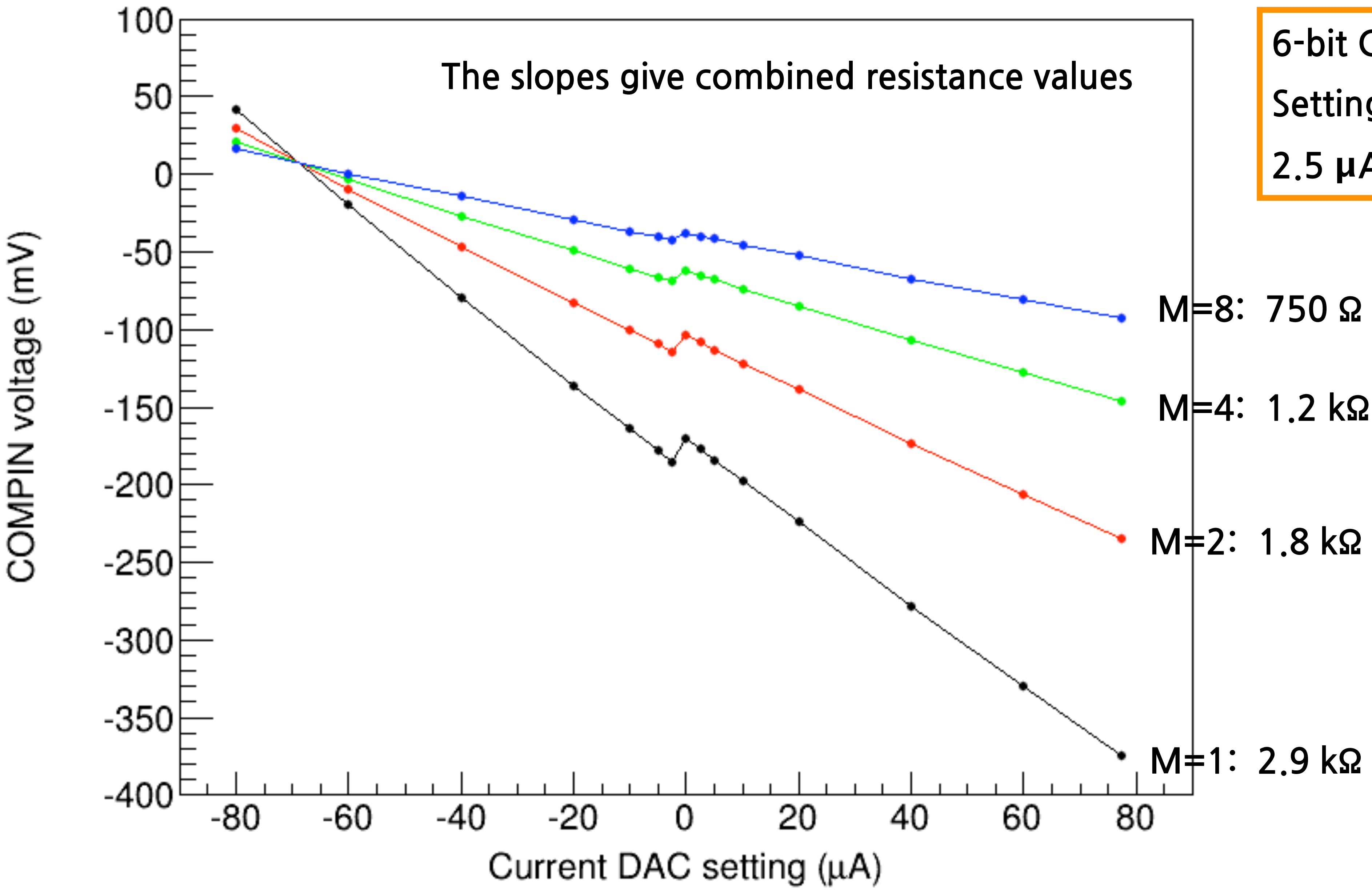
50 MHz square periodical test pulses are successfully counted with 0% loss (Maximum rate of the Pulse Generator)





Impedance measurement using TRIM DAC

Relation between the baseline voltage & current DAC settings



6-bit Current DAC
Setting from -32 to +31
2.5 μA/bit

※Different lines correspond to different load values (# of parallel MOS resistors)

Combined resistance $= \dfrac{Zo*(R+Zi)}{Zo+(R+Zi)}$ ⇒

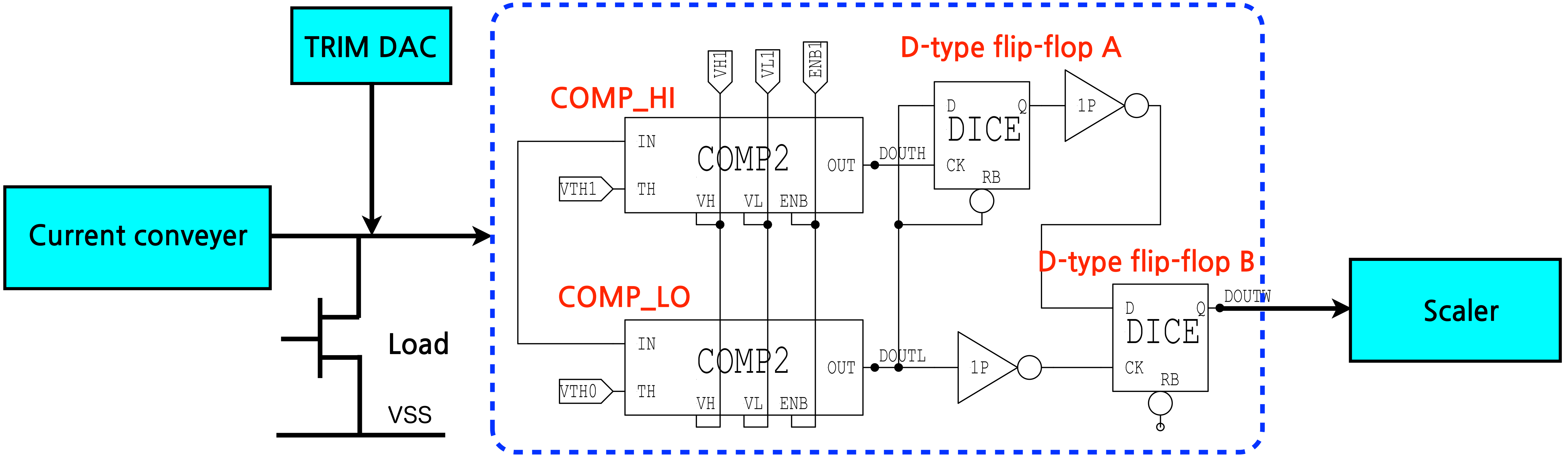
Input impedance of the C.C. = 89 Ω
Output impedance of the C.C. = 10.6 kΩ

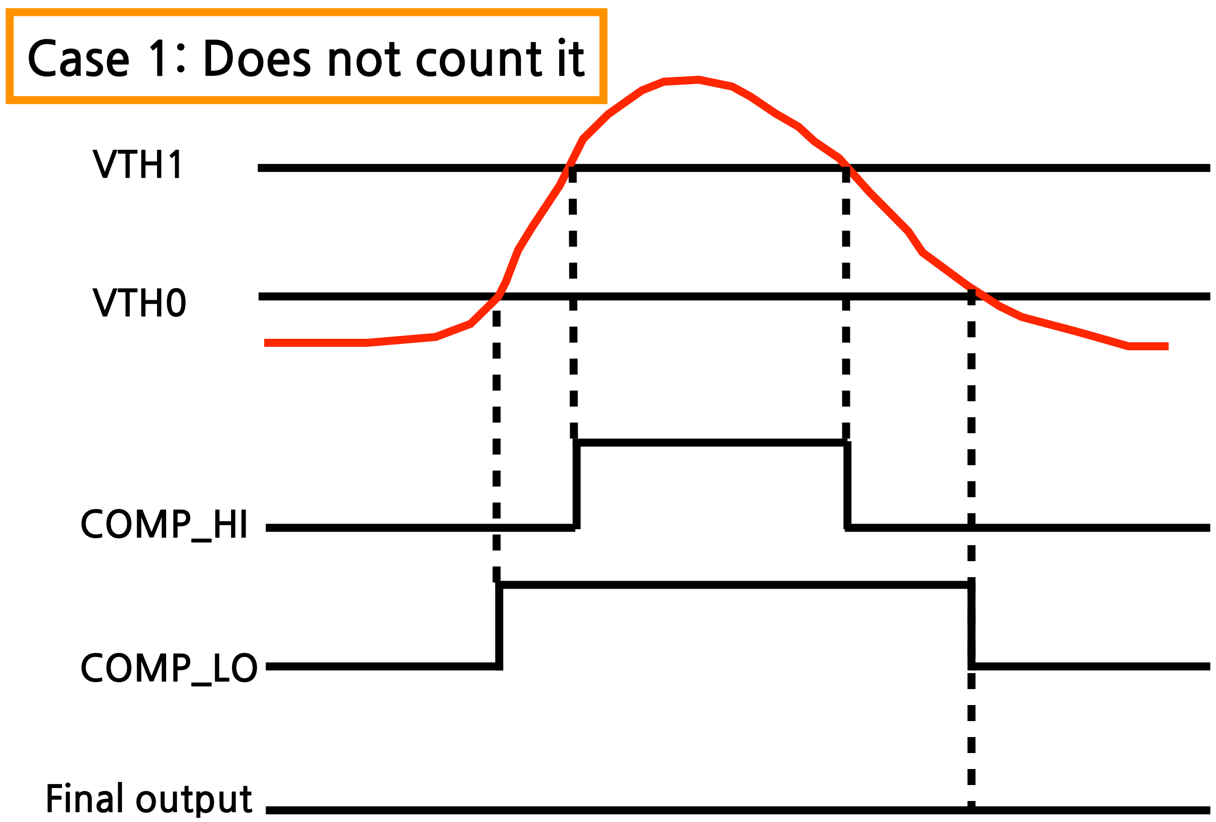
consistent ⟷

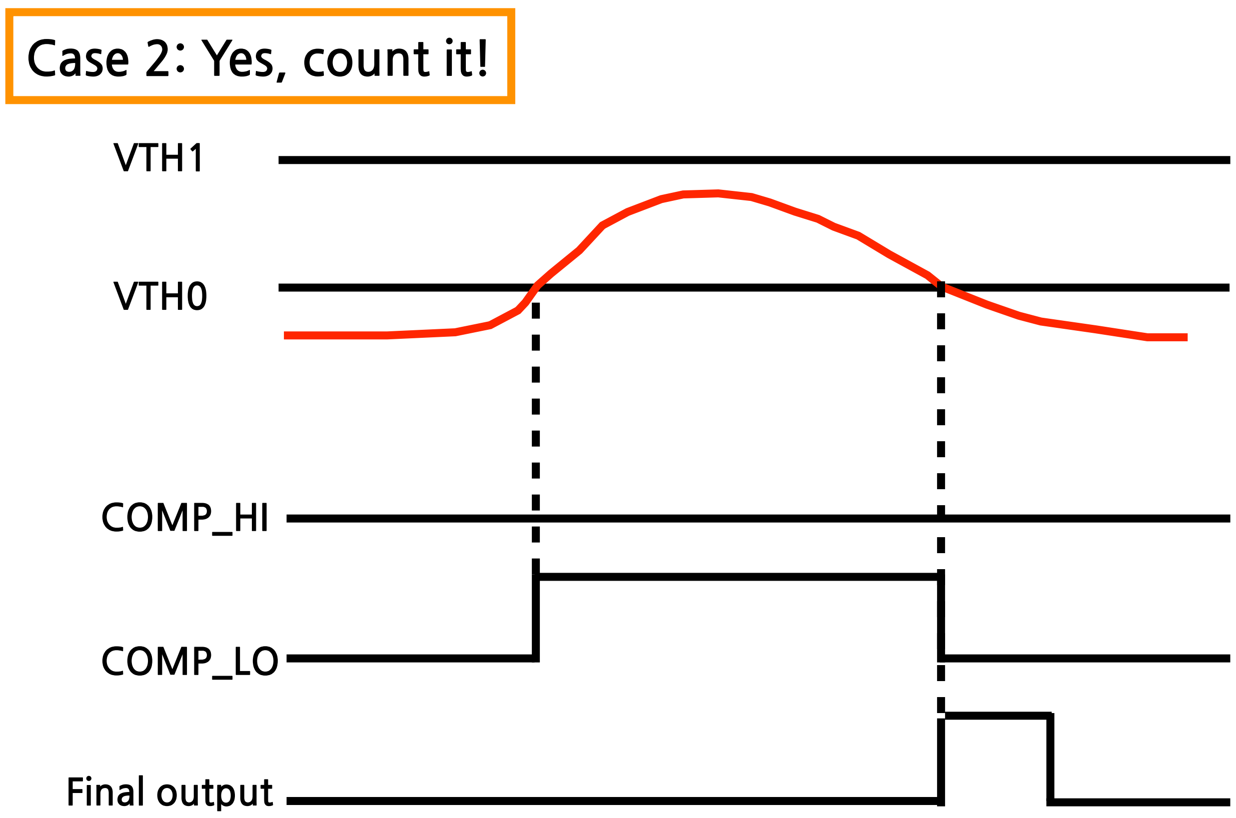
SPICE results
91 Ω
8.1 kΩ

Window comparator

1. When COMP_LO is hit, F-F A is enabled
2. F-F A remembers whether COMP_HI is hit
3. At the falling edge of COMP_LO
   F-F B makes the final judgement





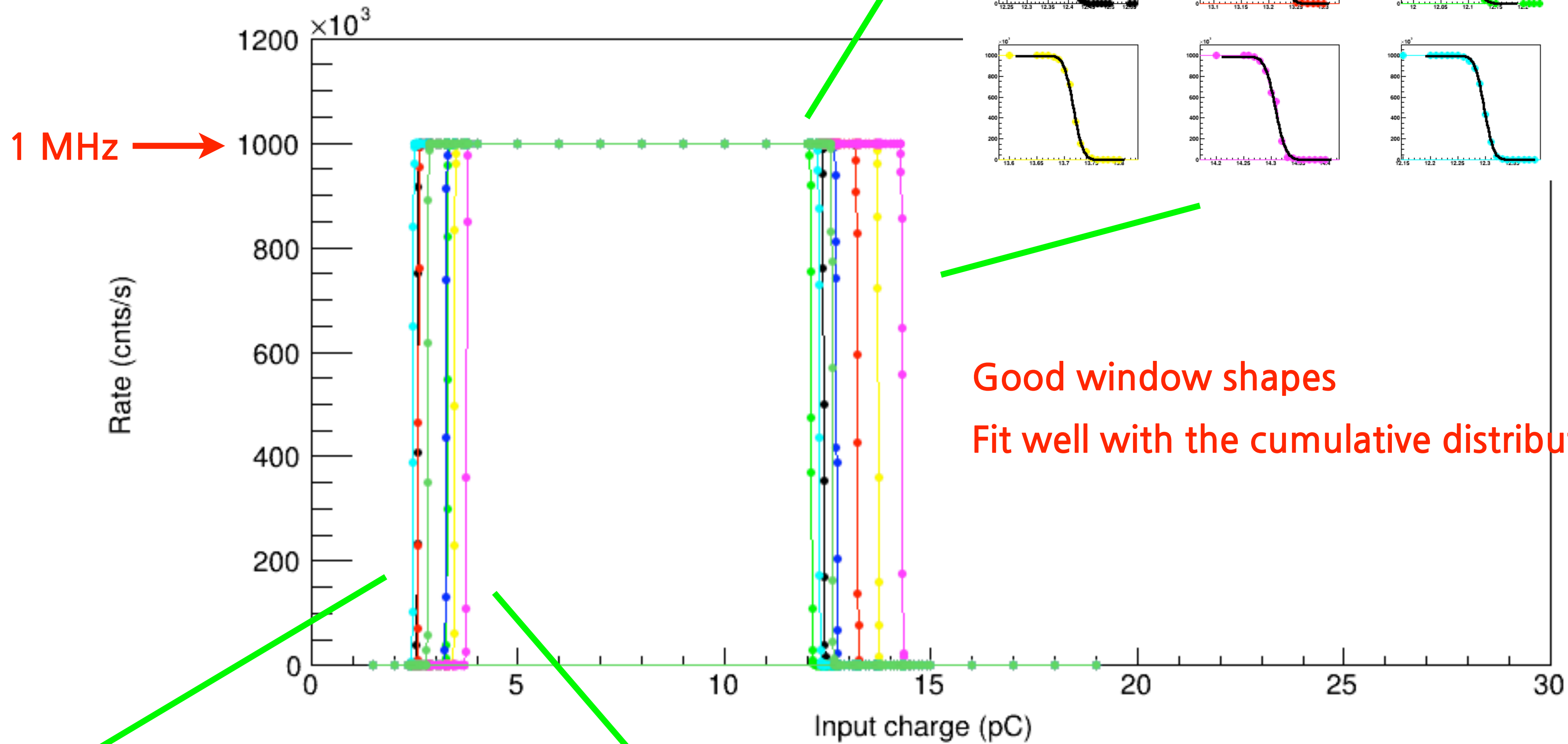


Window comparator performance

8 channels out of 40 were tested

1 MHz test pulse

Higher threshold dispersion: ± 9%



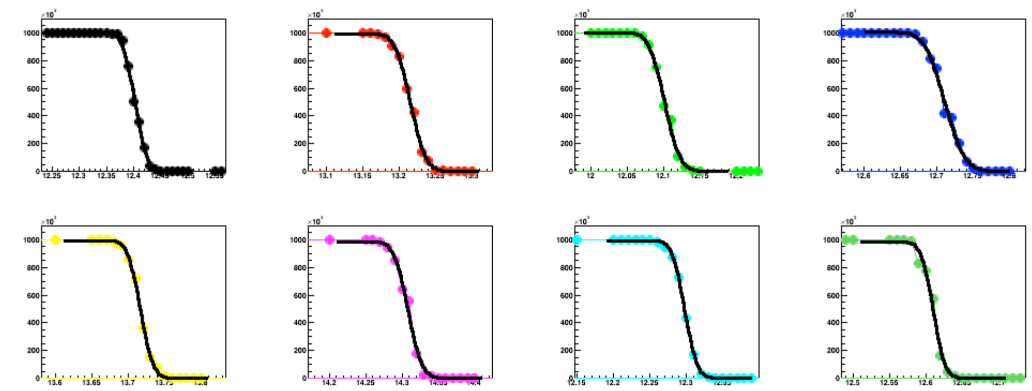
Good window shapes

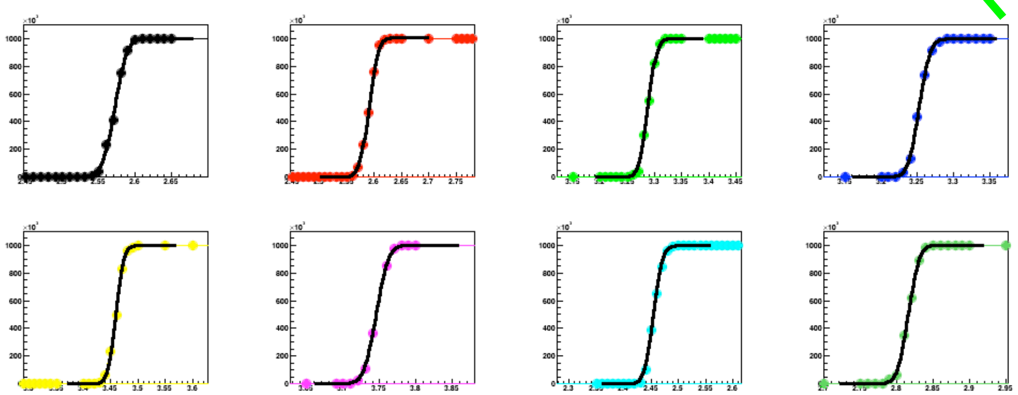
Fit well with the cumulative distribution function

VTH0: -100 mV

VTH1: -300 mV

Lower threshold dispersion: ± 20%

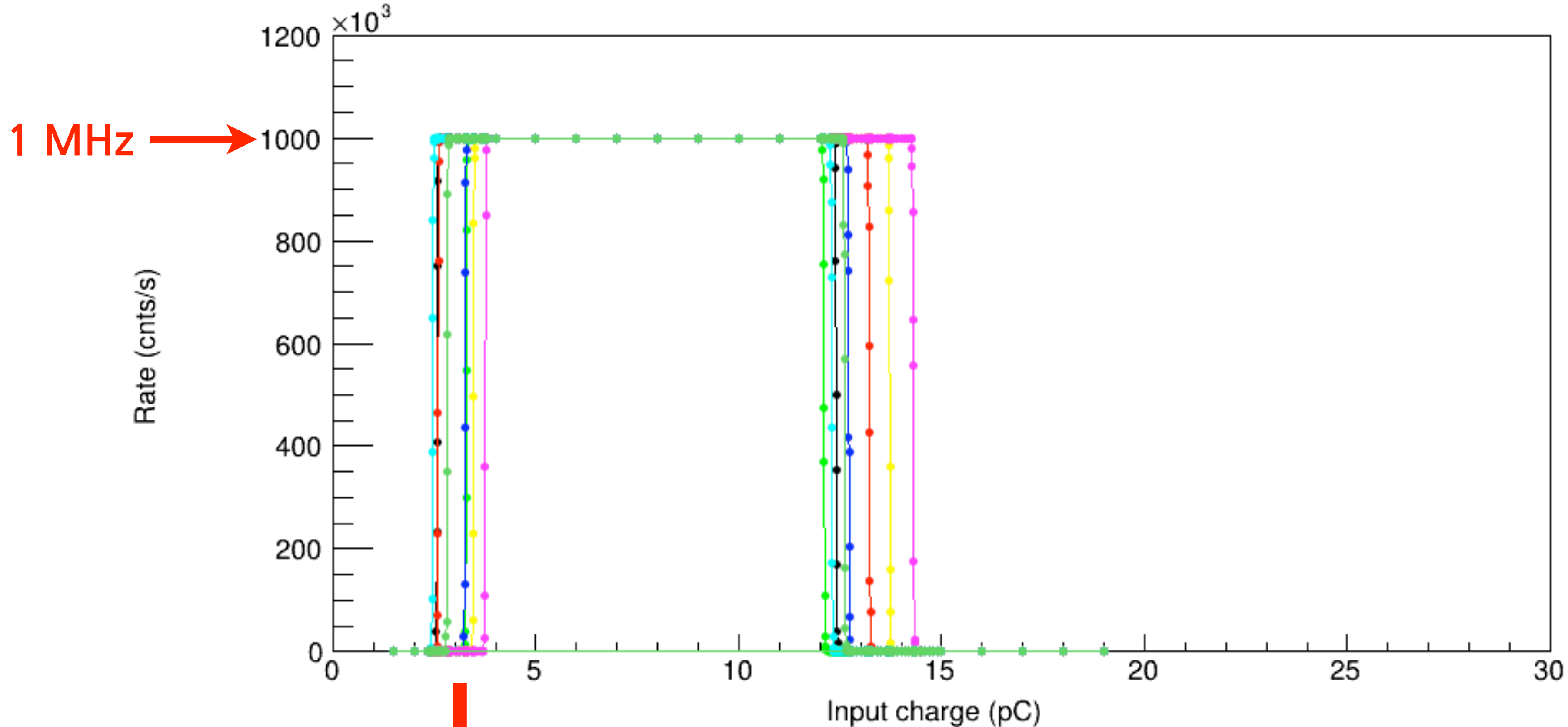




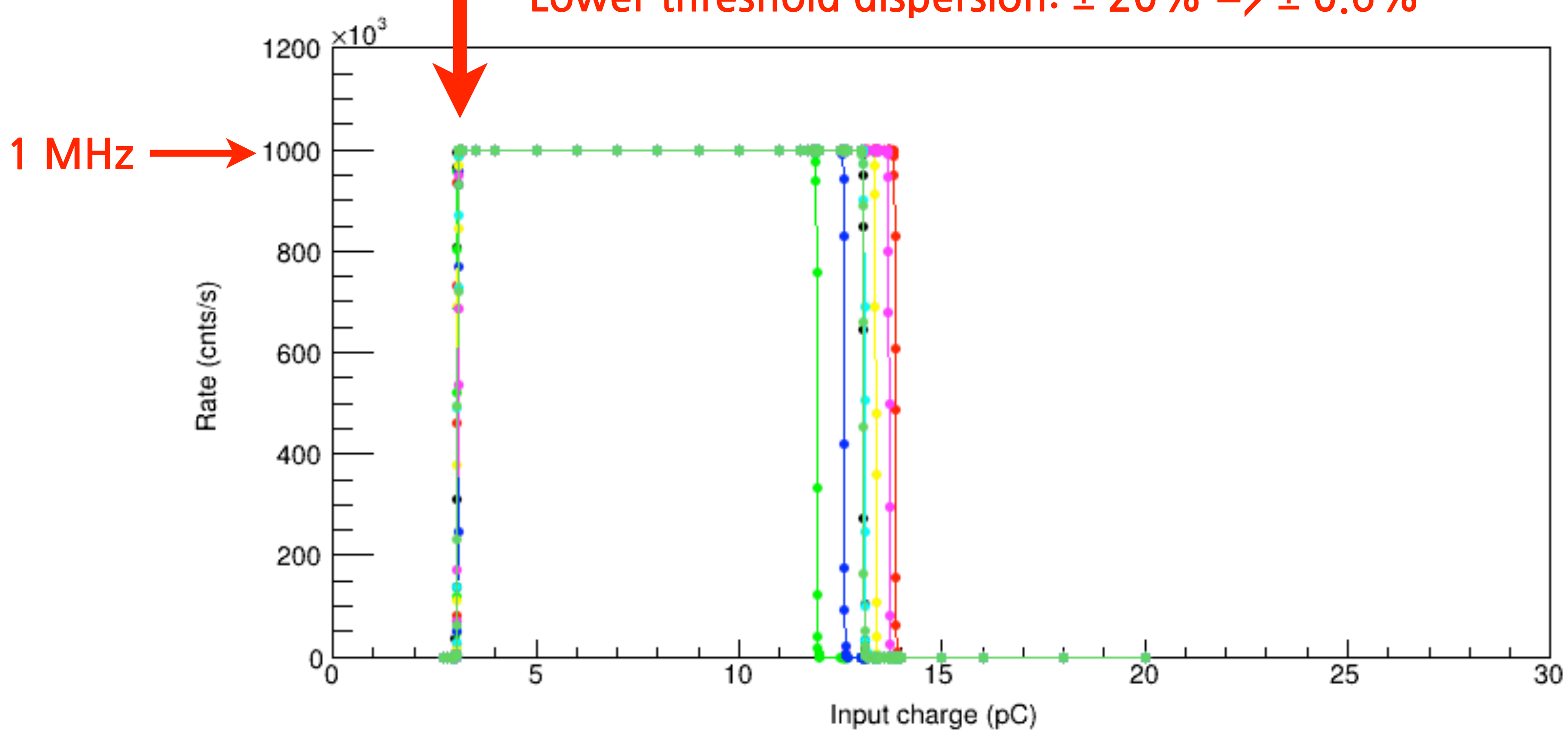
Gain dispersion: ± 9%

Noise distribution: 12~22 fC

Offset adjustment by TRIM DAC



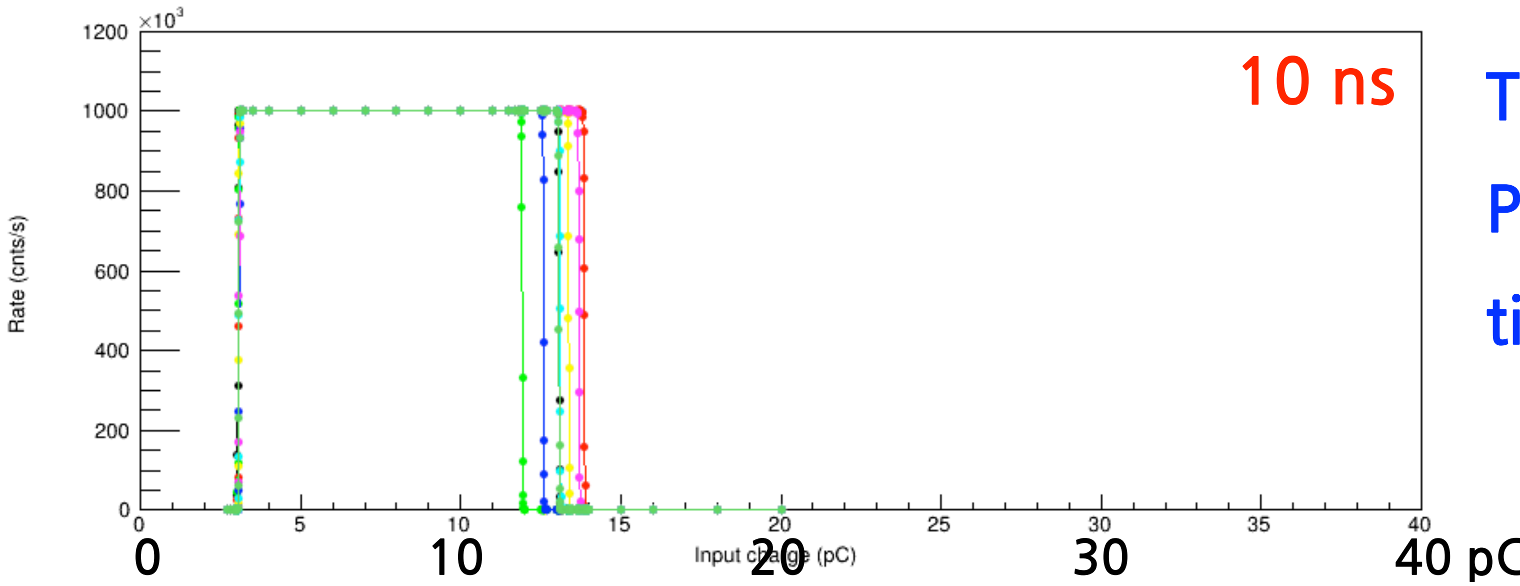
Lower threshold dispersion: ± 20% => ± 0.6%

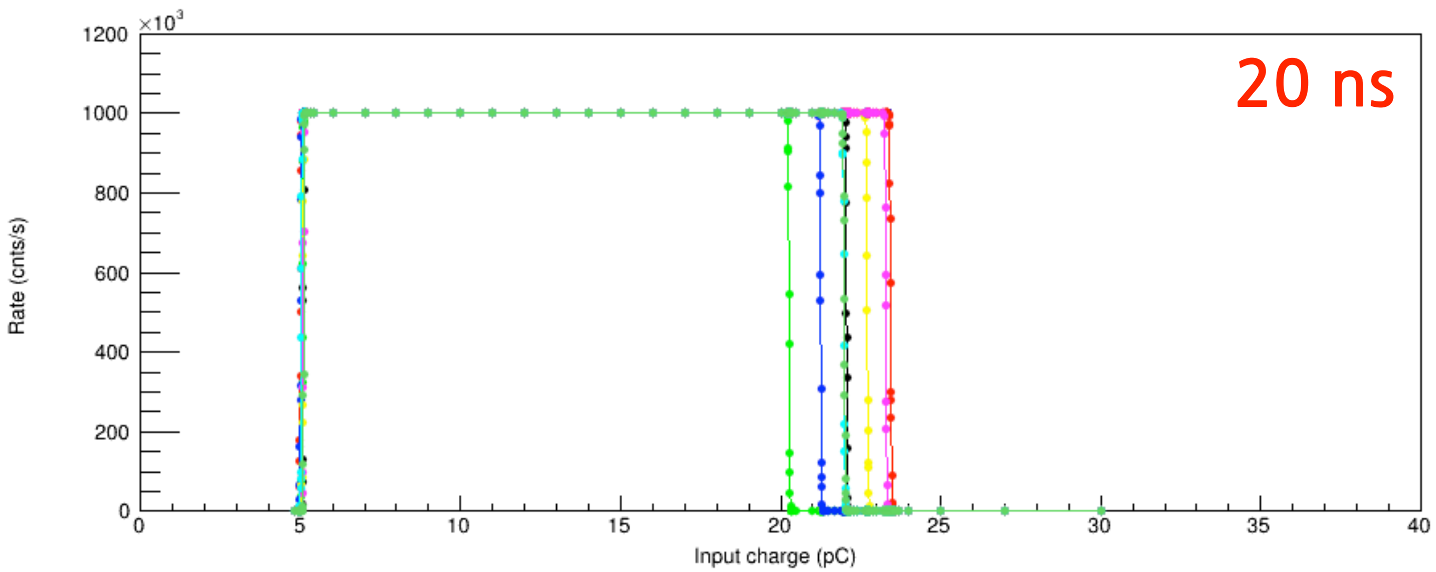


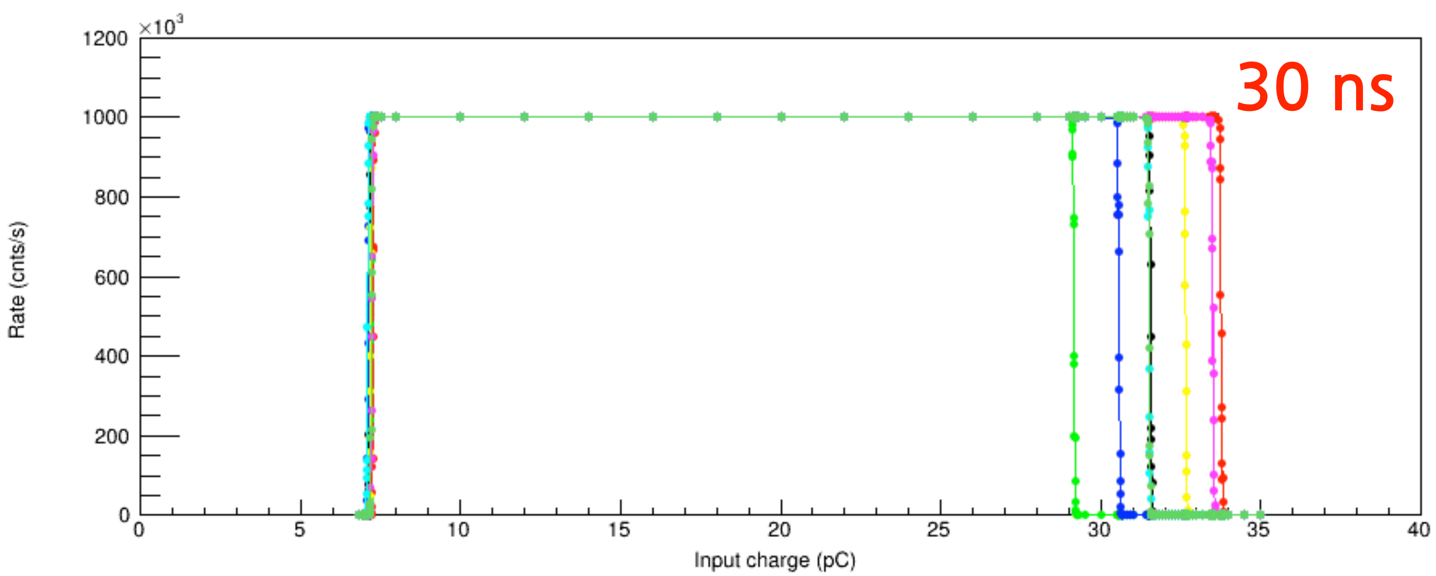
VTH0: -100 mV

VTH1: -300 mV

Response to different rise time







The circuit is current sensitive

Pulse height depends on the rise time of the input signals

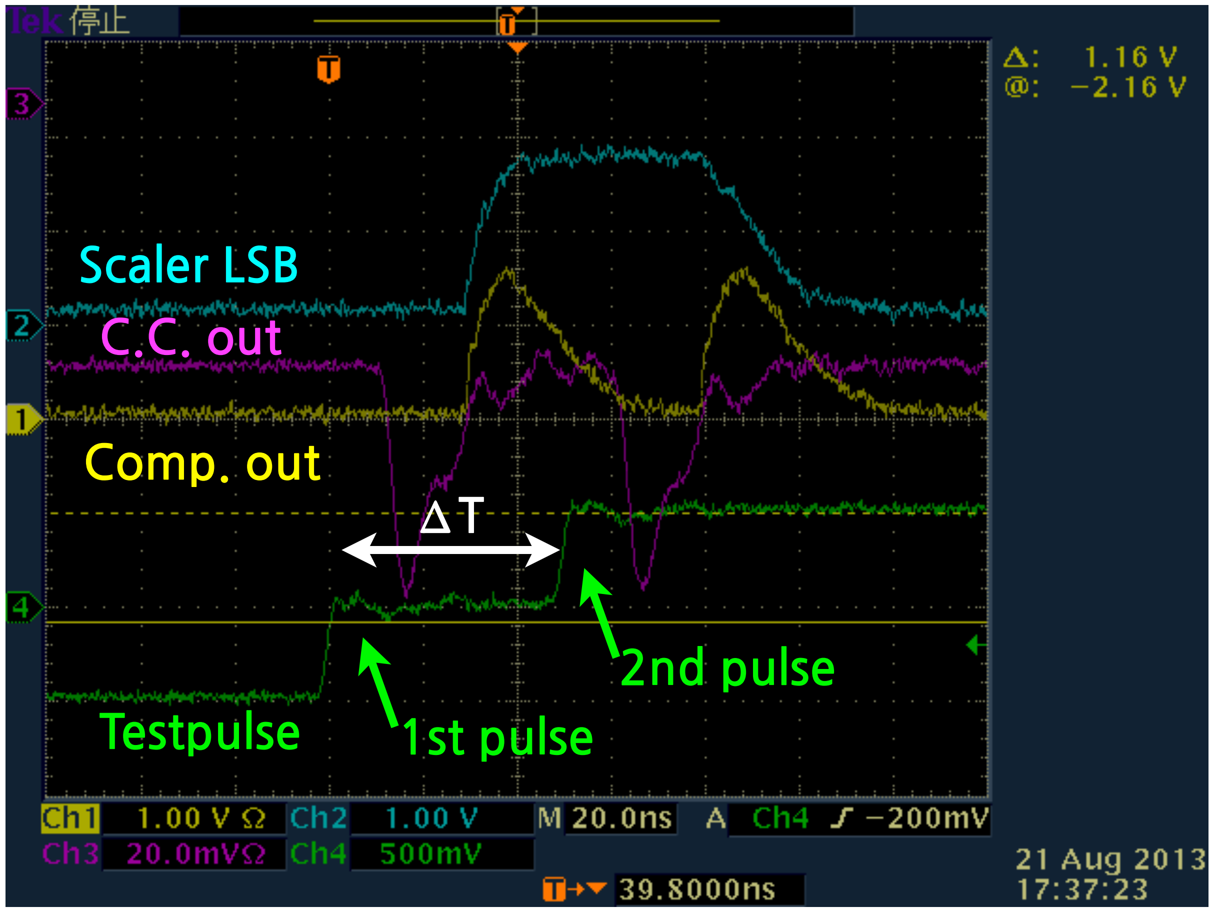
Expectation:

10-30 ns for Silicon strip detectors

Works just as expected

No problem found in this range

Double pulse experiment



Investigate how close pulses are distinguished

ΔT is changed

Fixed pulse height ~230 mV

Fixed VTH0 -200 mV

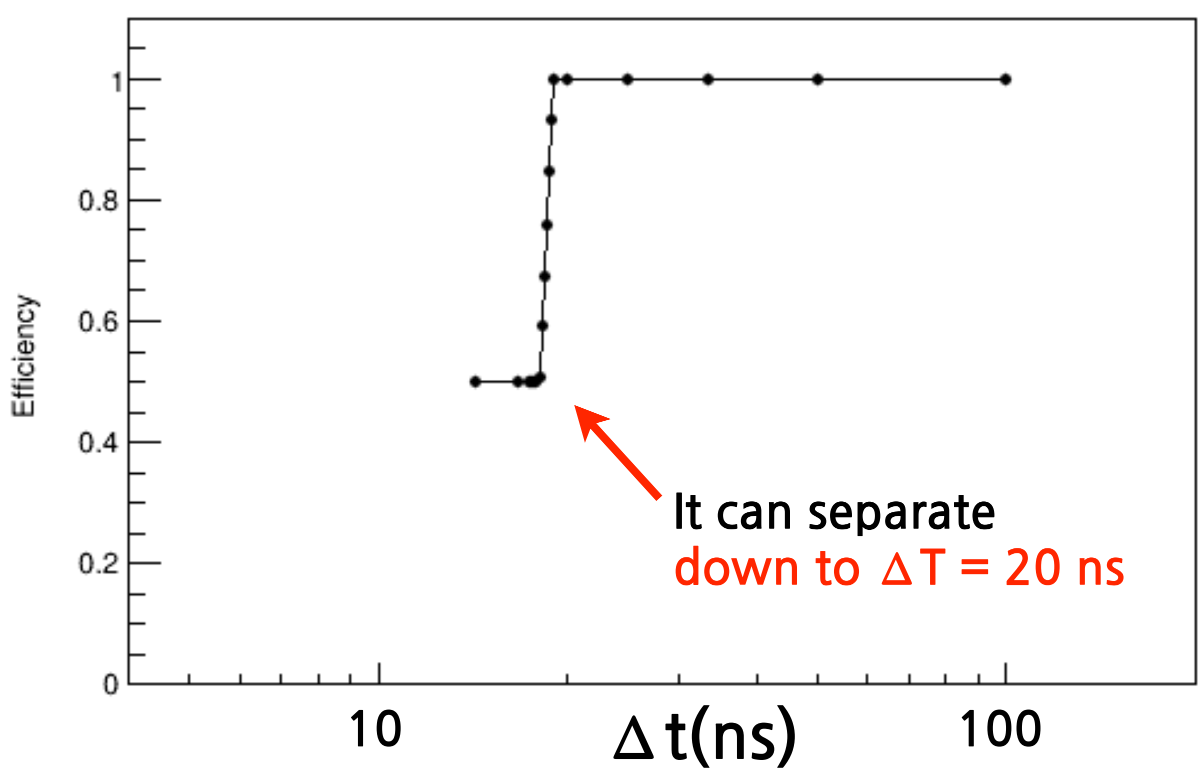
Counting efficiency is measured

Eff. = 1 : 0% loss

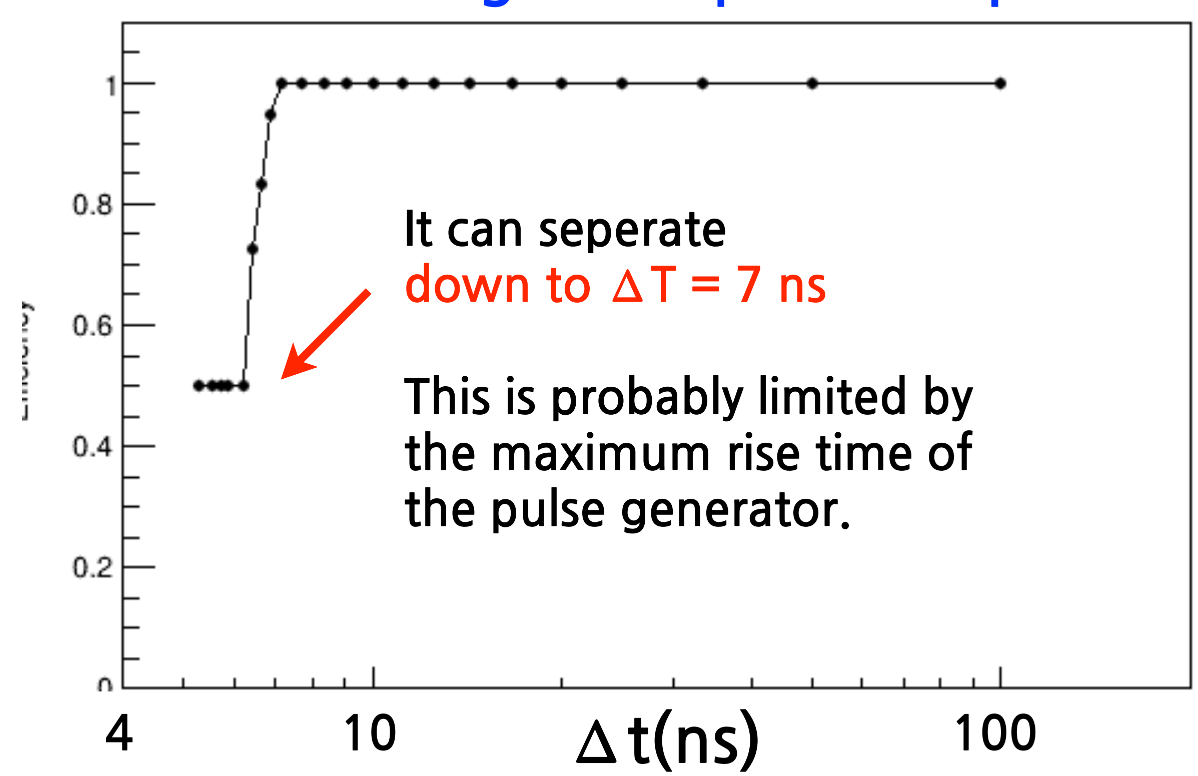
Eff. = 0.5 : Get 1st pulse, miss 2nd pulse

※ Pulse generator maximum rise time: 5 ns

Window comparator operation



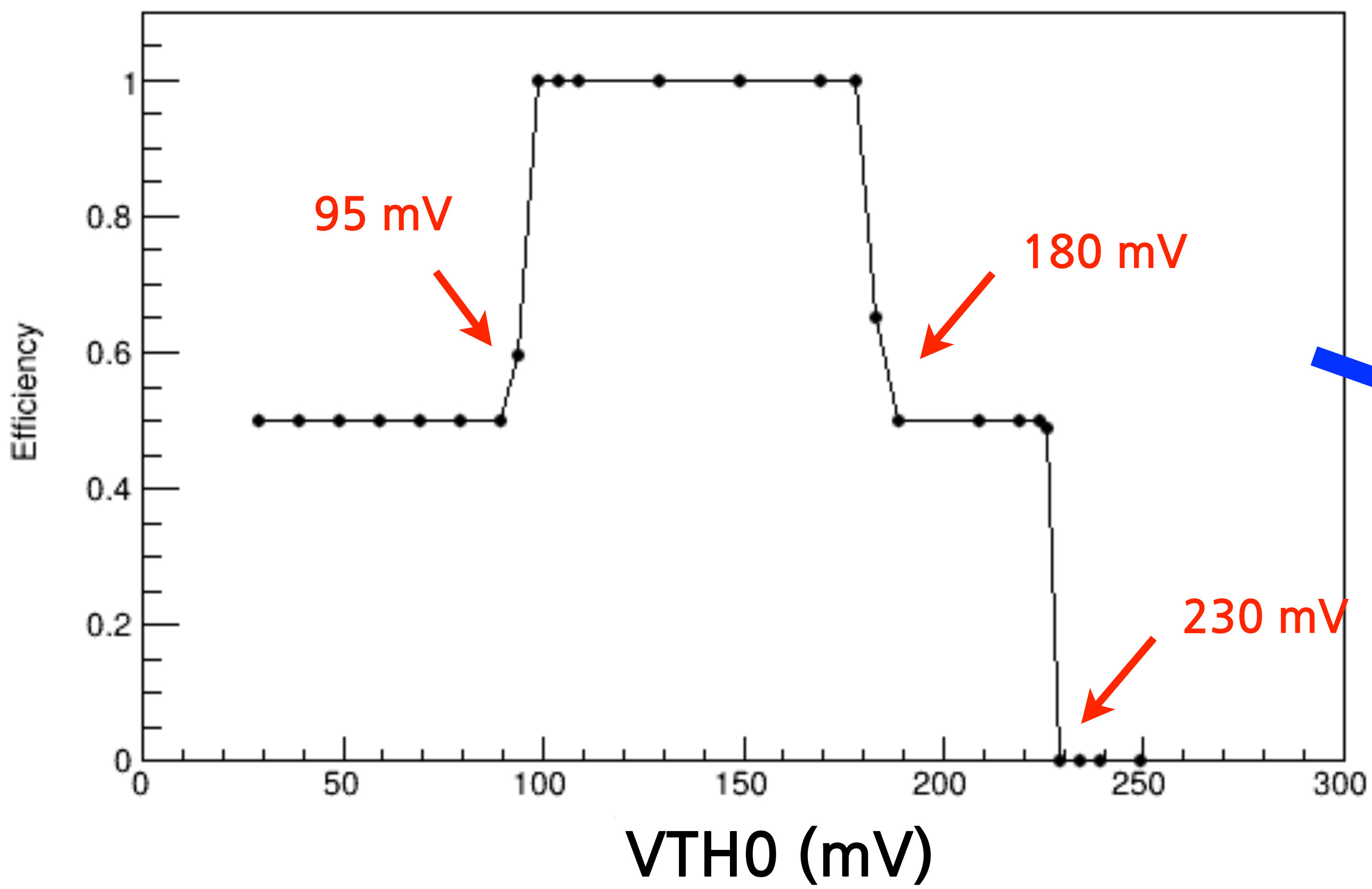
Faster response is achieved
with the single comparator operation



Double pulse experiment

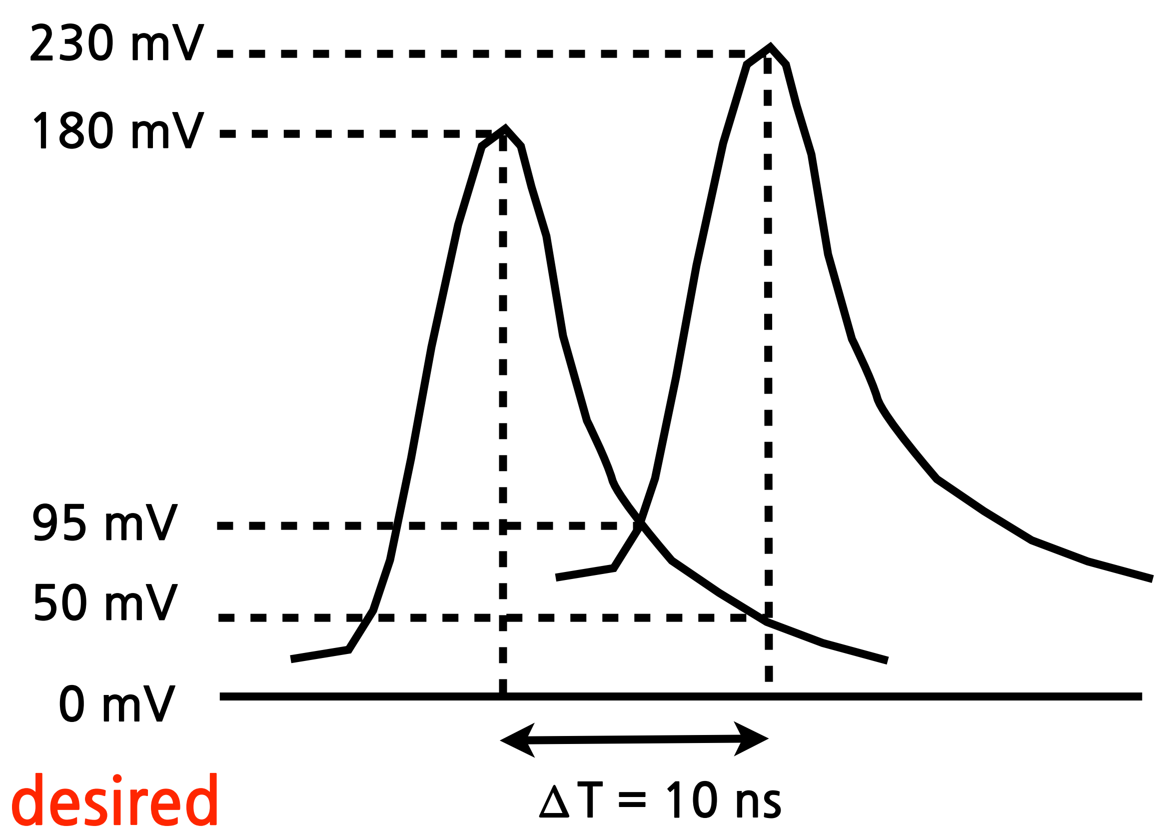
Fixed ΔT to 10 ns

Investigated dependence on VTH0



※Because of stray capacitance and probe capacitance, it is hard to observe actual pulse shape inside the ASIC.

Deduced pulse shape



Confirmed that the signal tail is quite small as desired

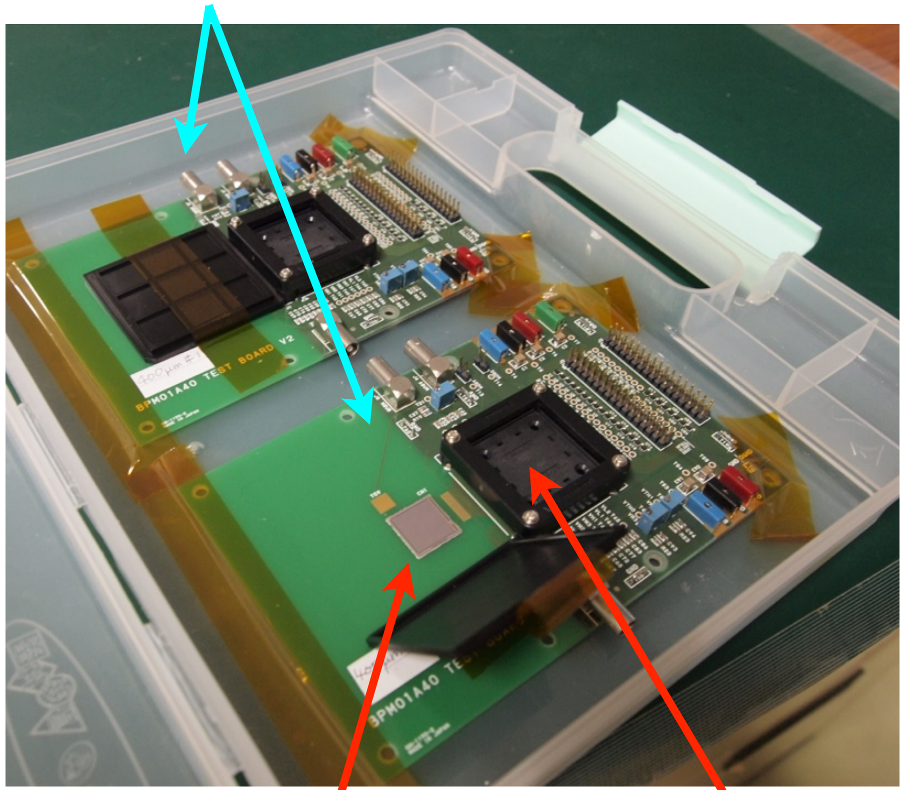
Summary

- We developed high rate counting ASIC for heavy ion beam monitoring
- Circuit properties agree well between SPICE simulation and measurements
- Confirmed no loss up to 50 MHz (periodic)
- Pulse can be distinguished down to
  - 20 ns with window comp.
  - 7 ns with single comp. (maybe better)

- Future plan
  - Connect the ASICs to Si single side strip detectors
  - Place two sets of detectors in orthogonal configuration
  - Beam experiment at Gunma medical center

Process	XFAB 0.35 µm CMOS
Chip size	8 mm x 3 mm
Pad pitch	150 µm
Number of channels	40 ch
Counter bits	21 bits
Power supply	± 1.65 V
Power consumption	230 mW/chip

Two sets of detectors will be located orthogonally



Si single side strip detector
300/400 µm pitch

ASIC