

Development of HPK n in p Pixel Sensors for HL-LHC

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Outline

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- 1. Introduction**
- 2. Development status**
 - 2-1 : Novel Slim edge**
 - 2-2 : Edge spark protection**
- 3. Summary**

Hamamatsu Si detectors for HEP

Direct detector

Silicon Strip Detector(SSD)

Silicon Pixel Detector

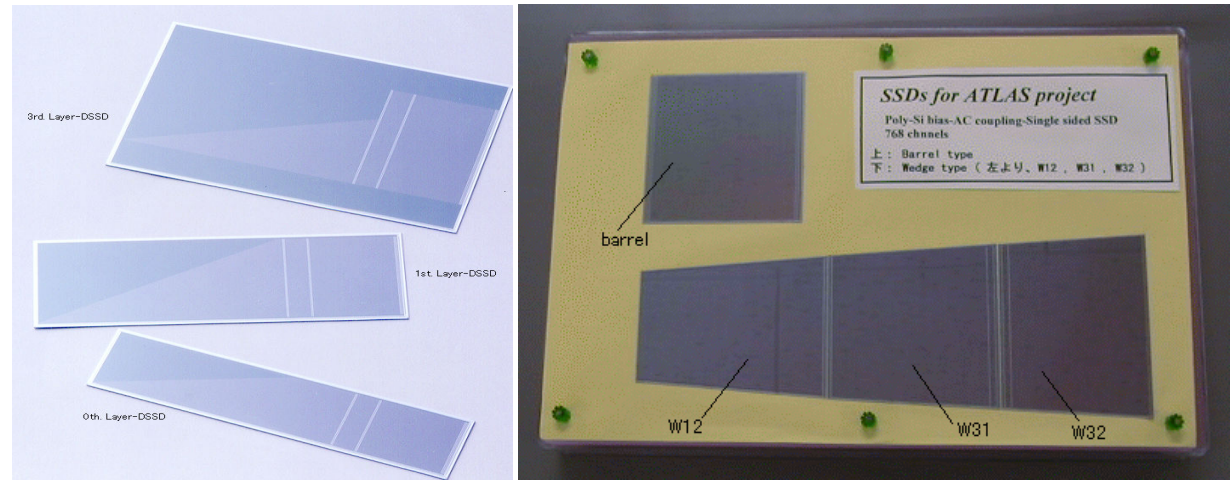
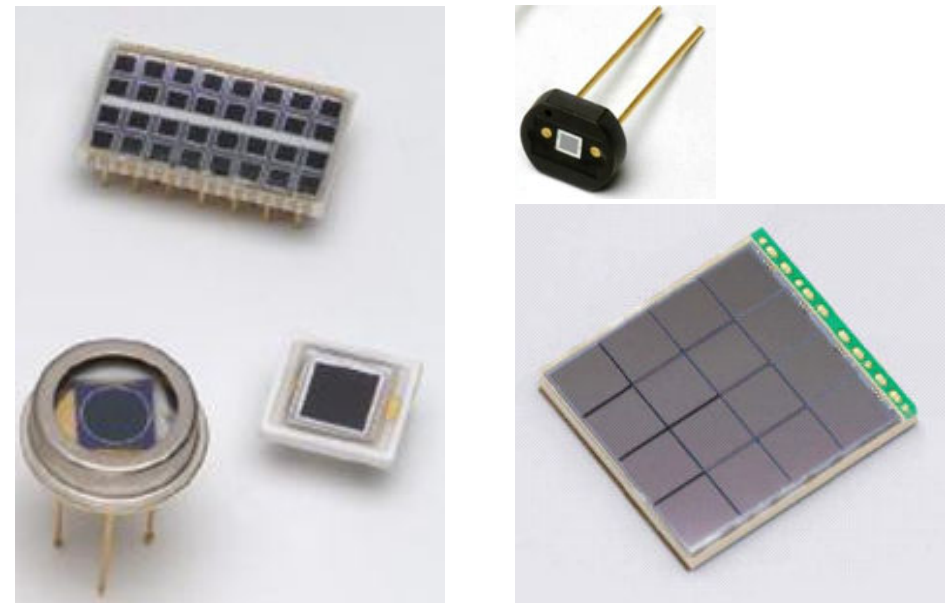


Photo detector

Silicon Photo Diode(PD)

Silicon Avalanche Diode(APD)

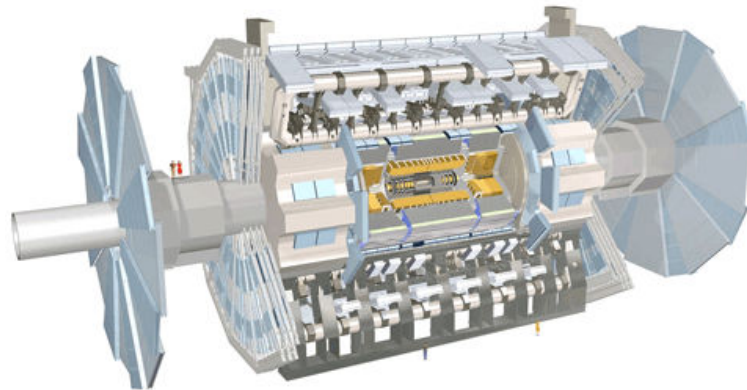
Multi Pixel Photon Counter(MPPC)



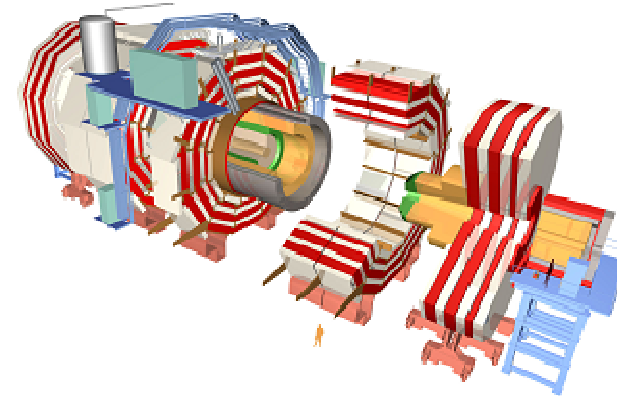
Current LHC detector

many HPK sensors have been used for LHC

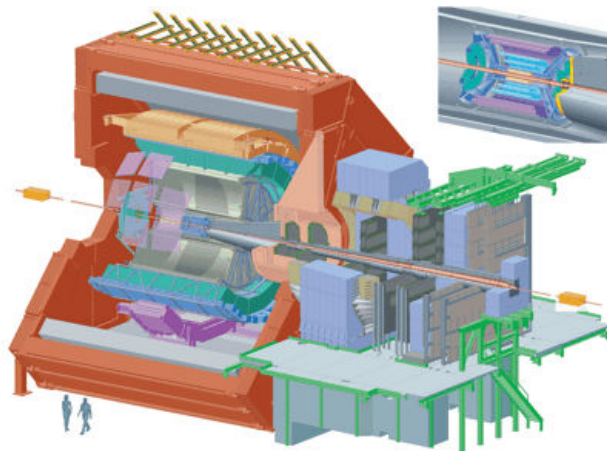
<ATLAS>



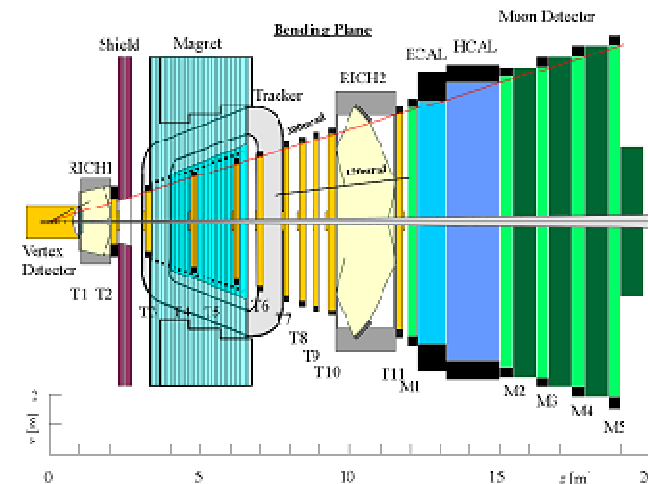
<CMS>



<ALICE>



<LHCb>



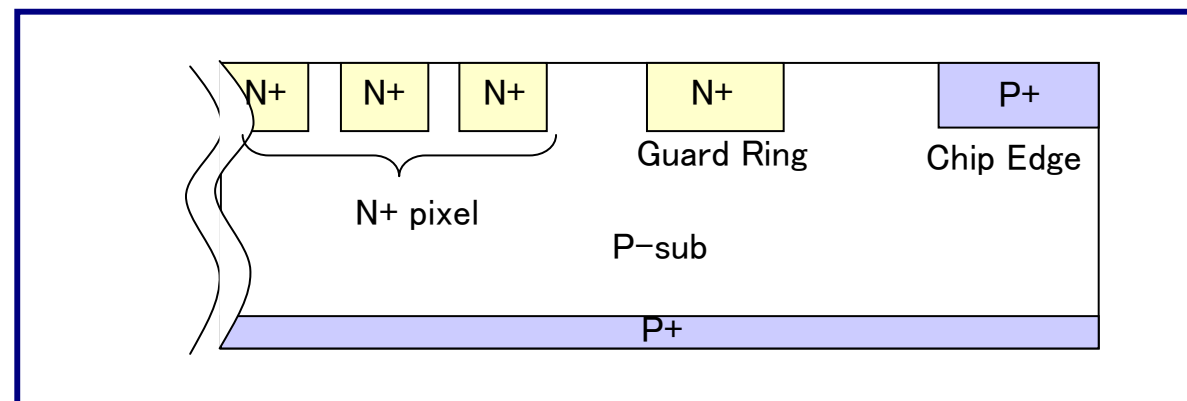
**very happy and proud to contribute such a big project !
and now developing new sensors for HL-LHC.**

PIXEL sensor for ATLAS-upgrade

Various type candidate

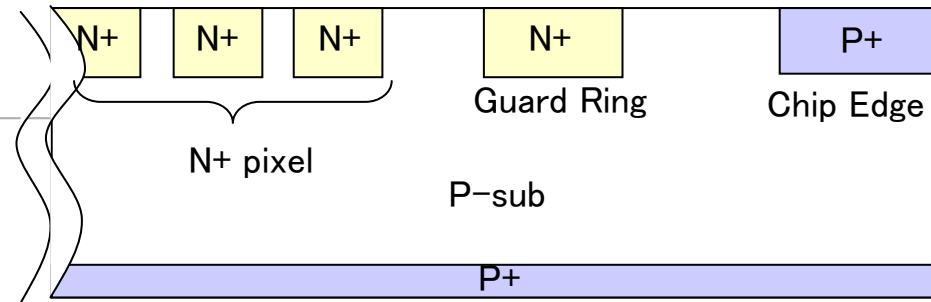
- N in N Planar
- 3D
- Diamond
- **N in P Planar**

We HPK suggest **N in P Planar Sensor**



N in P Planar Sensor

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Advantage

- Simple process (No backside-alignment needed) ⇒ Cost effective
- No type inversion ⇒ possible to partial depletion readout after irradiation
⇒ long life time

Disadvantage (under improvement)

- Slim edge
- Danger of sparks between chip and sensor
- Detection efficiency drop after irradiation

} today's talk

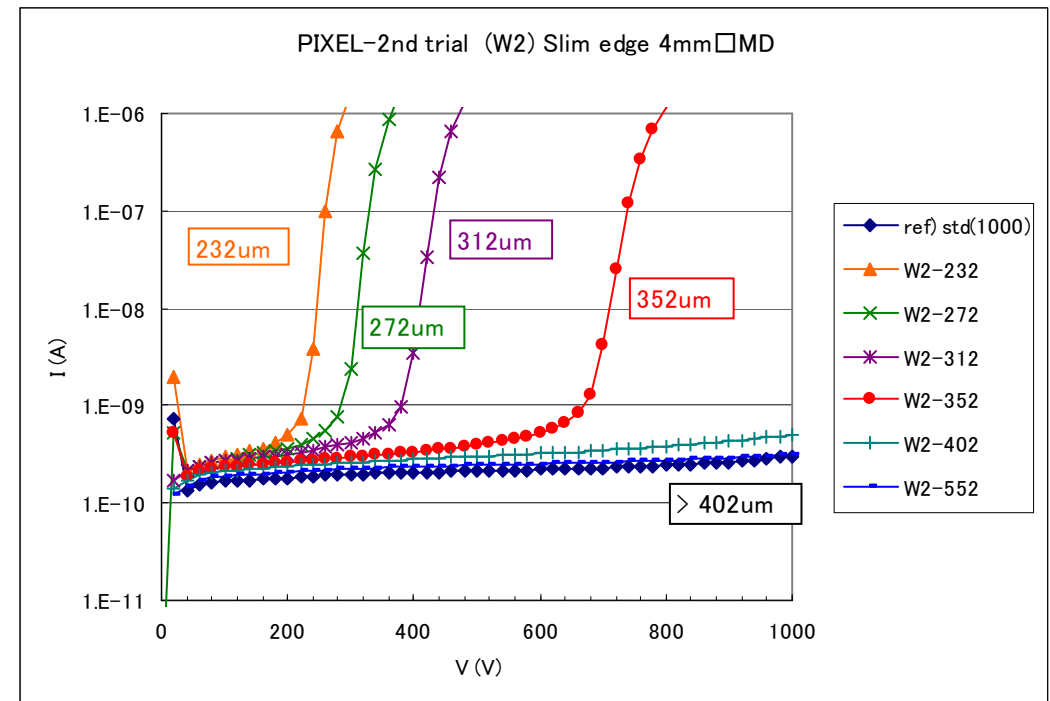
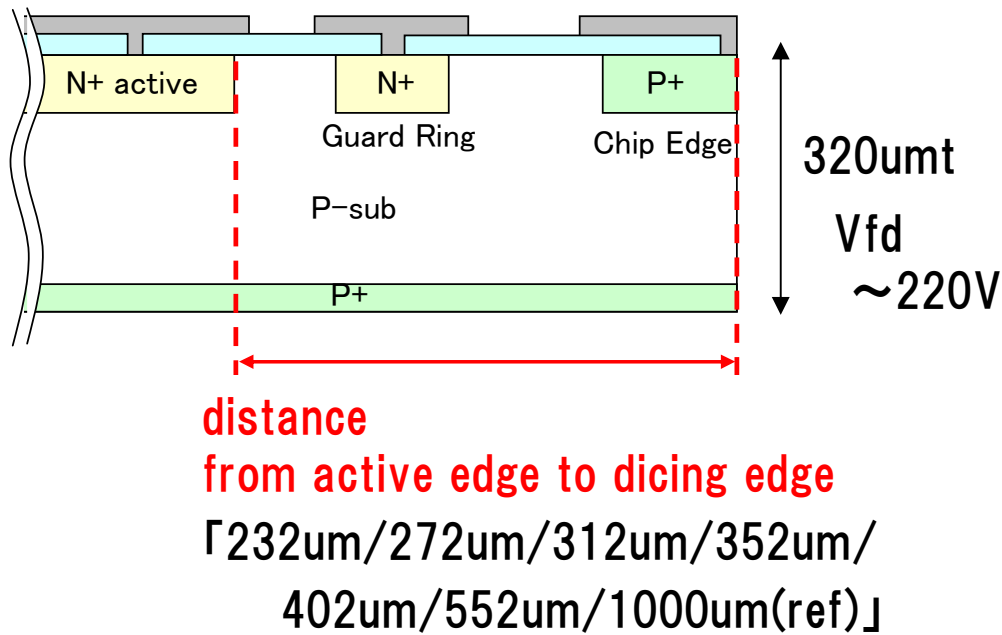
Development status

Novel Slim edge

previous result of slim edge (for reference)

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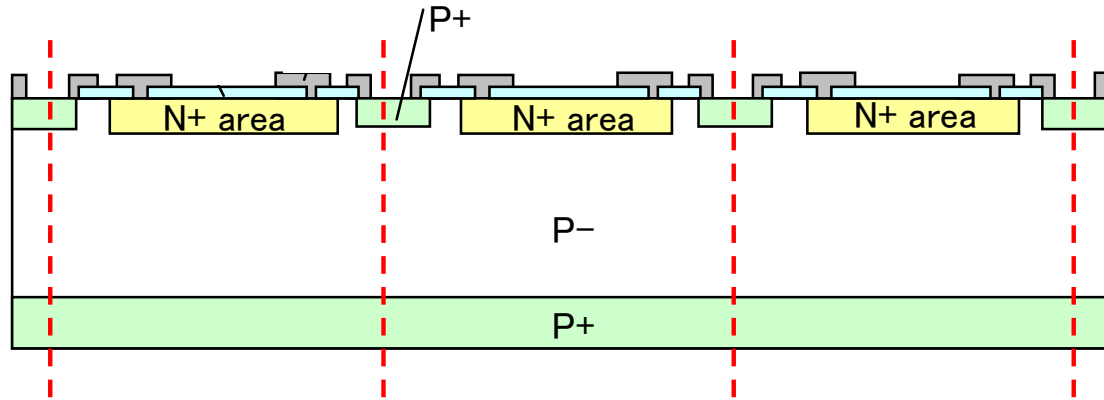
Shrunked edge distance (without side wall Al_2O_3 technology).



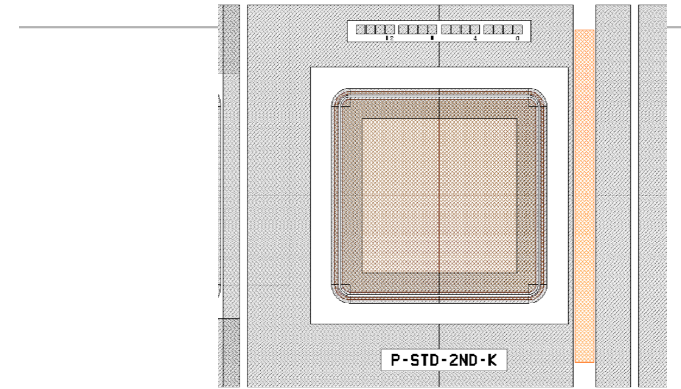
Needed about 400um edge distance to hold 1000V tolerance

Novel Slim edge (process)

Wafer Process as usual



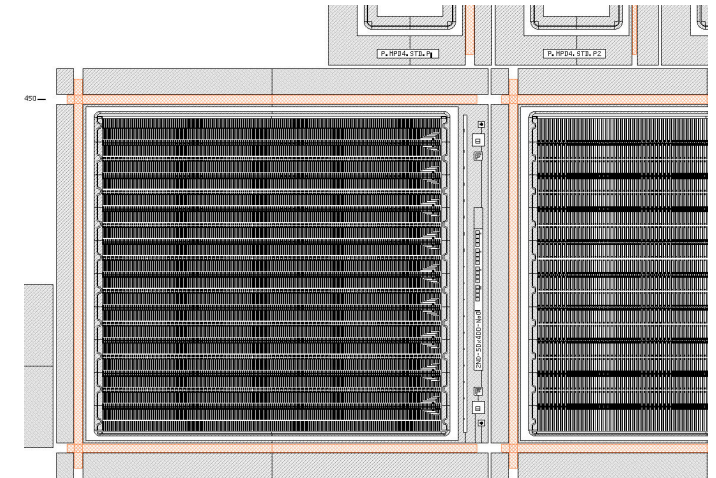
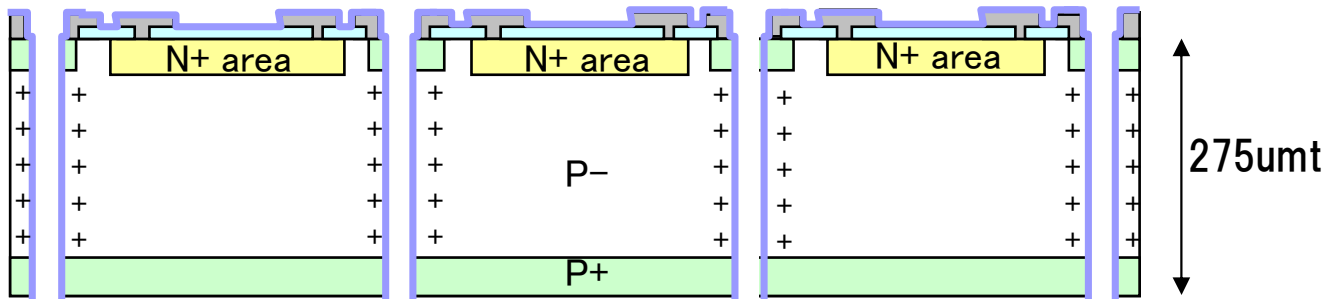
examples of design



1 side slim edge

And,

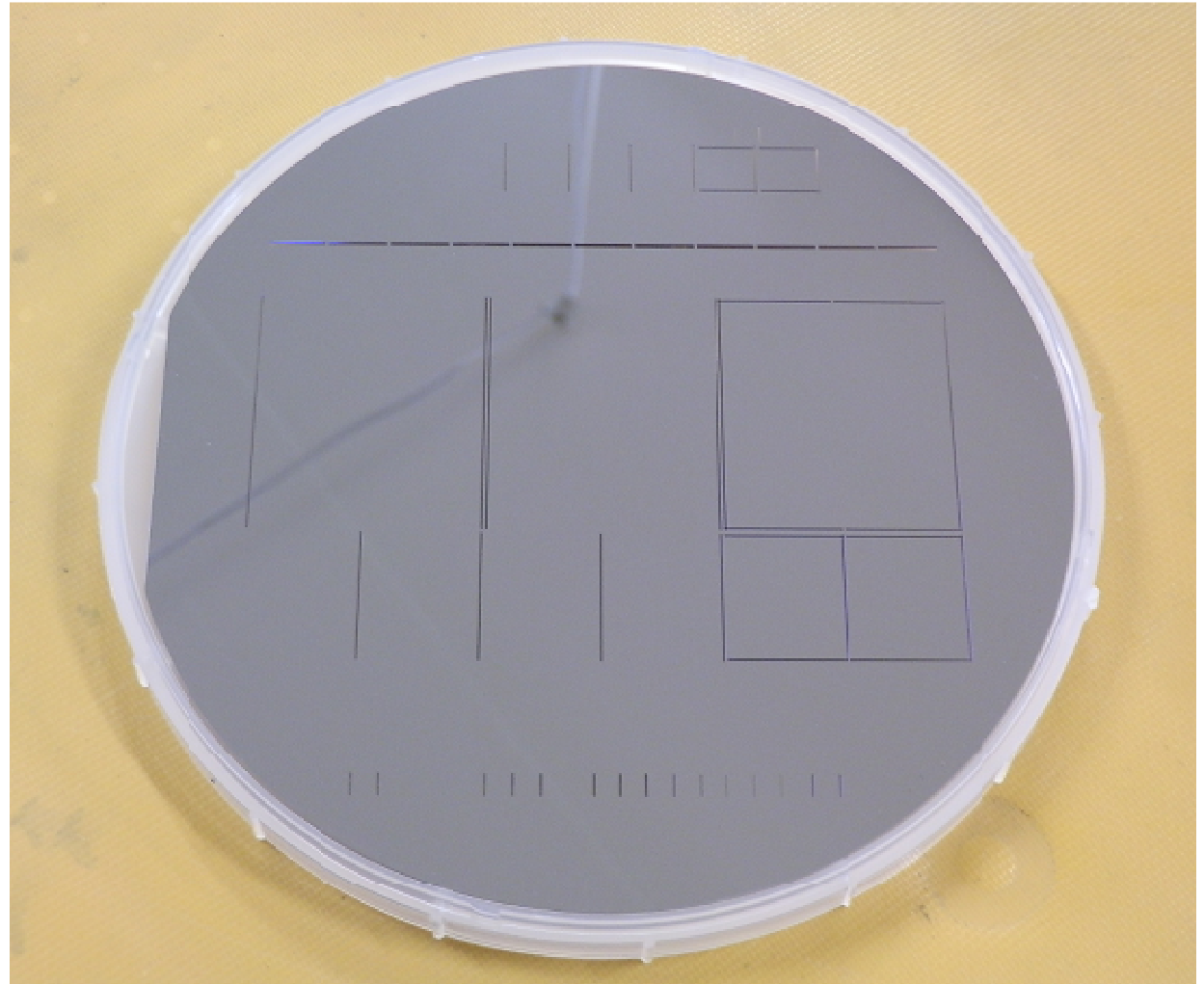
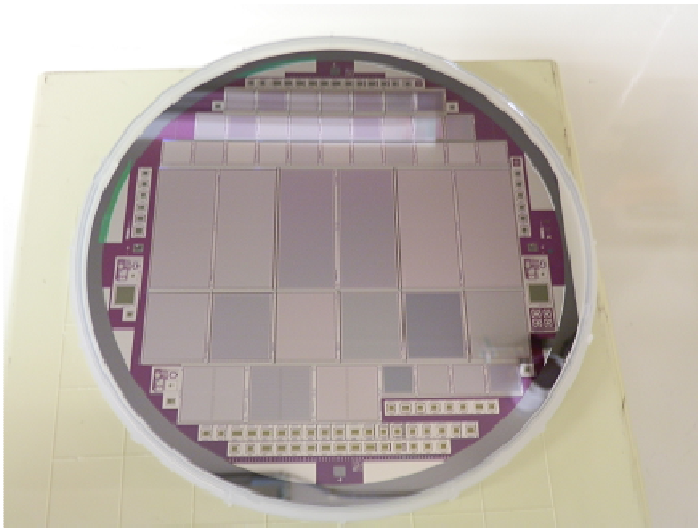
DRY etch penetration + AL_2O_3 coating



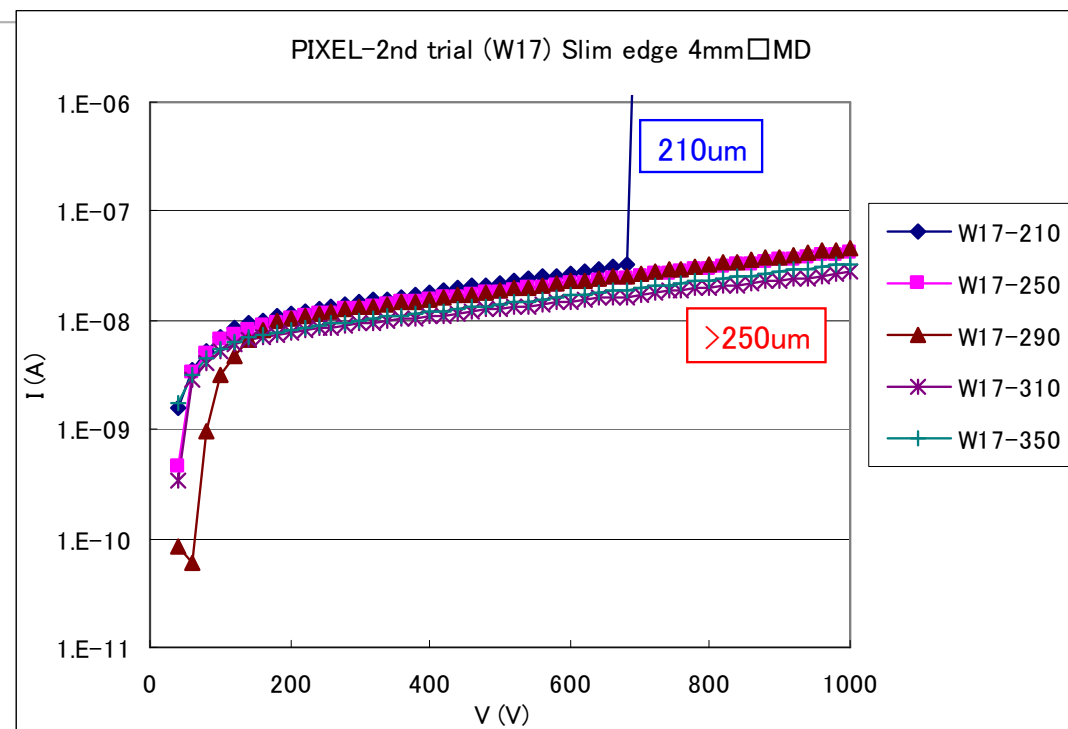
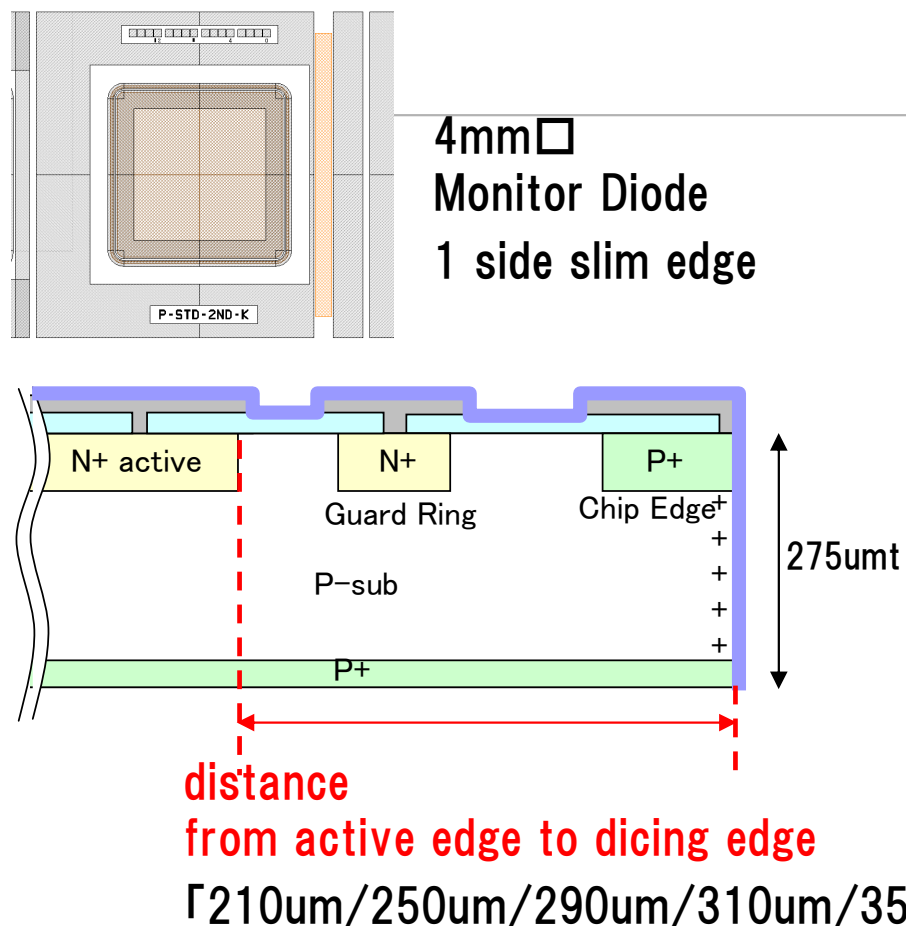
3 side slim edge

completing by only wafer process is important for mass production

Novel Slim edge (picture of wafer)



I-V results of Novel Slim edge — 1



- Achieved 1000V tolerance with about 250um edge distance.
- For 210um edge, breakdown occurred at 700V, however it might be induced by electric field of narrow PN gap, not edge leak.
- So, we have a possibility to achieve less than even 200um edge with 1000V tolerance by an optimum design. (It's next step)

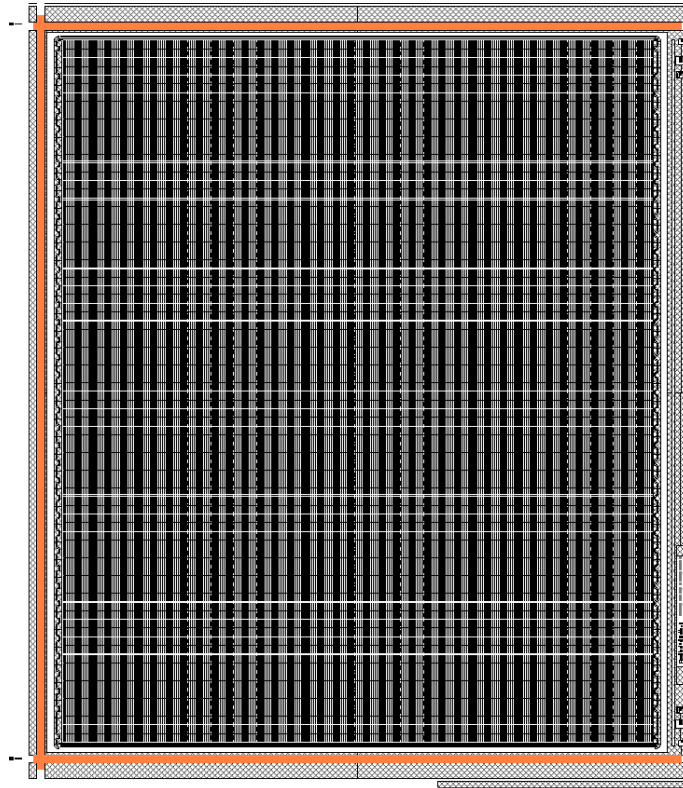
I-V results of Novel Slim edge –2

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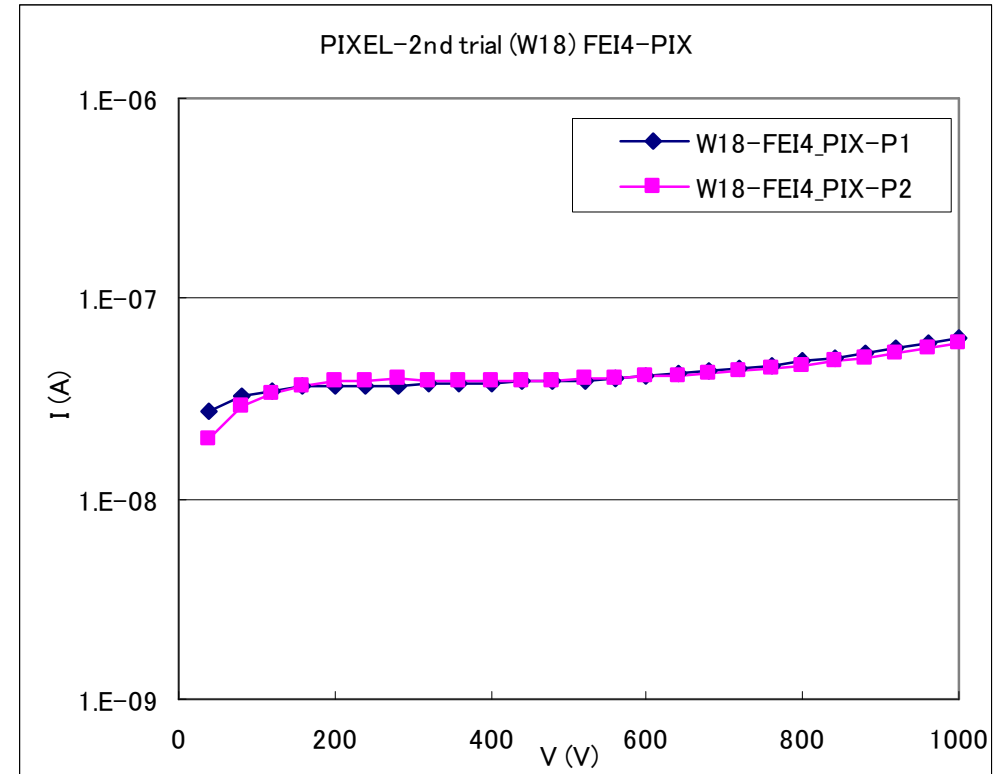
3 sides slim edge for about 20mm□ PIXEL sensor for FEI4 chip

310um slim edge

480um
slim
edge



310um slim edge



confirmed good I-V

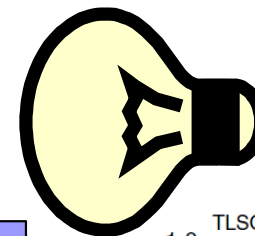
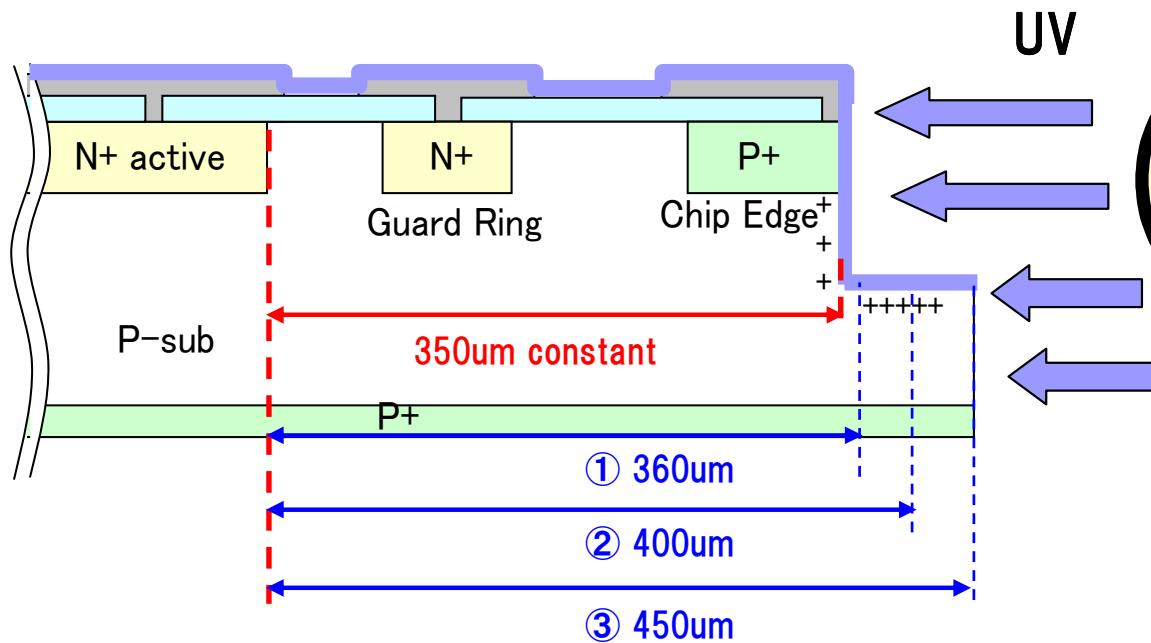
even with 3 sides slim edge of real size PIXEL sensor

Reliability test of Novel Slim edge (=UV irradiation)

Ideally we should do irradiation test assumption for HL-LHC.

KEK did 70MeV proton irradiation on July , the result will come soon , next time.

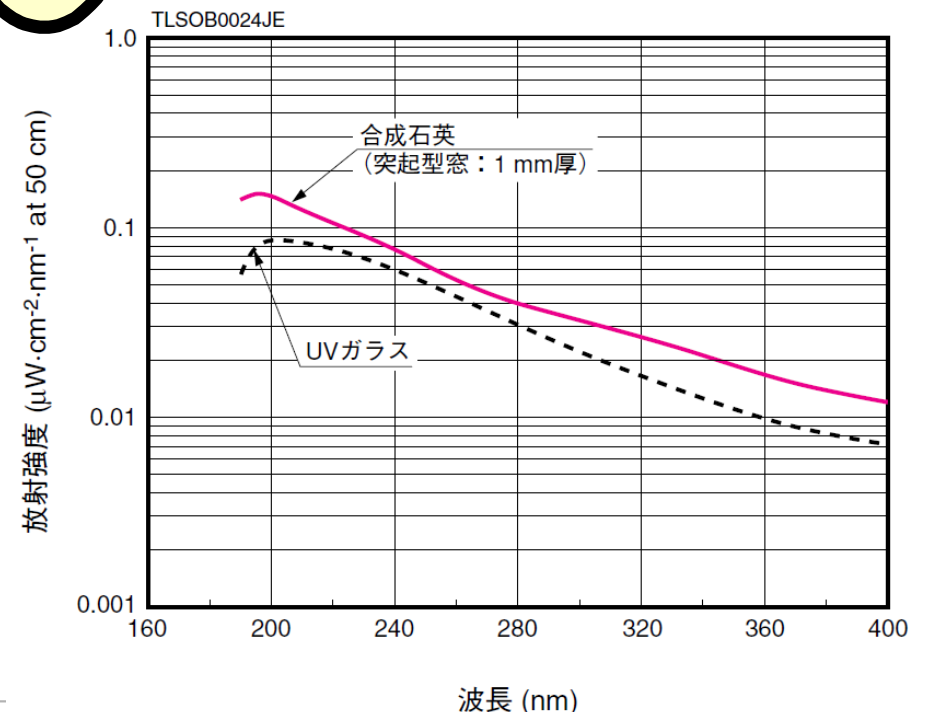
Instead, we did Ultra Violet irradiation for easy test.



D2 Lamp condition
($\lambda_p=200\text{nm}$ 、6cm distance)

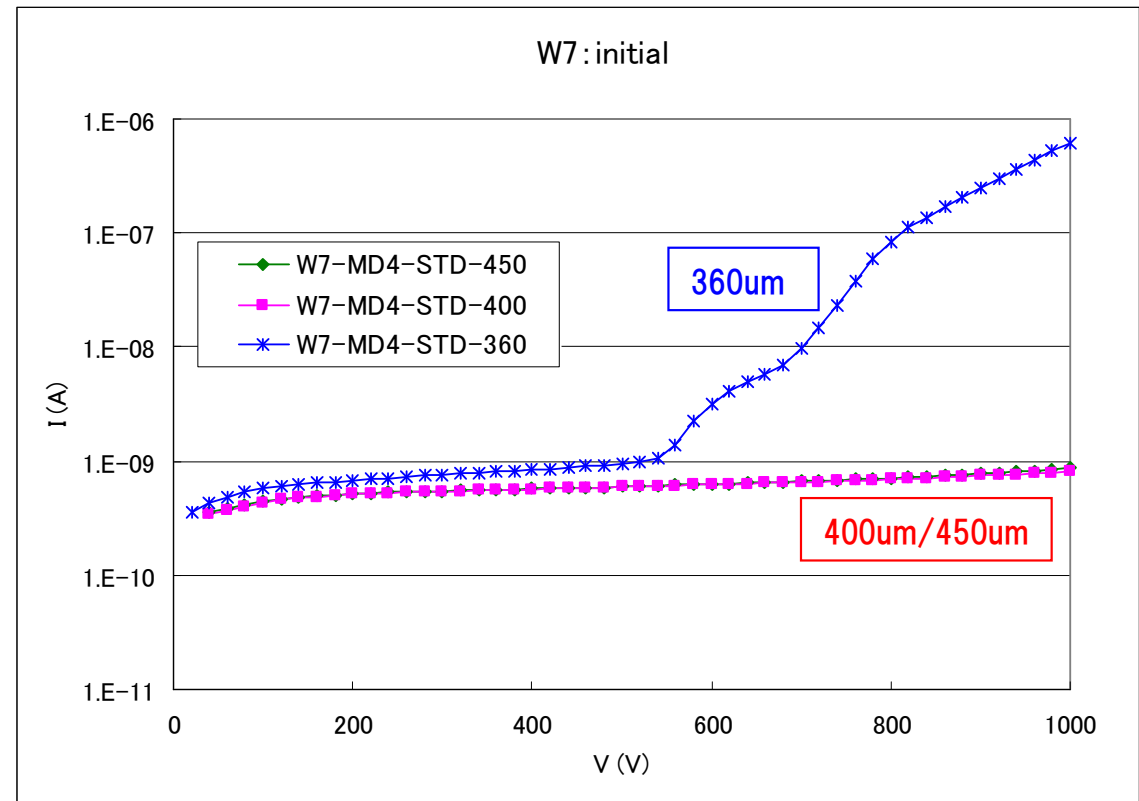
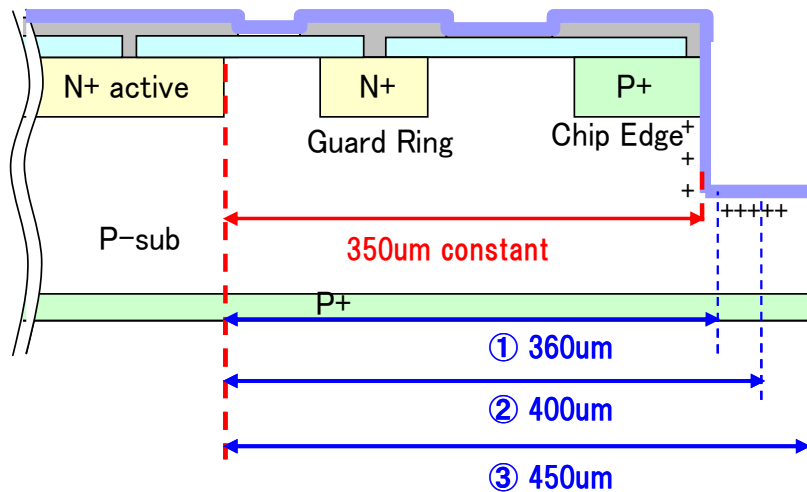
4mm \square Monitor Diode
1 side slim edge

3 types dicing edge
(by Stealth Dicing)



Reliability test of Novel Slim edge (=UV irradiation)

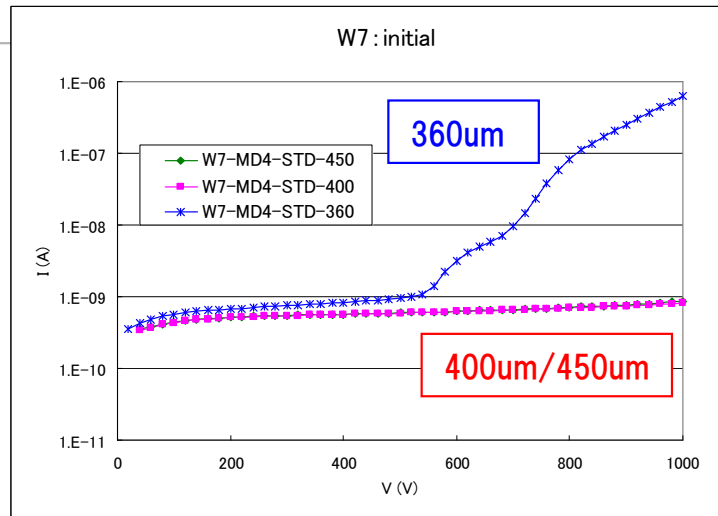
I-V before UV irradiation



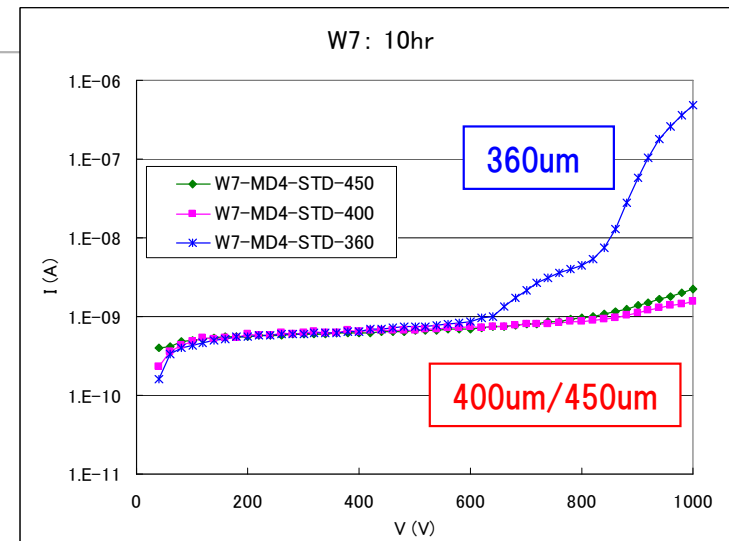
- indicates Al_2O_3 interface charge effect
- numerous leakage current flows after depletion region touch the dicing edge

Reliability test of Novel Slim edge (=UV irradiation)

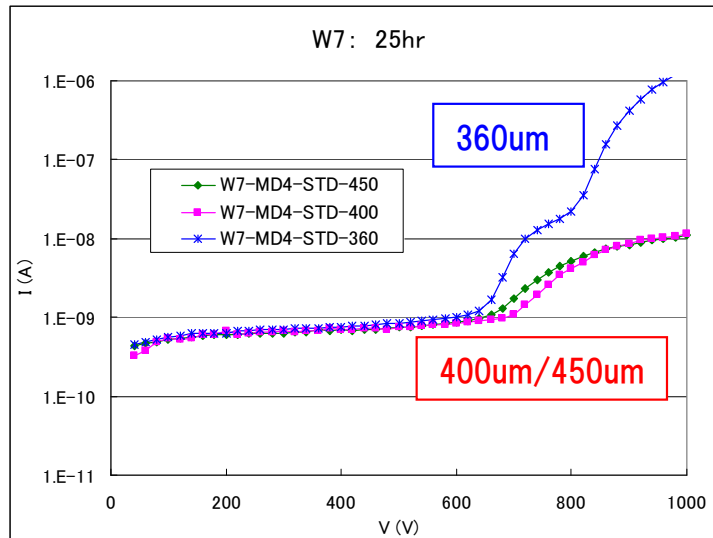
initial



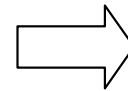
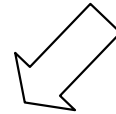
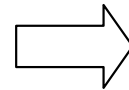
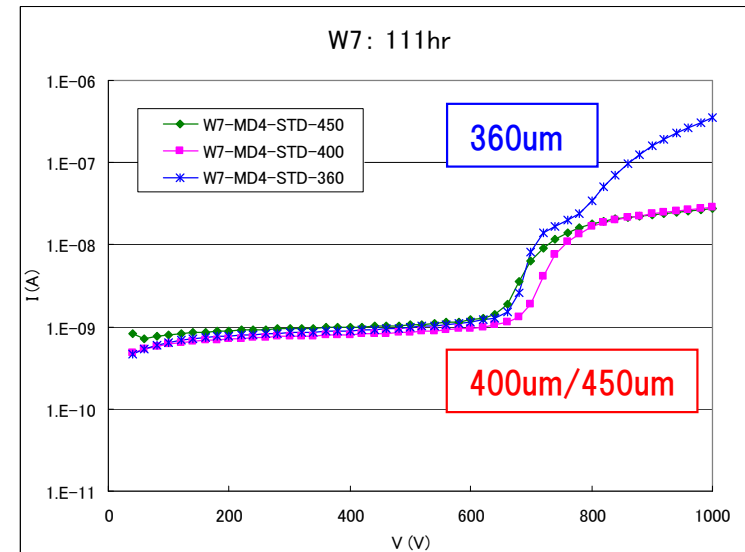
10hr



25hr



111hr

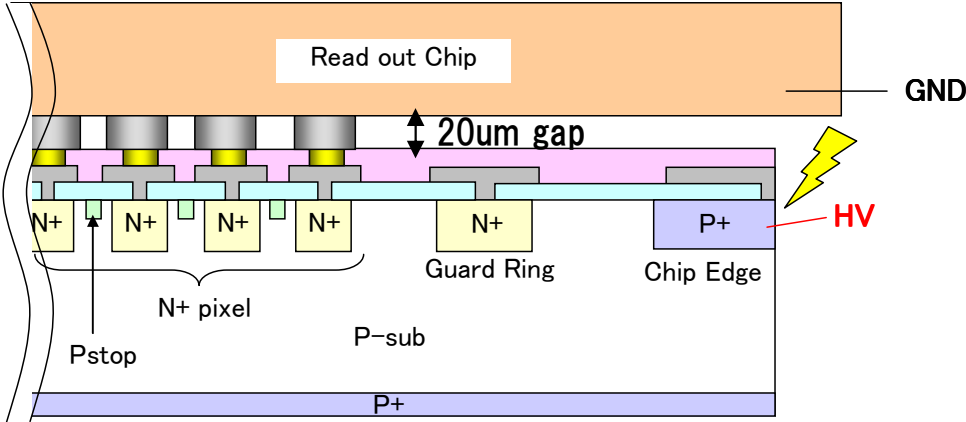


Development status

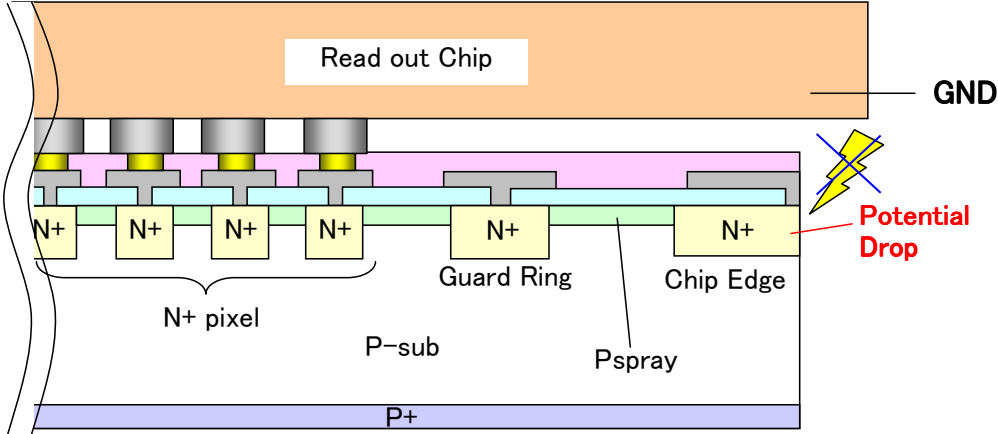
Edge Spark Protection

edge spark protection

conventional type



proposal type

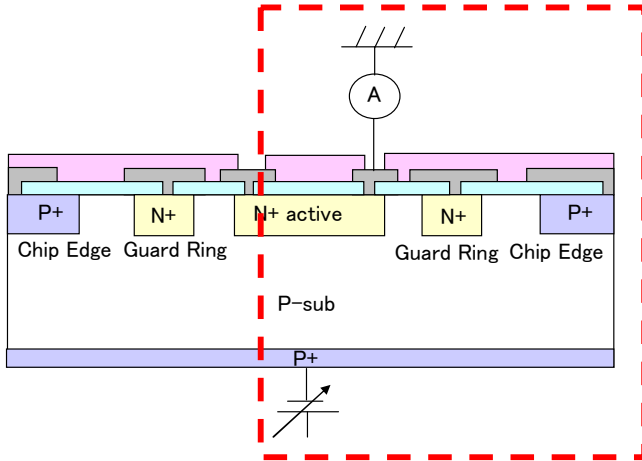


We suggest edge N+ design

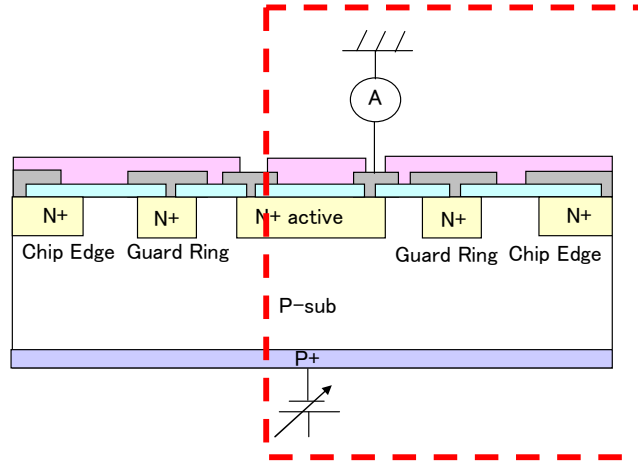
simulation result of edge potential

simulation region

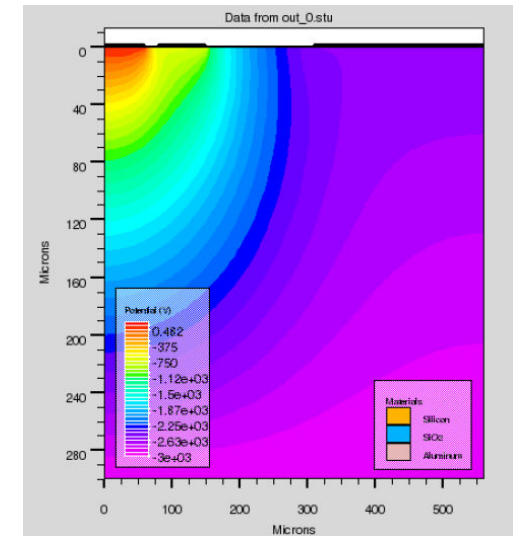
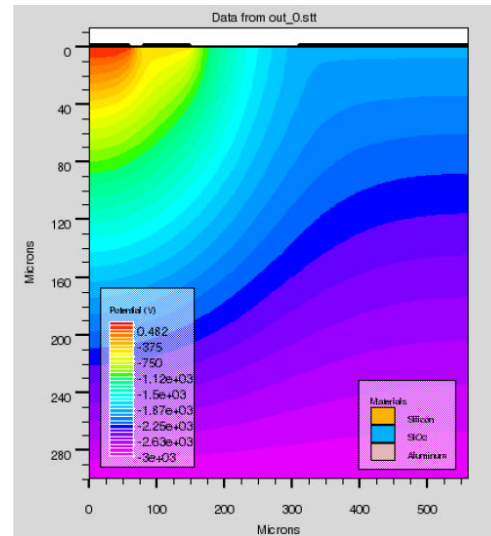
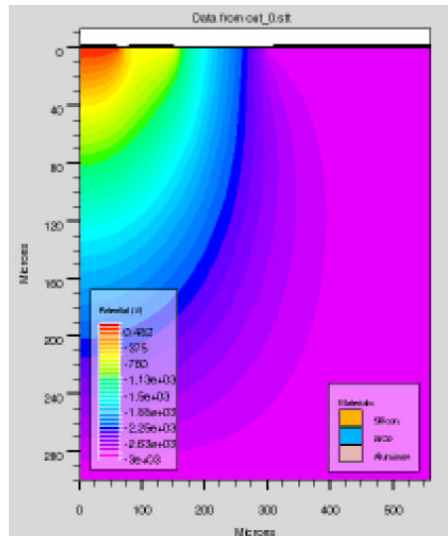
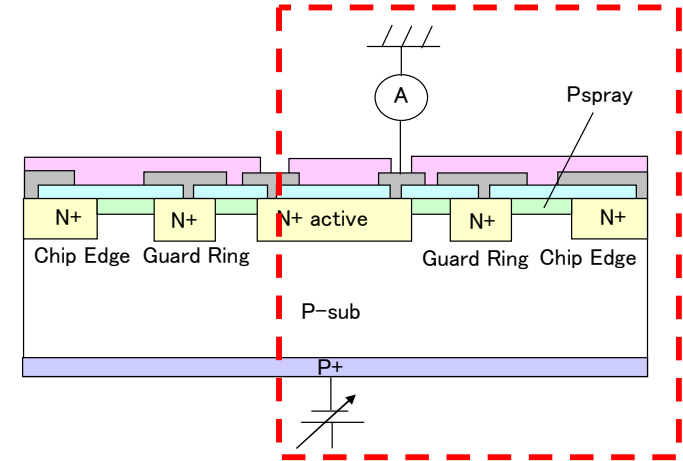
① P+edge (std design)



② N+edge (non isolation)



③ N+edge (with Pspray)

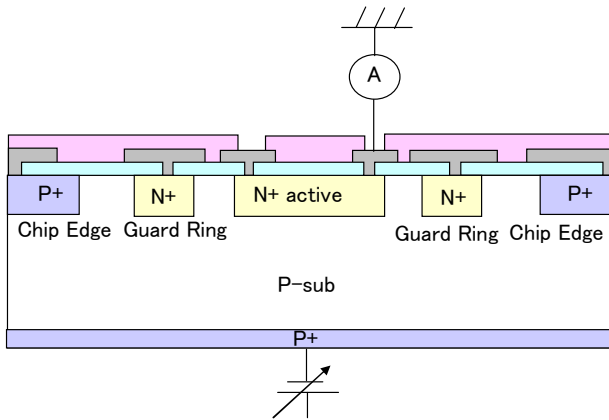


chip edge potential dropped

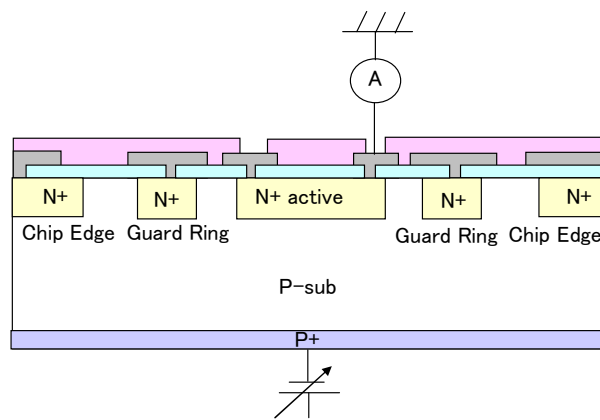
chip edge potential dropped

edge spark protection I-V test for 4mm□ MD

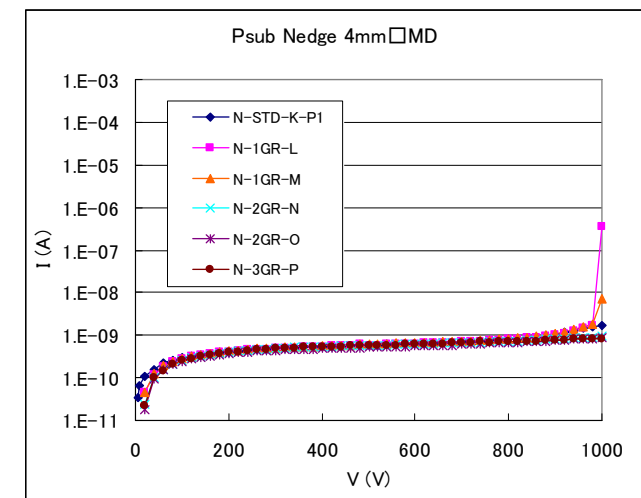
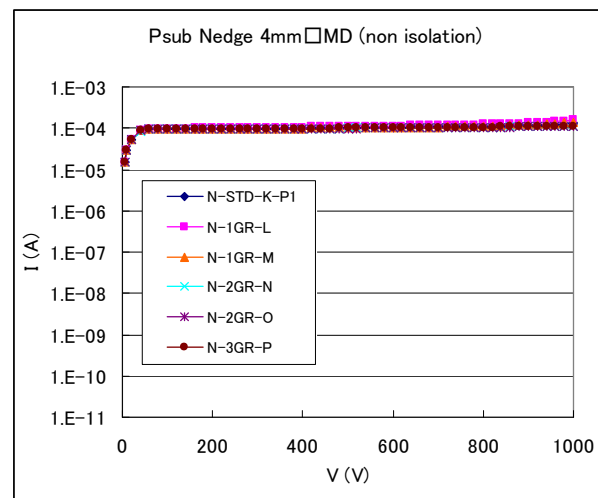
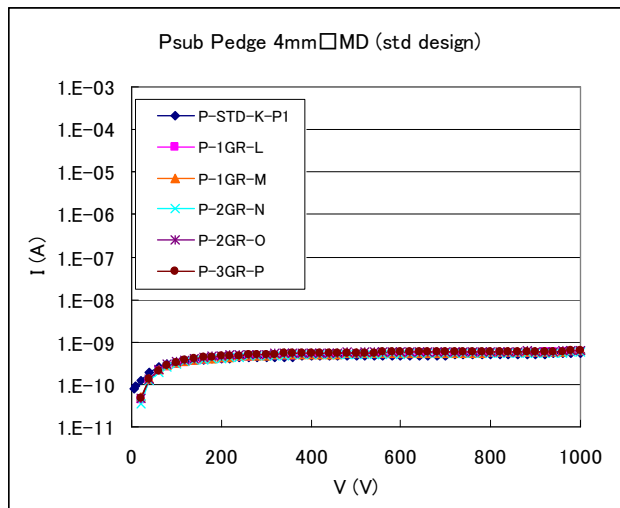
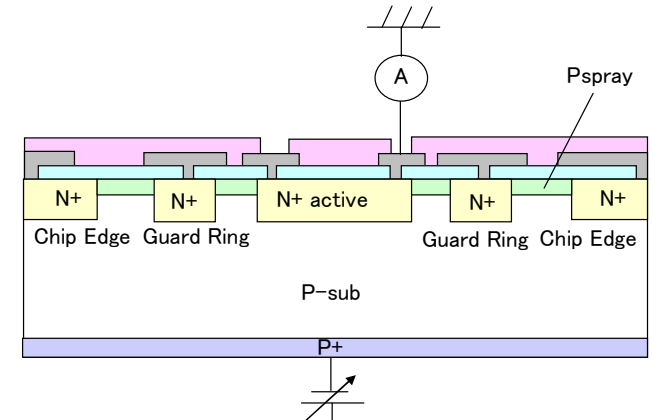
① P+edge (std design)



② N+edge (non isolation)



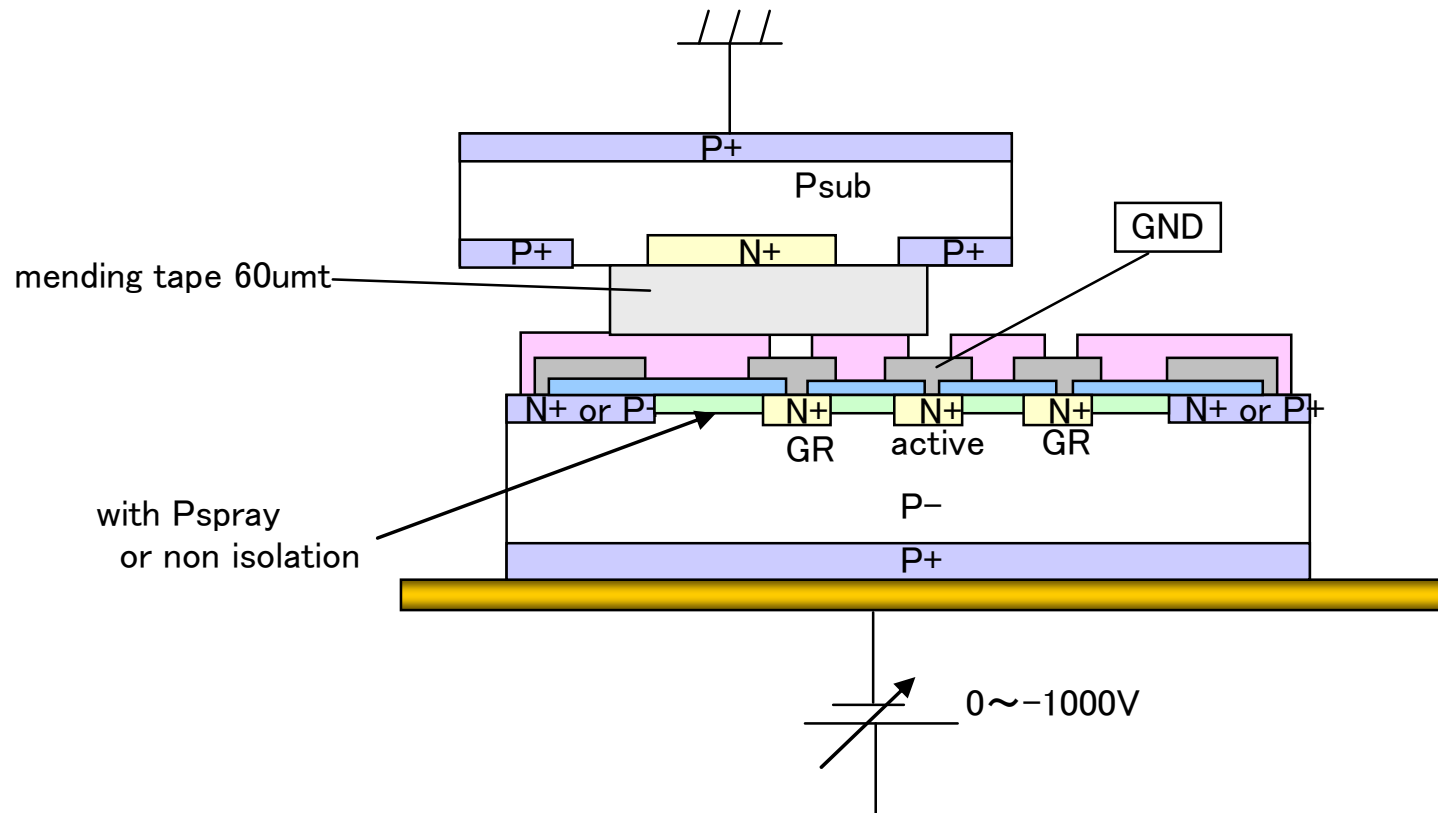
③ N+edge (with Pspray)



large leak current from chip edge

almost same as P+edge type

easy test for edge spark protection



type	result 1	result2
① P+edge (std design)	spark @ 740V	spark @ 780V
② N+edge (non isolation)	non spark up to 1000V	non spark up to 1000V
③ N+edge (with Pspray)	spark @ 960V	spark @ 980V

This result implies the possibility of edge N+ type goes well for edge spark protection

-
- We, HPK have been developing high radiation-tolerant n in p planar pixel sensors which can be used for HL-LHC.
 - For slim edge, we applied Al_2O_3 sidewall passivation technology to wafer process and achieved less than 250um edge, and have a possibility of less than 200um with 1000V tolerance by an optimum design. (It's next step)
In reliability test, Al_2O_3 interface charge looks disappeared after UV irradiation. We'll continuously check the reliability.
 - For edge spark protection, we suggested edgeN+ and isolation structure. We will obtain the result within this year.

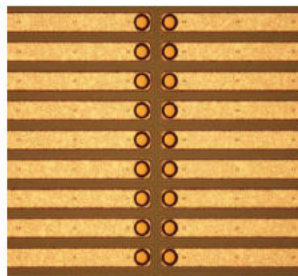
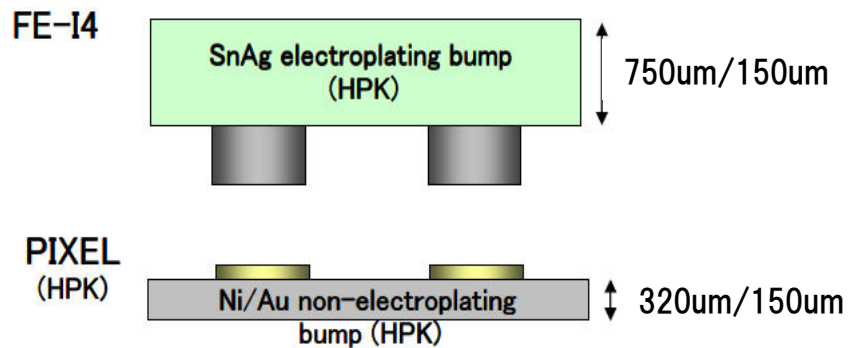
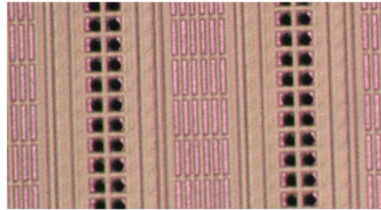
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Back up

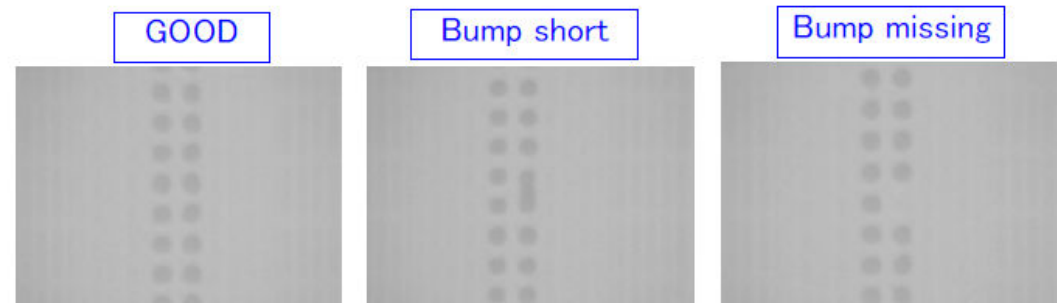
assembly (making bump and Flip chip bonding by HPK)

achievementspast records

	FEI4	PIXEL sensor	
1	750umt	320umt	done
2		150umt	done
3	150umt	320umt	done
4		150umt	plan to 2013/10



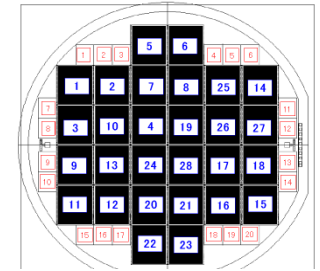
evaluation of FEI4(750um) – PIXEL(150umt)



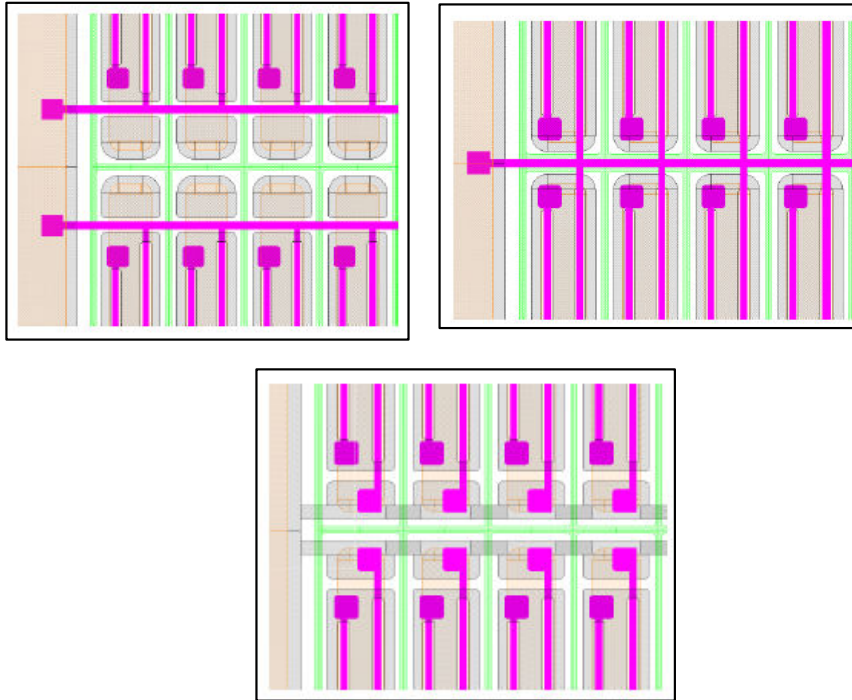
Most of bumps(>about 99.8%) look "GOOD".
But, some of bumps have short or missing.
We are trying to improve the yield.

Plan to 150um – 150um real sensor assembly
and going to thermal cycle test, within this year.

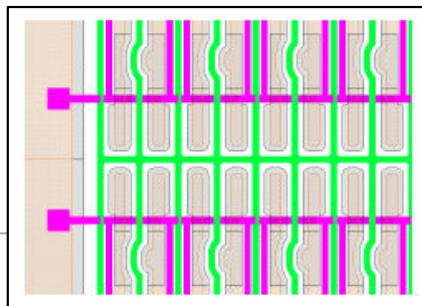
Detection efficiency drop after irradiation



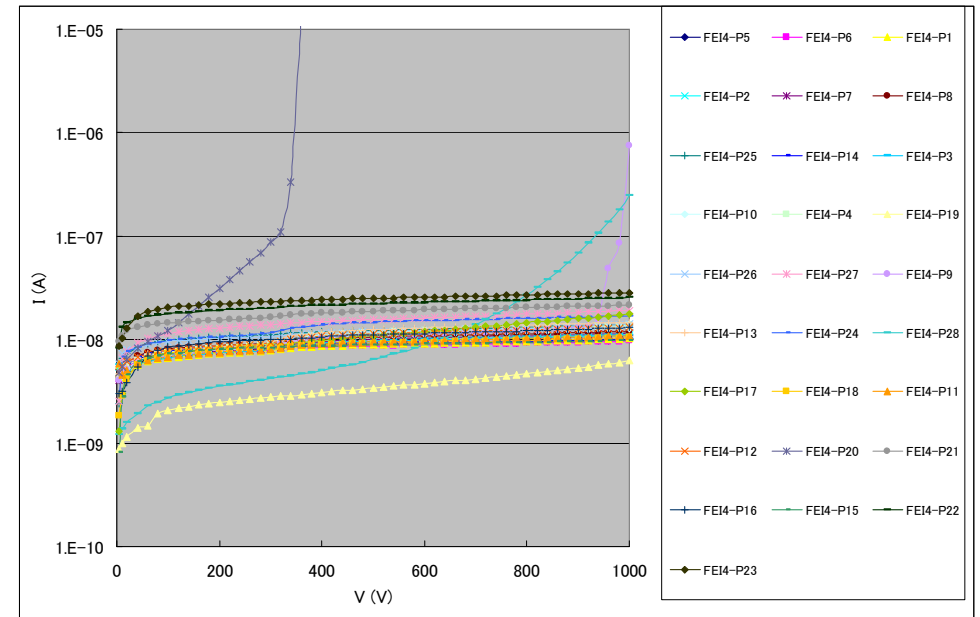
new mask design



-
- and
- 25um pitch type



prompt report of wafer I-V (320umt)



Work plan

- 150umt type : under process
- bump bonding : by HPK
- irradiation and efficiency evaluation
⇒ask for KEK