Measurements of Low Gain Avalanche Detectors (LGAD) for High Energy Physics applications

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Silicon Detectors with Internal Gain and Proportional Response

Tracking Detectors

☐ **PiN based Diodes**

- → **Proportional Response**
- → **Good efficiency**
- → **Good spectral range**
- → **Segmentation is technologically available (strip and pixel detectors).**

After Irradiation:

- ✗ **Worse signal to noise ratio (lower quality signal + noise increment)**
- ✗ **Increment of the power consumption**
- ✗ **Radiation damage.**

Why Low Gain?

Internal Gain

☐ **Low Gain Avalanche Detectors (LGAD)**

- → **Proportional Response (linear mode operation)**
- → **Good efficiency**
- → **Good spectral range**
- ✓ **Better Sensibility**
- ✓ **Thin detector integration with the same signal and higher collection efficiency**
- ✓ **Better signal/noise ratio**

After Irradiation

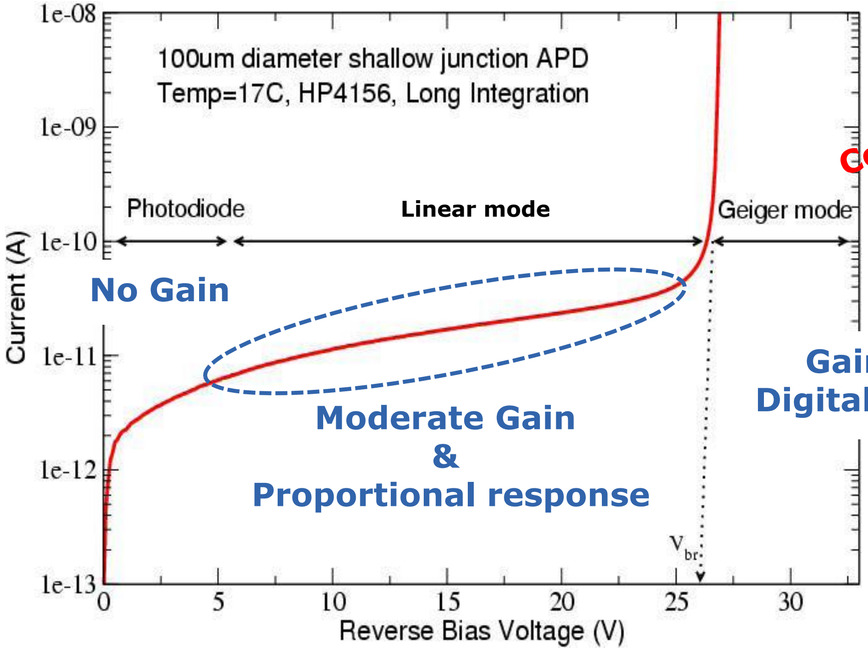
- ✓ **Similar pre & post irradiation signal (higher quality signal + lower noise increment)**
- ✓ **Lower increment of the power consumption**

- ☐ **High Gain implies higher levels of multiplication noise (inherent to the stochastic process of multiplication), spoiling the improvement of the Signal to Noise ratio.**
- ☐ **Collection times are increased with gain (more charge to be collected), increasing the trapping efficiency and avoiding the off-setting of the charge loss.**
- ☐ **Avoid cross-talk among adiacent pixels/strips.**

Linear Mode Operation. Gain Definition

- **Diodes with multiplication** can operate in Linear or Geiger mode
  - **Linear** mode: Moderate gain & Proportional response
  - **Geiger** mode: Very high gain & Digital response

Gain Definition



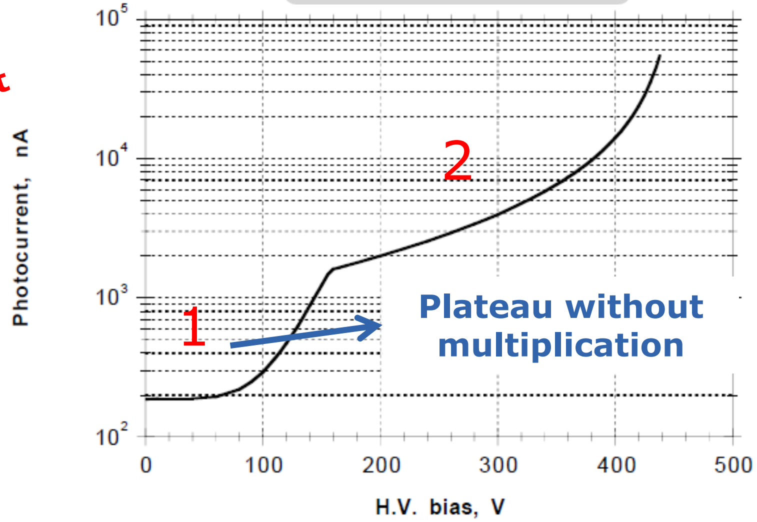
No Gain

Moderate Gain & Proportional response

Gain > 10^4 Digital response

[1] A.G. Stewart et al. in Proc. of SPIE, Vol. 6119, 2006

Continuous light illumination

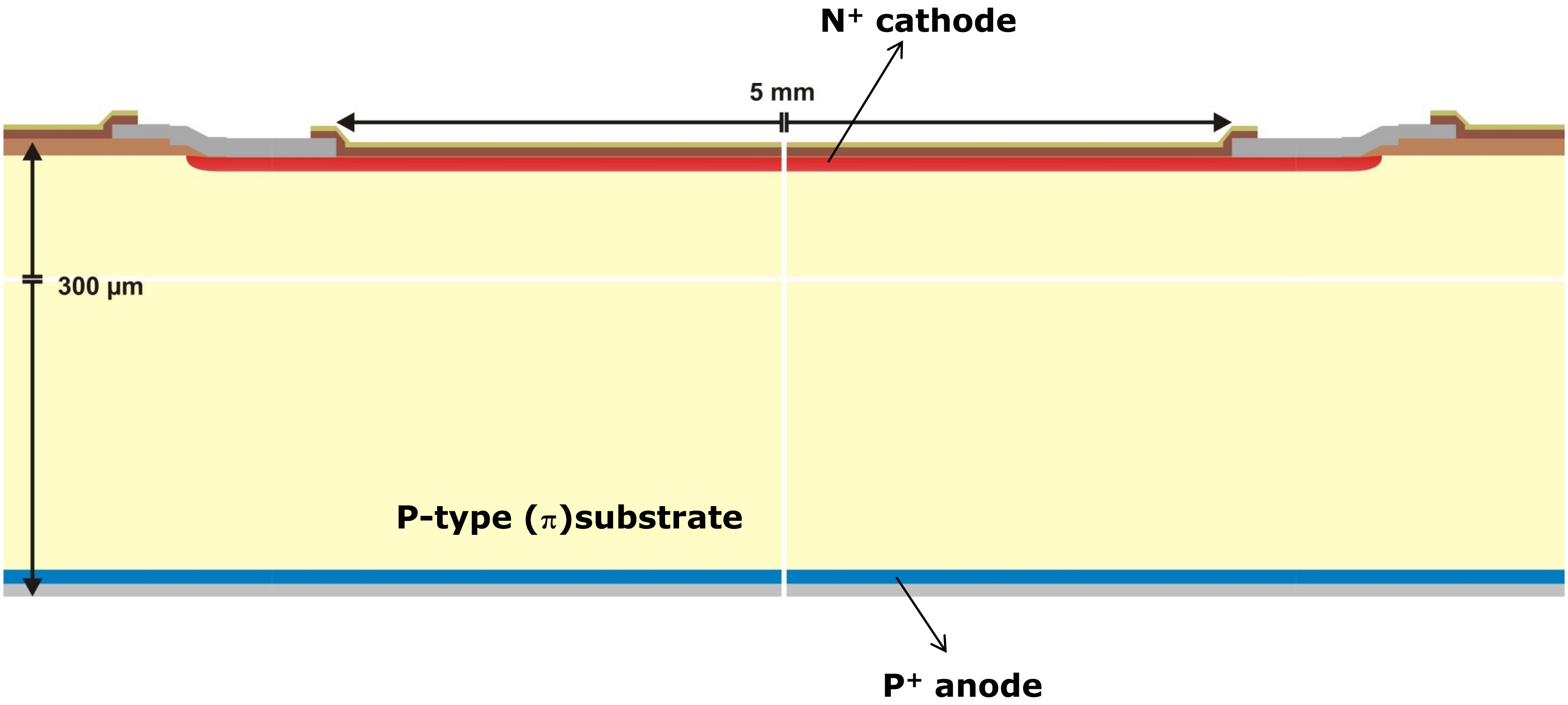


Plateau without multiplication

I. Tapan ,et al. NIMA 388 (1997) 79-90: “The plateau for low bias voltage may be taken to correspond to unit gain […] and the gain for higher bias measured simply as the ratio of the pulse size to that plateau”

Pad Diodes with internal Gain

- ☐ **M. Bruzzi, IEEE TNS-48(4) 2001: "The general approach followed by the HEP community in radiation–damage studies has been to investigate the radiation effects in silicon detectors using the simplified geometry of a single pad detector."**



Pad Diodes with internal Gain

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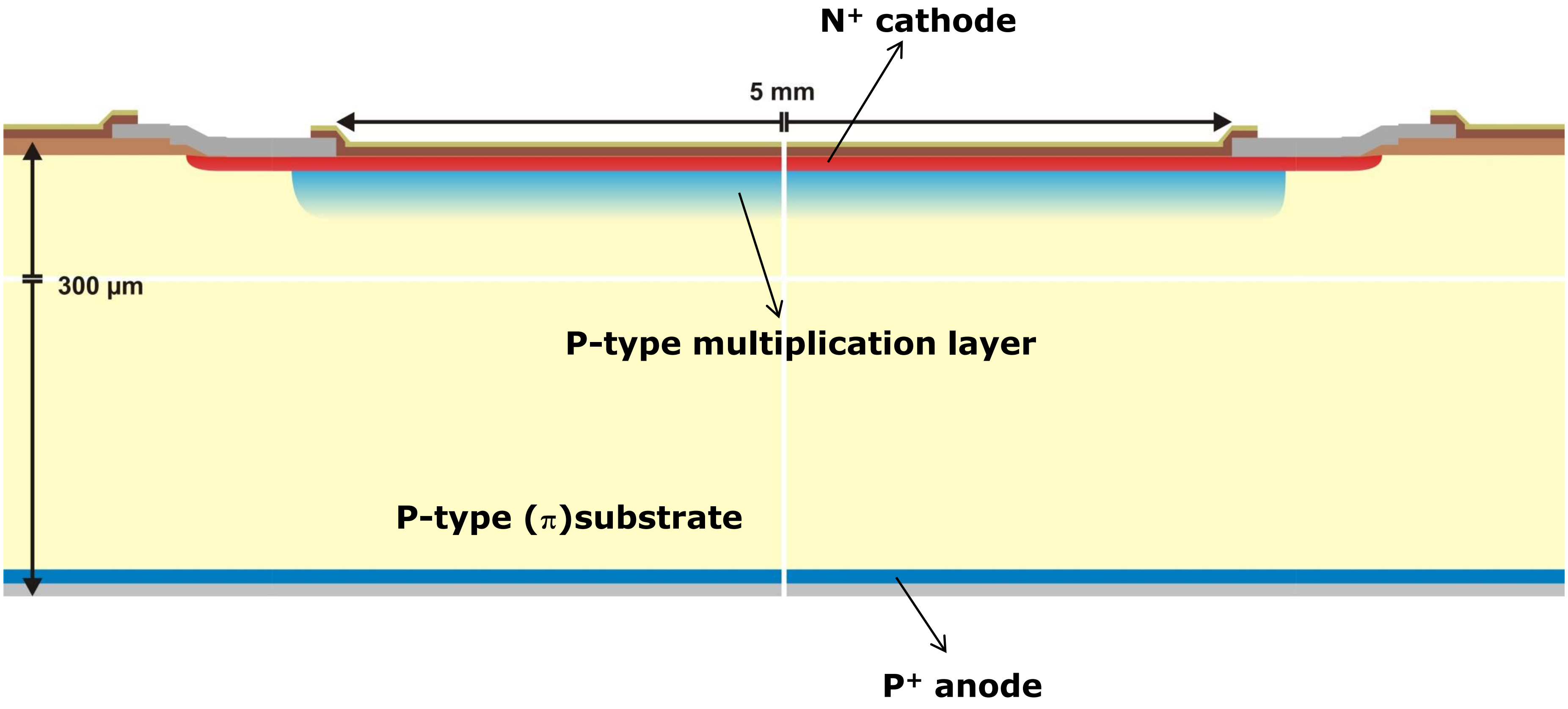
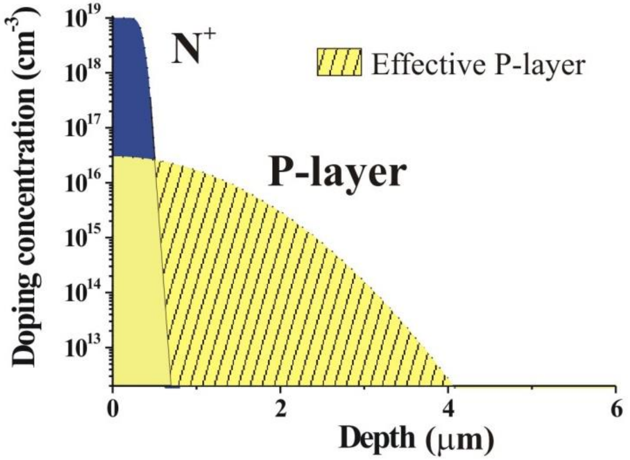


Design of the Multiplication Region

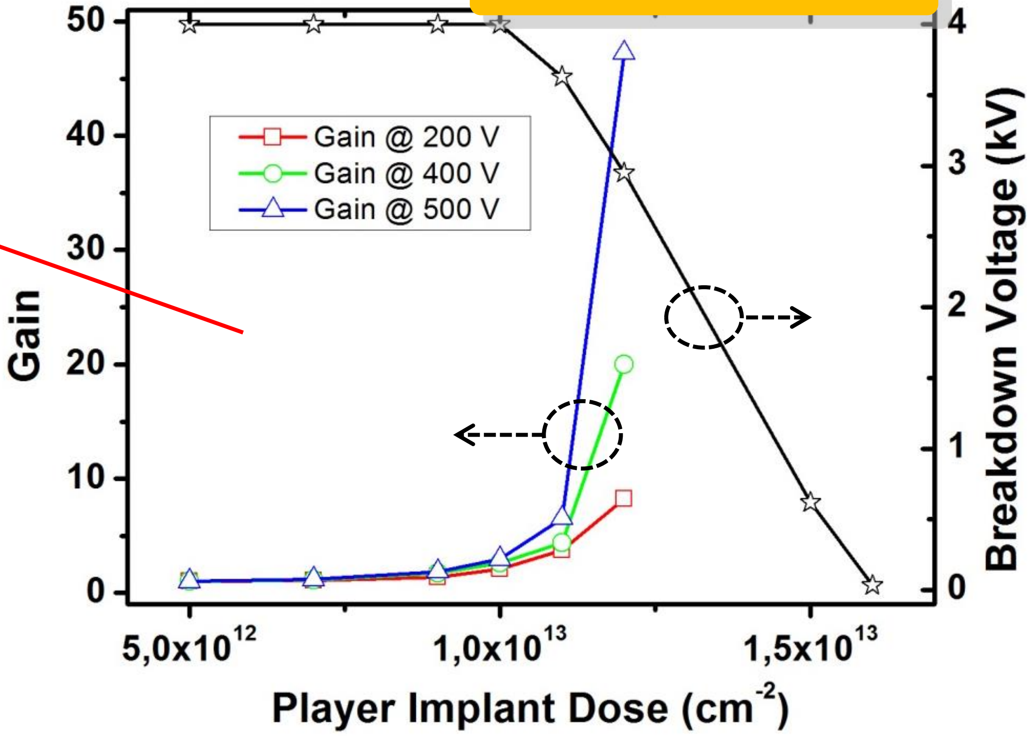
Gain/V_{BD} trade-off

✓ If implant dose increases:
  - Gain increases
  - V_{BD} decreases

☐ **Technological adjust of the multiplication region p-layer becomes critical.**



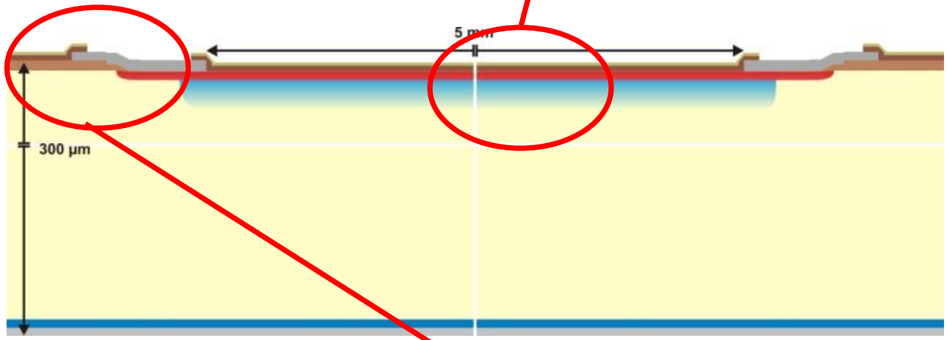
1D Simulation @ Pad Centre

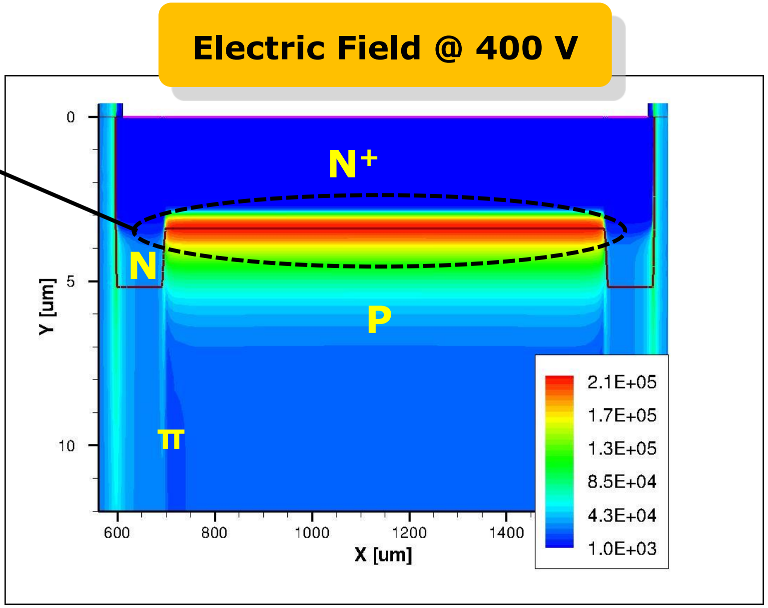


Small modifications in the Boron implant dose (~ 2 × 10^{12} cm^{-2}) induce great changes in Gain and V_{BD}

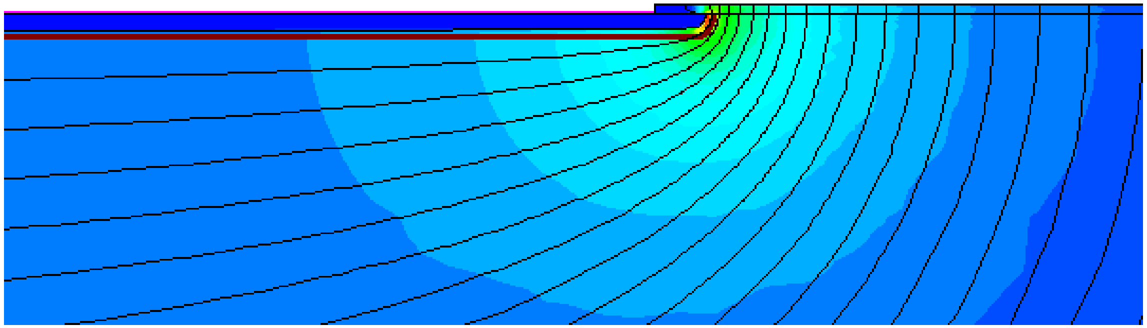
Design of the Edge Termination

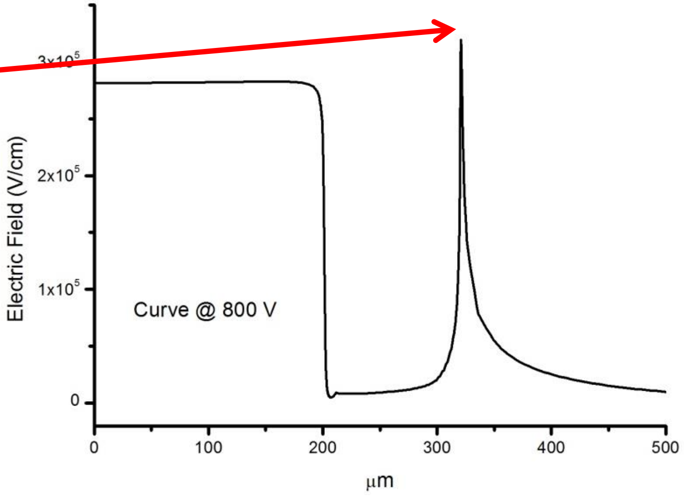
Planar and uniform electric field distribution, high enough to activate charge multiplication




Electric Field @ 400 V

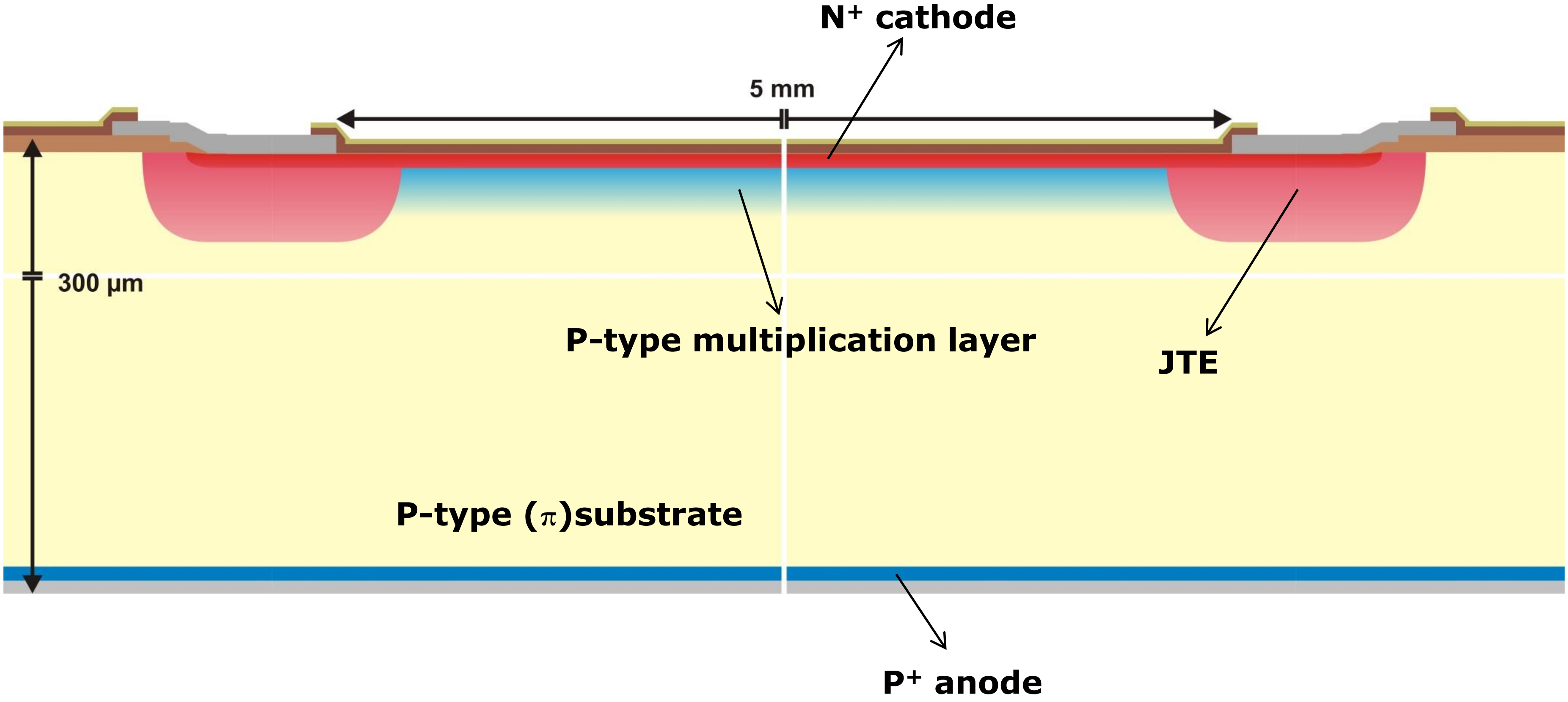
$$V_{BD}|_{Central} \ll V_{BD}|_{Termination}$$





Design of the Edge Termination

- ☐ **Junction Termination Extension** **(JTE). Peripheral low doping N-well to increase the voltage capability of this area, reducing the Electric Field in the periphery, allowing the maximum Electric Field is reached in the multiplication area (N^+/P junction).**



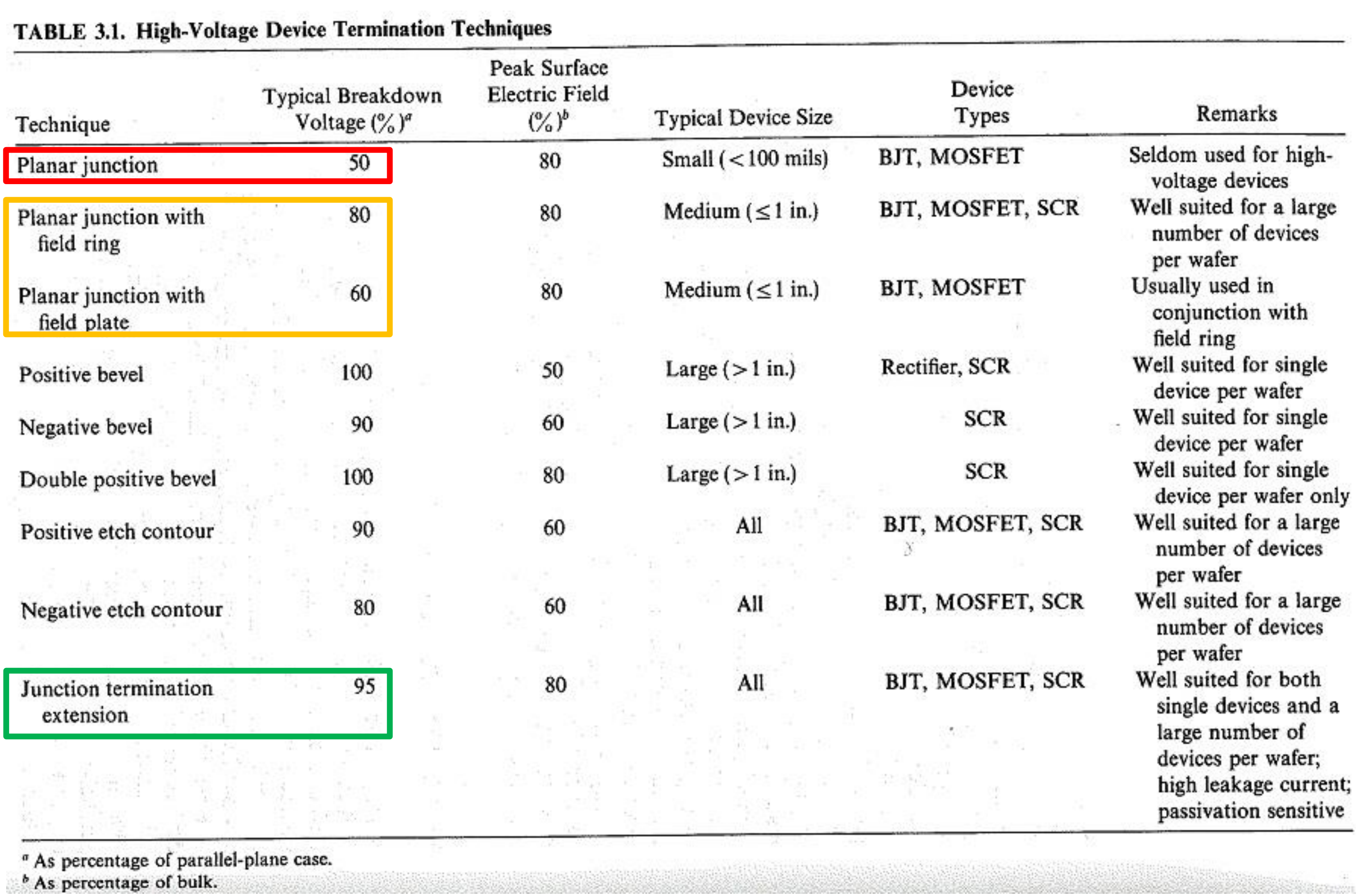


TABLE 3.1. High-Voltage Device Termination Techniques

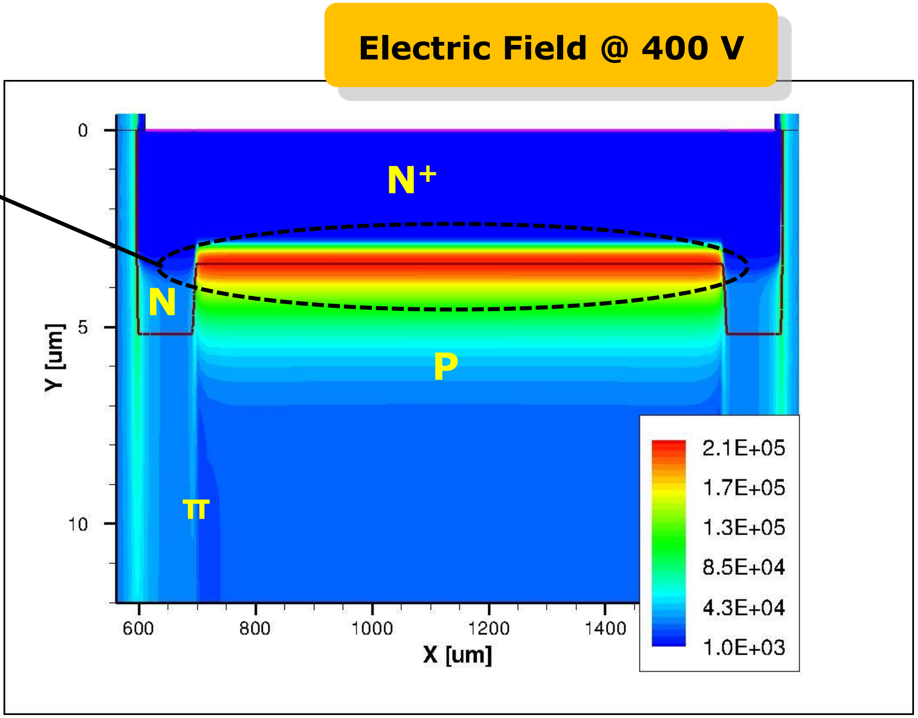
Technique	Typical Breakdown Voltage (%)[a]	Peak Surface Electric Field (%)[b]	Typical Device Size	Device Types	Remarks
Planar junction	50	80	Small (< 100 mils)	BJT, MOSFET	Seldom used for high-voltage devices
Planar junction with field ring	80	80	Medium (≤ 1 in.)	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Planar junction with field plate	60	80	Medium (≤ 1 in.)	BJT, MOSFET	Usually used in conjunction with field ring
Positive bevel	100	50	Large (> 1 in.)	Rectifier, SCR	Well suited for single device per wafer
Negative bevel	90	60	Large (> 1 in.)	SCR	Well suited for single device per wafer
Double positive bevel	100	80	Large (> 1 in.)	SCR	Well suited for single device per wafer only
Positive etch contour	90	60	All	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Negative etch contour	80	60	All	BJT, MOSFET, SCR	Well suited for a large number of devices per wafer
Junction termination extension	95	80	All	BJT, MOSFET, SCR	Well suited for both single devices and a large number of devices per wafer; high leakage current; passivation sensitive

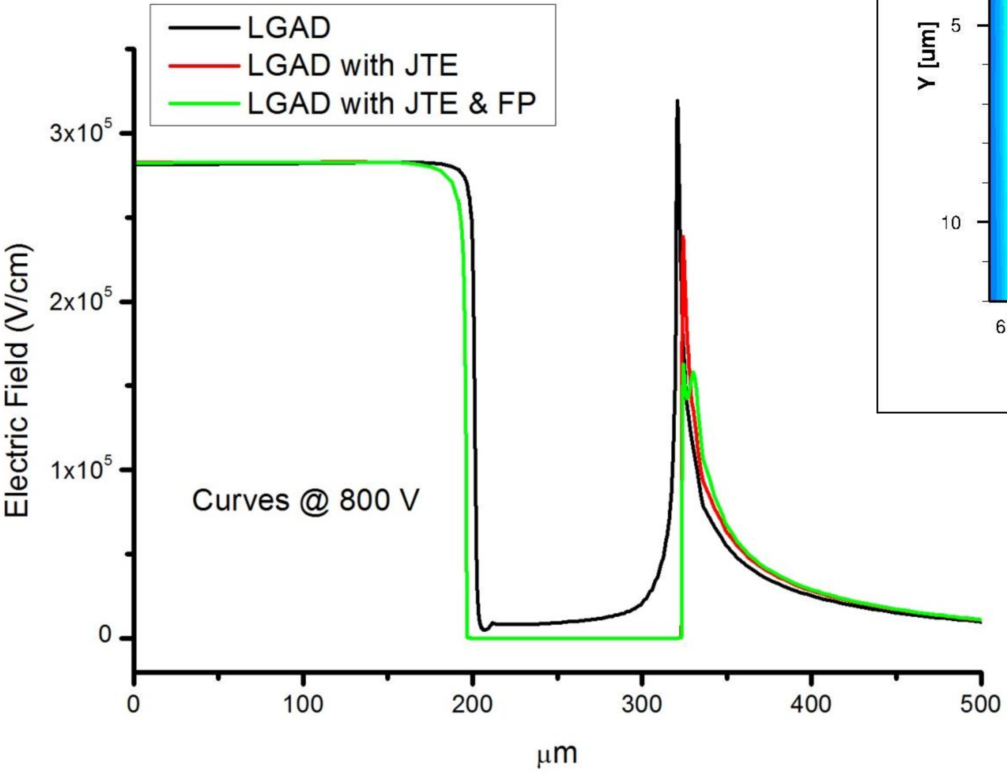
[a] As percentage of parallel-plane case.

[b] As percentage of bulk.

Design of the Edge Termination

Planar and uniform electric field distribution, high enough to activate charge multiplication

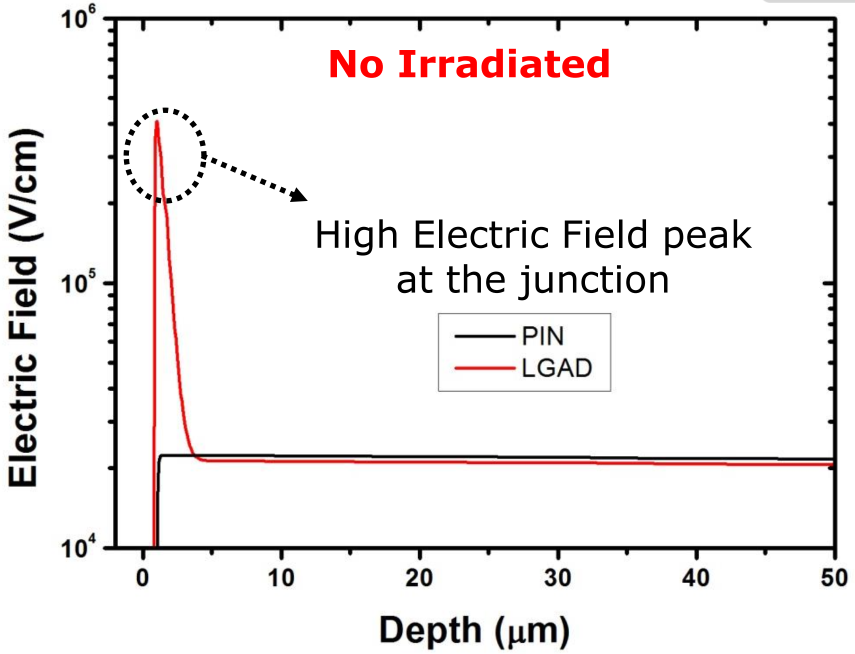

Electric Field @ 400 V



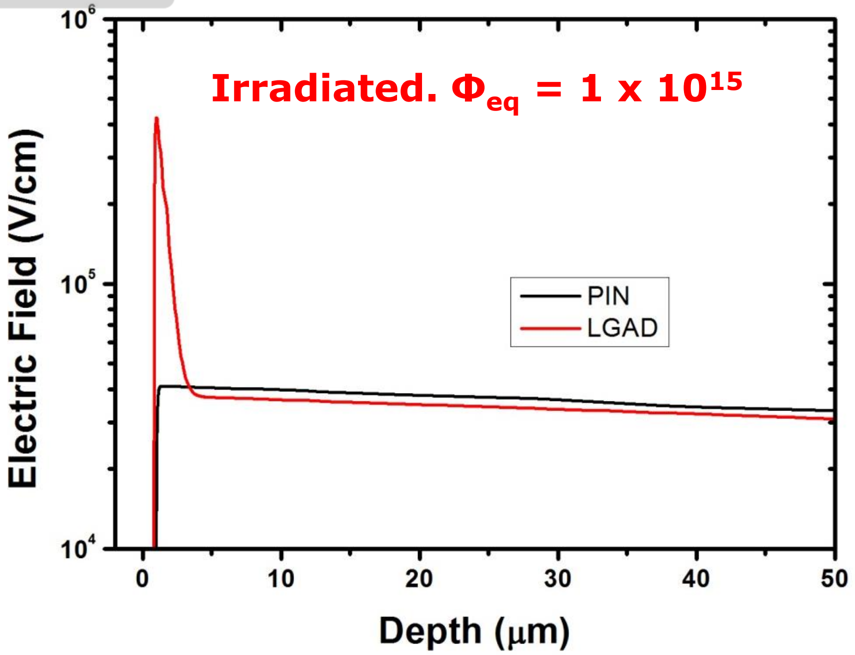
$$V_{BD}|_{Central} \ll V_{BD}|_{Termination}$$

Simulation of the Irradiated Devices

Curves @ 600 V


No Irradiated

High Electric Field peak at the junction


Irradiated. Φ_{eq} = 1 x 10^{15}

- **PiN**: electric field strength at the junction increases after irradiation
- **LGAD**: electric field strength at the junction is held after irradiation

▪ **Irradiation Trap Model (Perugia Model):**

Acceptor;	E= E_c + 0.46 eV;	η=0.9;	$\sigma_e = 5 \times 10^{-15}$;	$\sigma_h = 5 \times 10^{-14}$
Acceptor;	E= E_c + 0.42 eV;	η=1.613;	$\sigma_e = 2 \times 10^{-15}$;	$\sigma_h = 2 \times 10^{-14}$
Acceptor;	E= E_c + 0.10 eV;	η=100;	$\sigma_e = 2 \times 10^{-15}$;	$\sigma_h = 2.5 \times 10^{-15}$
Donor;	E= E_v - 0.36 eV;	η=0.9;	$\sigma_e = 2.5 \times 10^{-14}$;	$\sigma_h = 2.5 \times 10^{-15}$

▪ **Impact Ionization Model:**
Universty of Bolonia

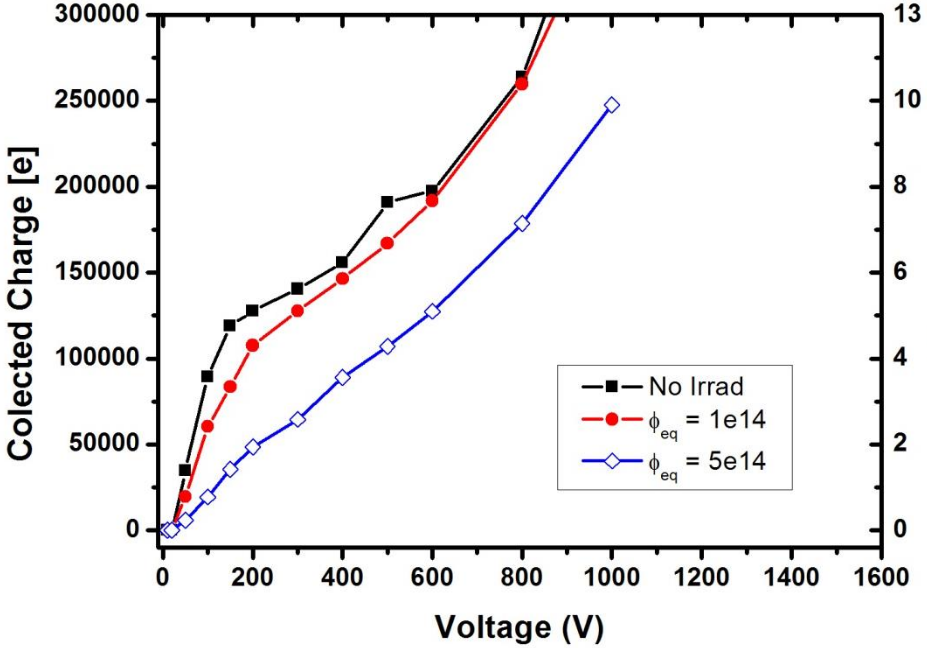
$$Conc = \eta \cdot \phi$$

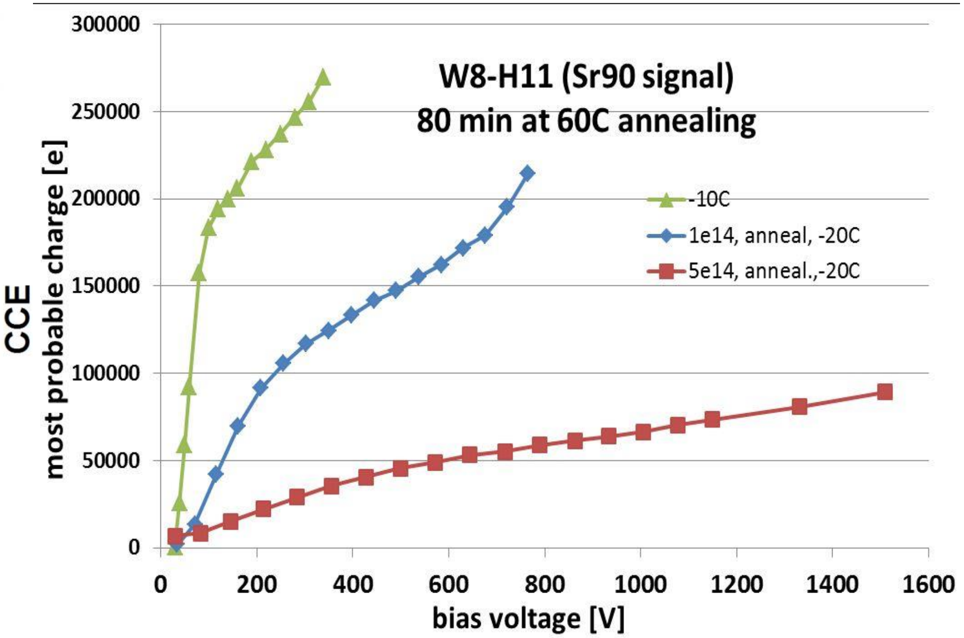
Simulation of the Irradiated Devices

Numerical Simulations

LGAD Wafer 8

Experimental Measurements





CCE @ 400 V

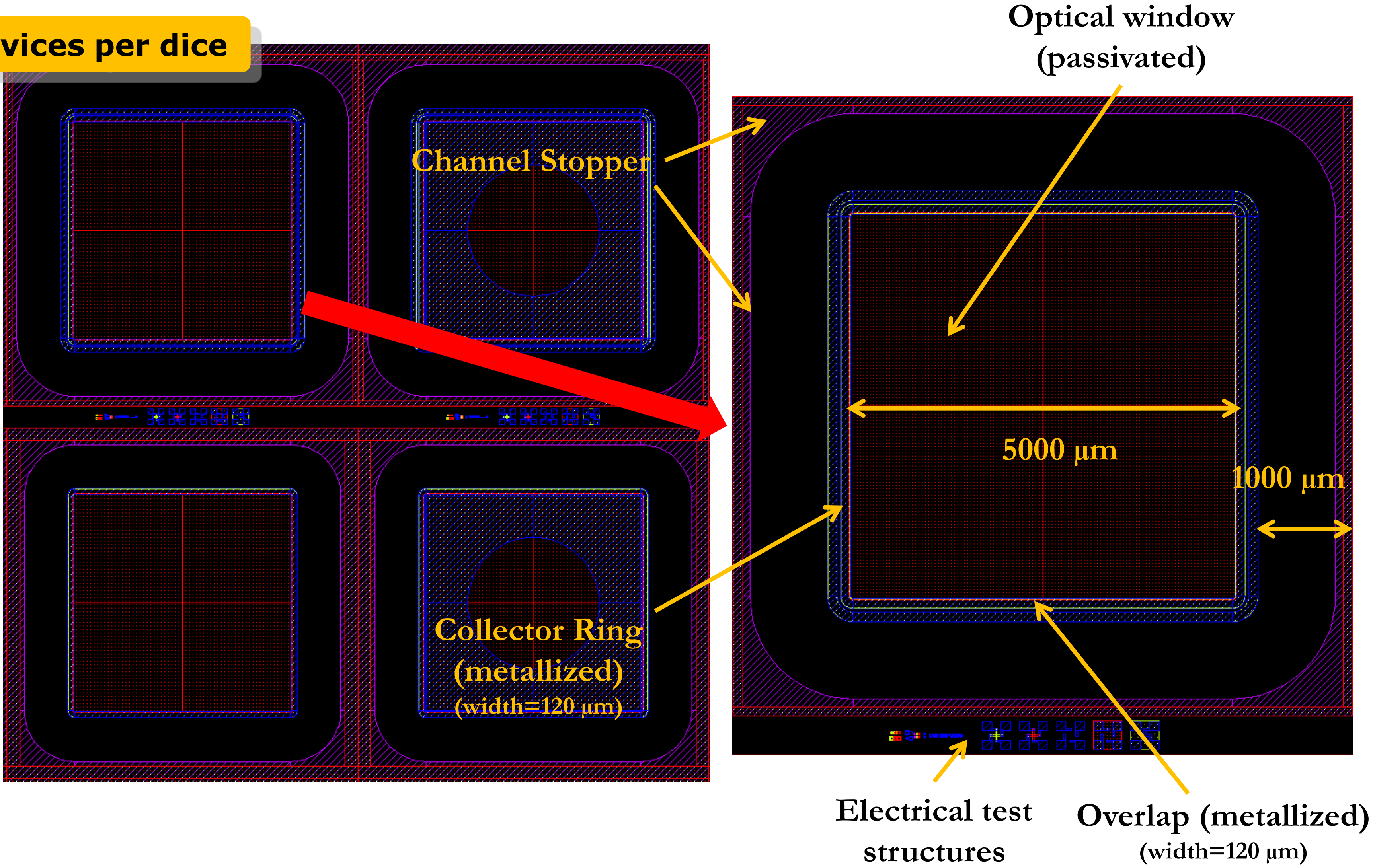
Φ_{eq} [cm^{-2}]	Simulated	Measured
No Irrad	7	10
1e14	6	6
5e14	3	2

Measurements done in Ljubjana

First estimation by simulation. We must work to enhance this study

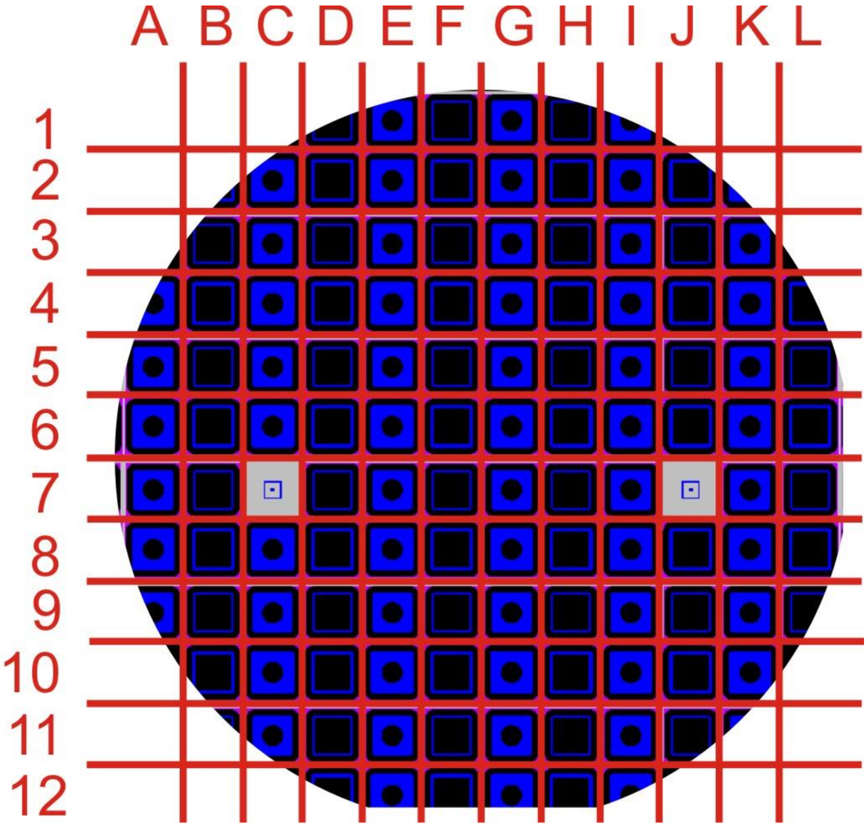
Fabrication (I)

4 Devices per dice

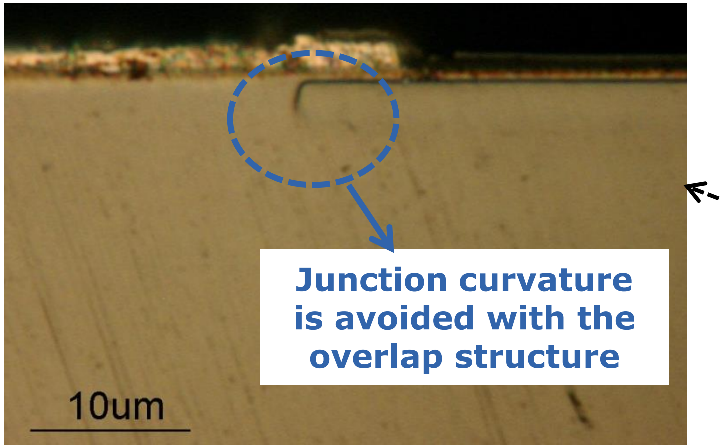


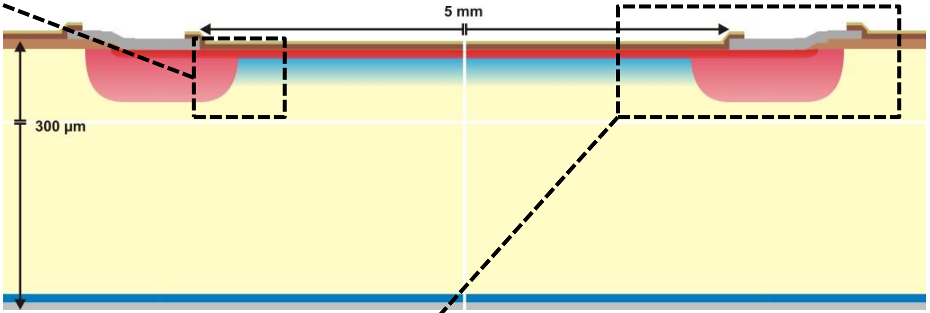
Fabrication (II)

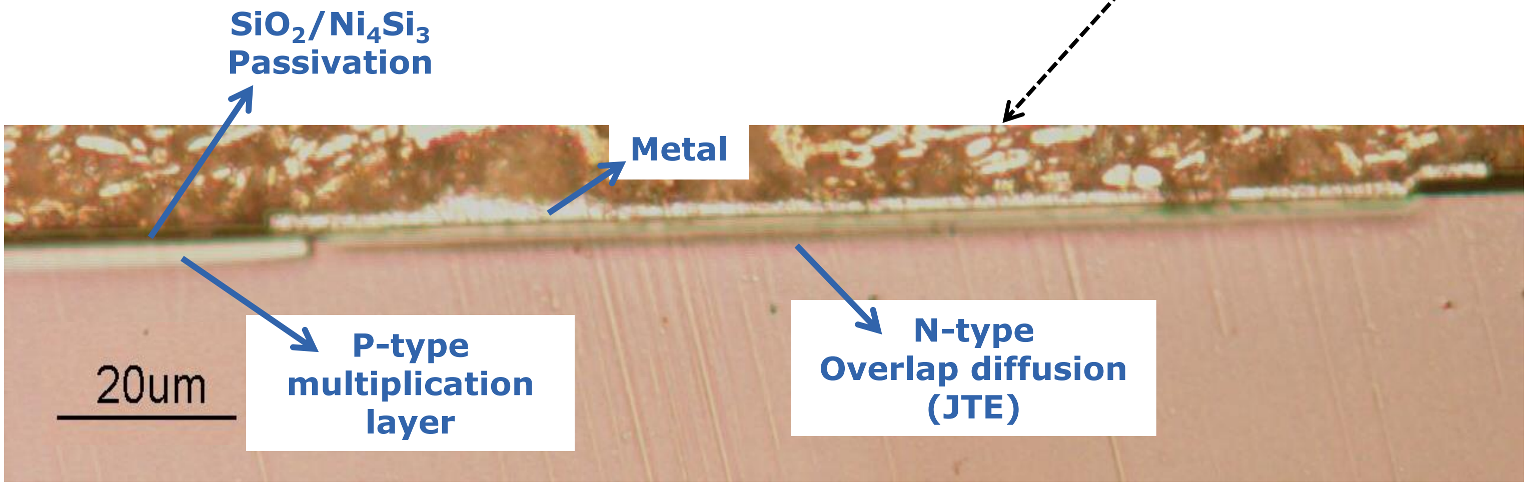
Wafer Number	P-layer Implant (E = 100 keV)	Substrate features
1	1.0×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
2	1.1×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
3	1.2×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
4	1.3×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
5	1.4×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
6	1.5×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
7	1.6×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
8	2.0×10^{13} cm^{-2}	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
9	----- (PIN wafer)	HRP 300 (FZ; ρ>10 KΩ·cm; <100>; T = 300±10 μm)
10	1.1×10^{13} cm^{-2}	HRP OXG (DOFZ; ρ = 5-15 KΩ·cm; <100>; T = 285±25 μm)
11	1.3×10^{13} cm^{-2}	HRP OXG (DOFZ; ρ = 5-15 KΩ·cm; <100>; T = 285±25 μm)



Technological Characterization



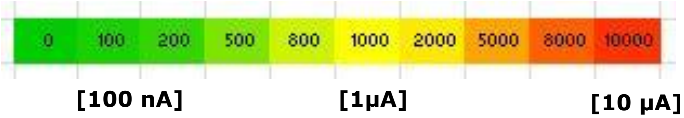




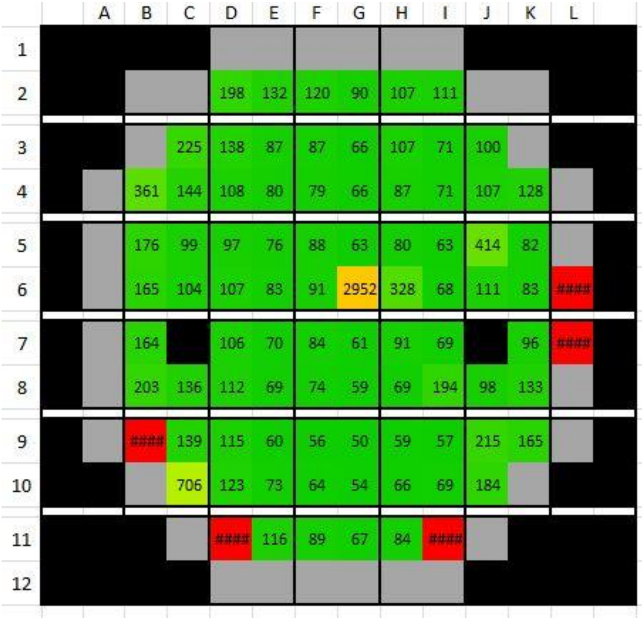
Electrical Characterization (I)

- ☐ **Fabrication yield worsens with increasing implant dose for the p-type multiplication layer.**

Measured Current [nA] at 200 V

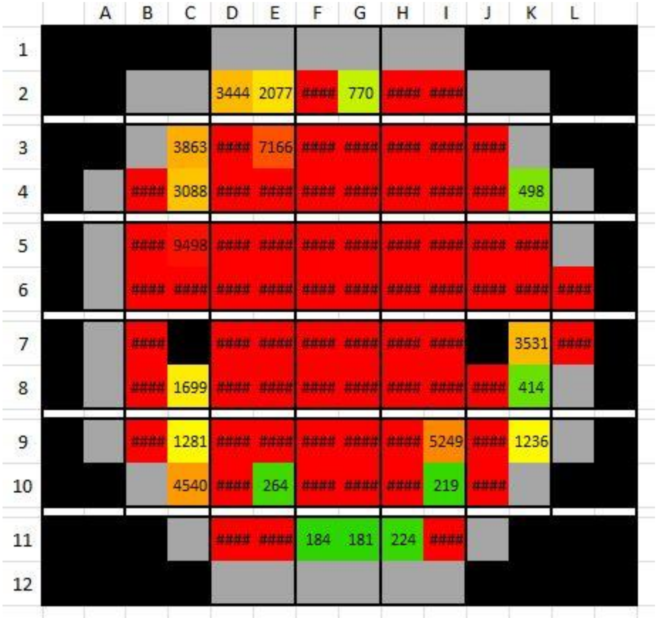


Wafers were fabricated in the same run, following exactly the same fabrcation steps. Only difference between W9 and W8 is that PiN wafer was not implanted with the multiplication implantation.



	A	B	C	D	E	F	G	H	I	J	K	L
1												
2				198	132	120	90	107	111			
3			225	138	87	87	66	107	71	100		
4		361	144	108	80	79	66	87	71	107	128	
5		176	99	97	76	88	63	80	63	414	82	
6		165	104	107	83	91	2952	328	68	111	83	####
7		164		106	70	84	61	91	69		96	####
8		203	136	112	69	74	59	69	194	98	133	
9		####	139	115	60	56	50	59	57	215	165	
10			706	123	73	64	54	66	69	184		
11				####	116	89	67	84	####			
12												

PiN Wafer (W9)



	A	B	C	D	E	F	G	H	I	J	K	L
1												
2				3444	2077	####	770	####	####			
3			3863	####	7166	####	####	####	####	####		
4		####	3088	####	####	####	####	####	####	####	498	
5		####	9498	####	####	####	####	####	####	####	####	
6		####	####	####	####	####	####	####	####	####	####	####
7		####		####	####	####	####	####	####		3531	####
8		####	1699	####	####	####	####	####	####	####	414	
9		####	1281	####	####	####	####	####	5249	####	1236	
10			4540	####	264	####	####	####	219	####		
11				####	####	184	181	224	####			
12												

Wafer 8 (Implant dose = 2×10^{13} cm^{-2})

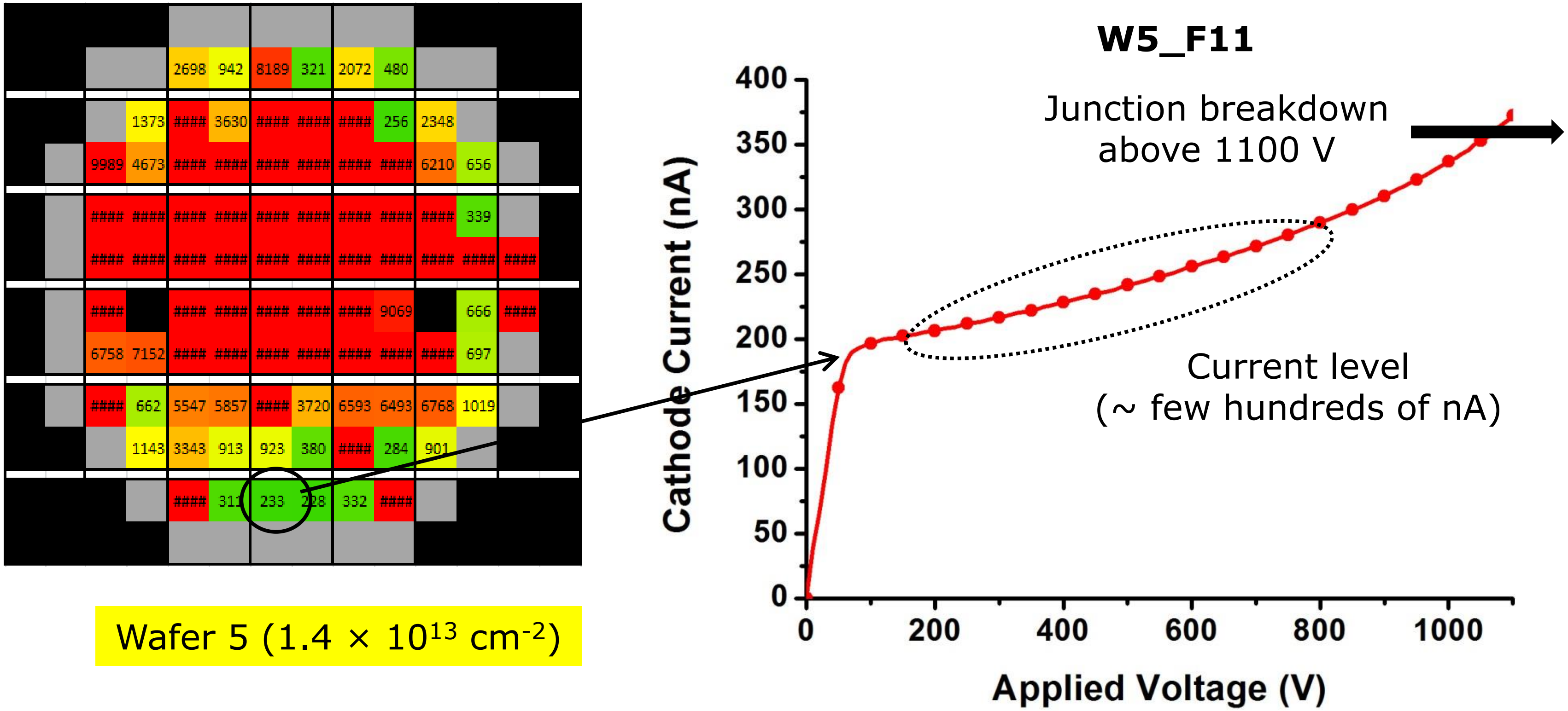
We are working in the yield improvement

Electrical Characterization (II)

✓ "Good" Devices

→ **Current levels below 1 µA thorough the whole voltage range**

→ **Junction breakdown above 1100 V (*Except Wafer 8: < 800 V, still good)**



		2698	942	8189	321	2072	480			
	1373	####	3630	####	####	####	256	2348		
9989	4673	####	####	####	####	####	####	6210	656	
####	####	####	####	####	####	####	####	####	339	
####	####	####	####	####	####	####	####	####	####	####
####		####	####	####	####	####	9069		666	####
6758	7152	####	####	####	####	####	####	####	697	
####	662	5547	5857	####	3720	6593	6493	6768	1019	
	1143	3343	913	923	380	####	284	901		
		####	311	233	228	332	####			

Wafer 5 (1.4 × 10^{13} cm^{-2})

W5_F11

Junction breakdown above 1100 V

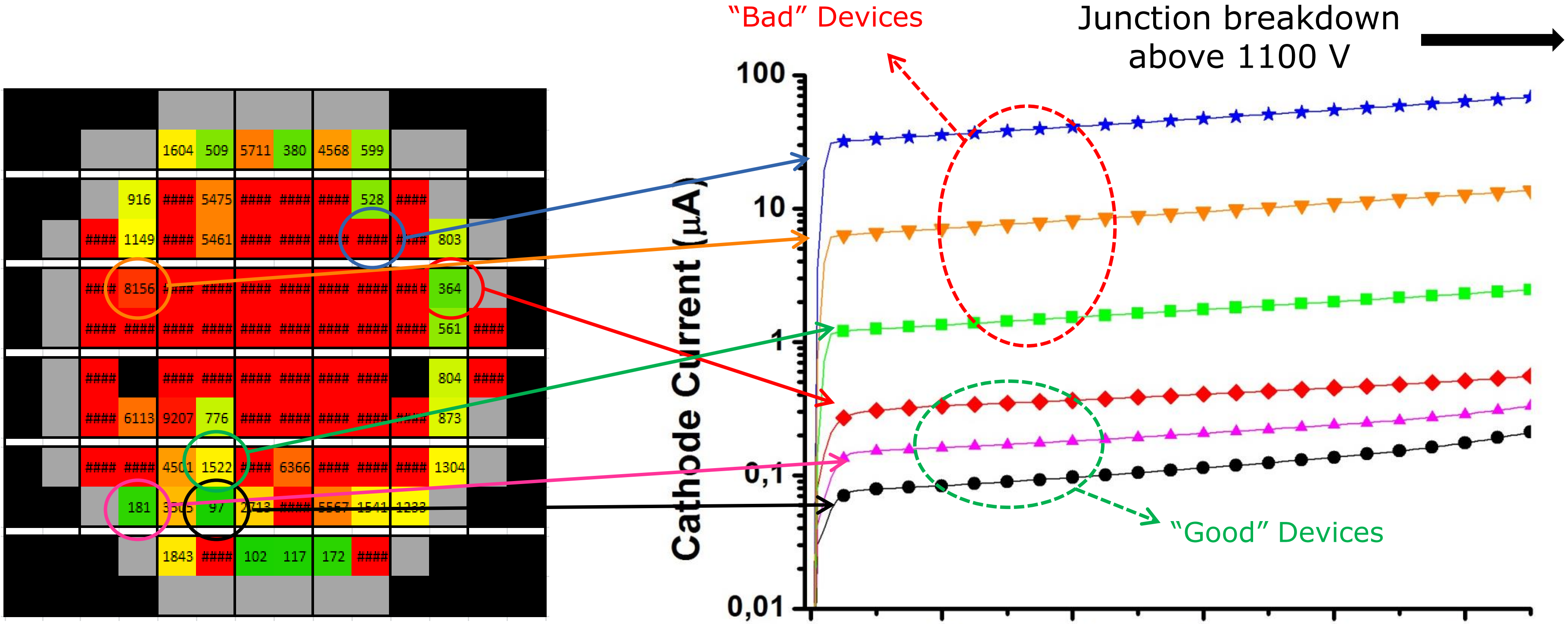
Current level (~ few hundreds of nA)

Electrical Characterization (III)

✘ "Bad" Devices

→ **Current levels above 1 μA thorough the whole voltage range**

→ **Junction breakdown above 1100 V (*Except Wafer 8)**



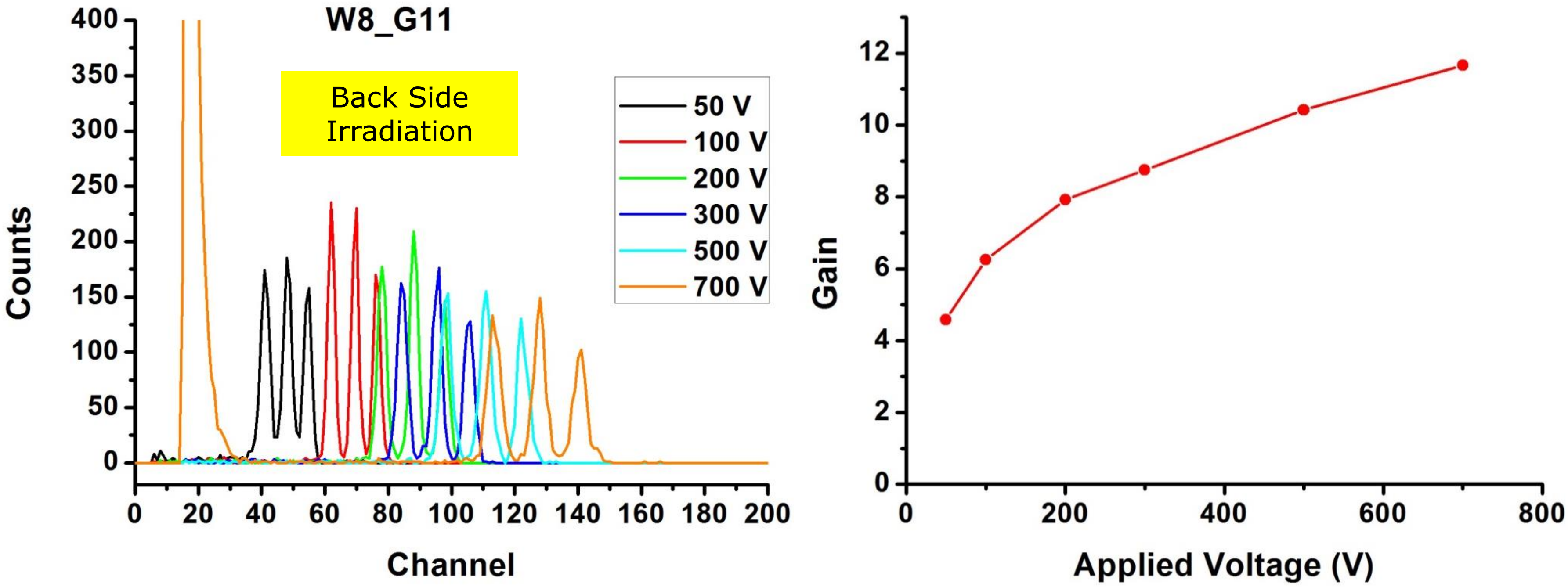
			1604	509	5711	380	4568	599			
		916	####	5475	####	####	####	528	####		
	####	1149	####	5461	####	####	####	####	####	803	
	####	8156	####	####	####	####	####	####	####	364	
	####	####	####	####	####	####	####	####	####	561	####
	####		####	####	####	####	####	####		804	####
	####	6113	9207	776	####	####	####	####	####	873	
	####	####	4501	1522	####	6366	####	####	####	1304	
		181	3305	97	2713	####	5567	1541	1233		
			1843	####	102	117	172	####			

Wafer 6 (1.5 × 10^{13} cm^{-2})

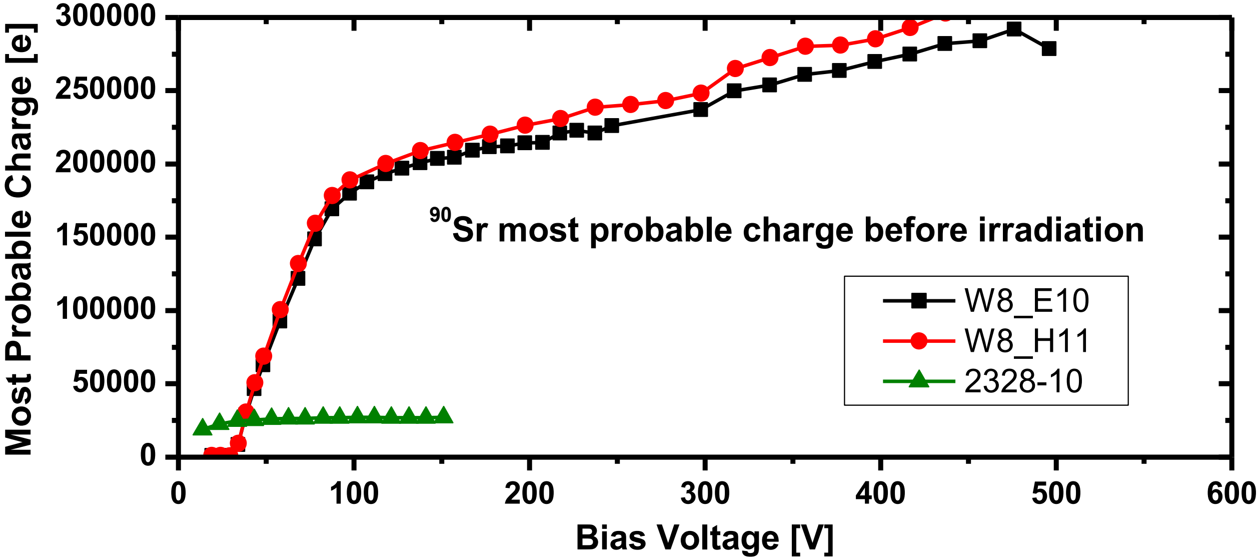
Charge collection (alpha)

- ☐ **Multiplication factor has been tested with tri-alpha (^{239}Pu/^{241}Am/^{244}Cm) source.**
  → **Irradiation through the anode (back side, 1 µm Aluminum):**

$$Gain_{@V} = \frac{Channel\ Central\ peak_{@V}}{Channel\ Central\ peak_{No\ multiplied}}$$



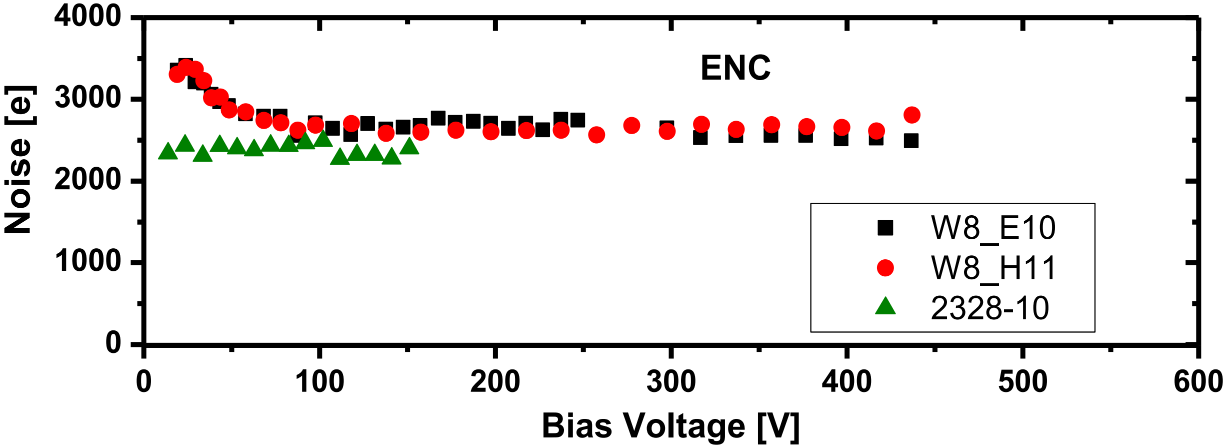
Charge collection (mips)



90Sr Setup (done at JSI):

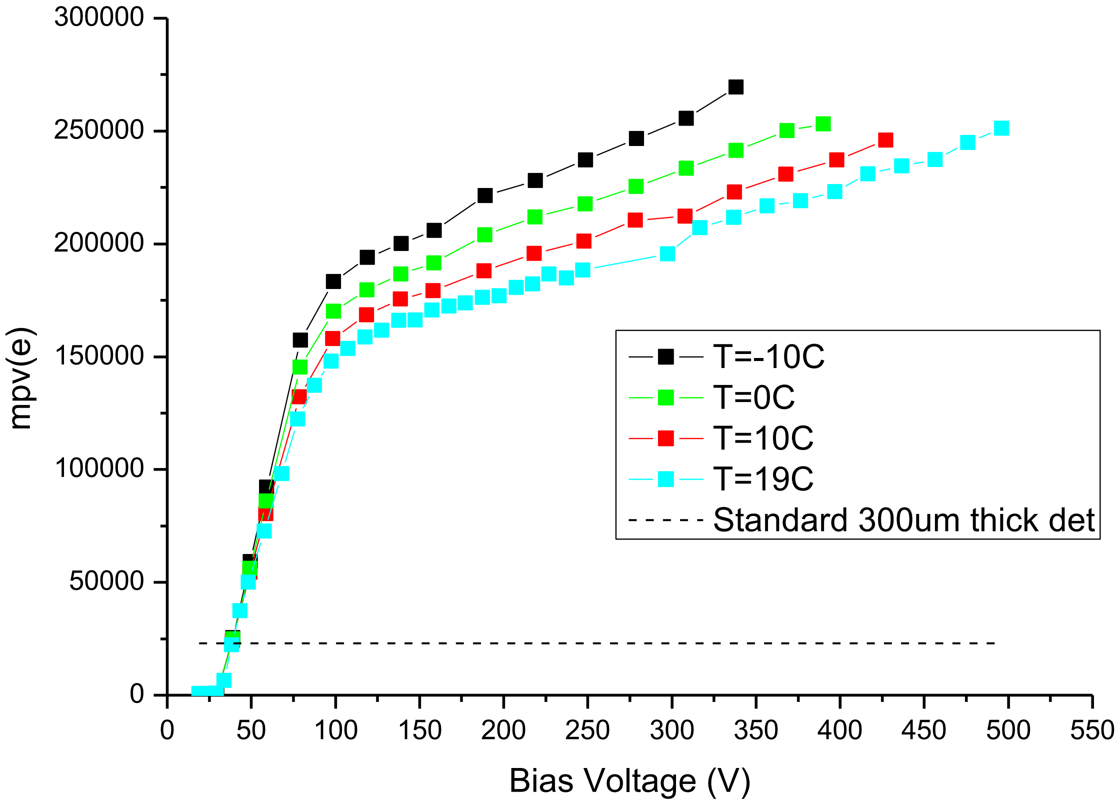
- Measuring absolute charge collection for MIP with LHC-type electronics

- Measuring noise performance



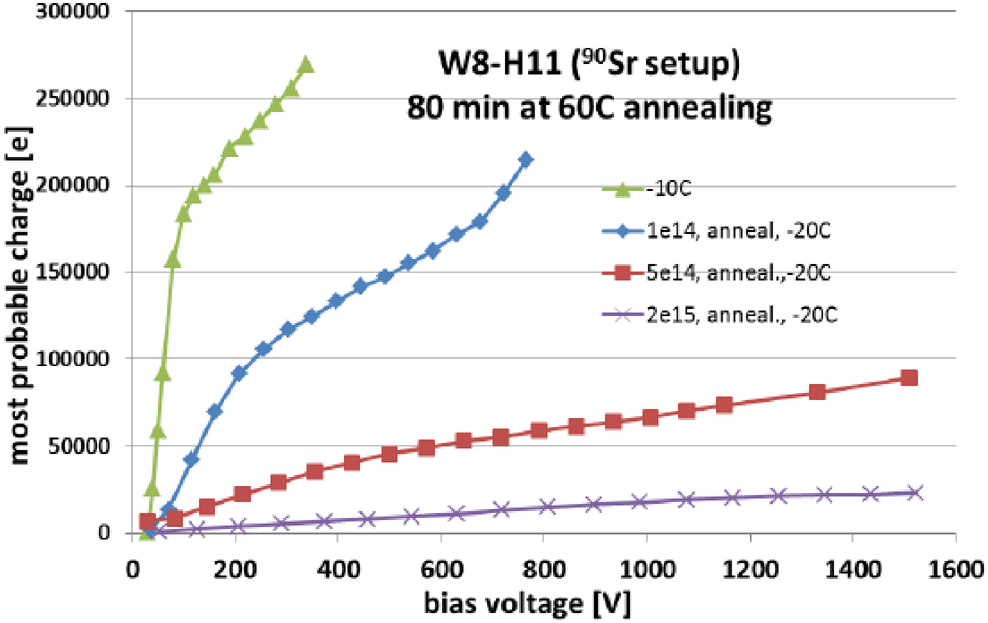
Improvement of signal for a **factor 8** at 300 V before irradiation
No significant increase of noise – dominated by series noise

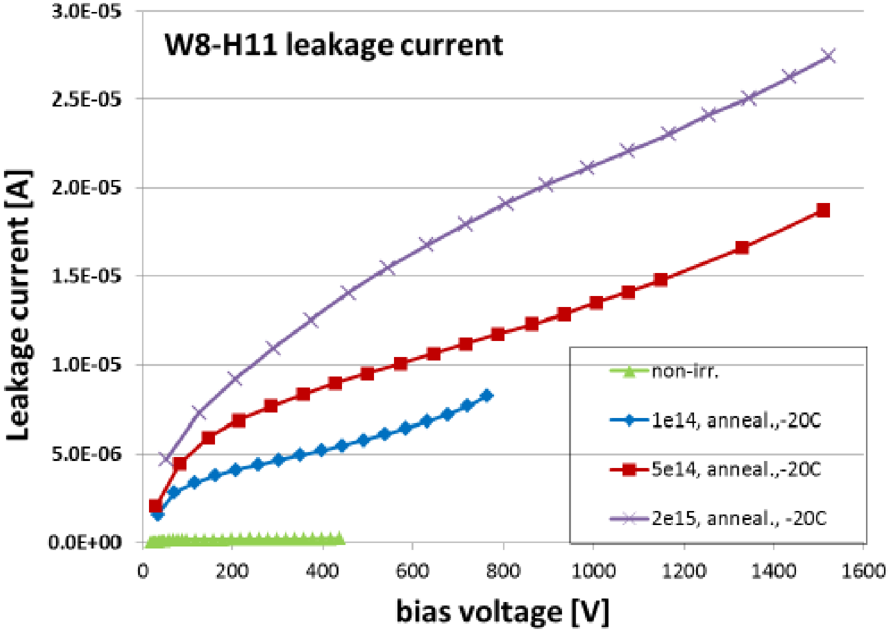
Temperature dependence of Multiplication



- It seems that there is a limit on multiplication of around a factor of 10. At lower temperatures break down is reached at lower voltages.
- Increase of multiplication at lower temperatures is expected – larger impact ionization coefficients.

Irradiation studies





Detectors irradiated with neutrons in Ljubljana.

Multiplication decreases significantly with irradiation:

- Break-down performance is good
- Leakage current increase is not linear with fluence – increase with fluence in smaller due to degradation of multiplication

$$I_{leak} = M_I \cdot I_{gen} = \underset{\downarrow}{M_I} \cdot \alpha \cdot \underset{\uparrow}{\Phi}$$

For more details please see G. Kramberger´s talk at 22nd RD50 Workshop, University of New Mexico, Albuquerque, USA

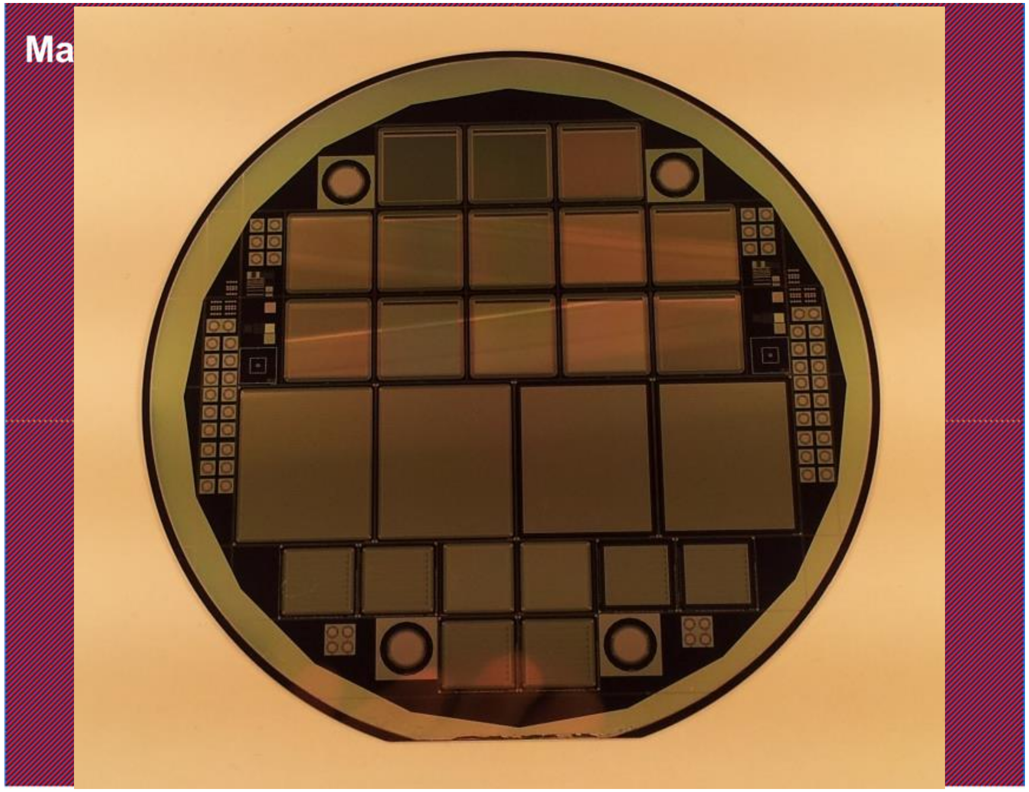
New Fabrication run: microstrip and pixel detectors

Project financed by RD50 collaboration.

Fabrication run already finished, very preliminary measurements are presented.

Different geometries, implant doses and substrates.

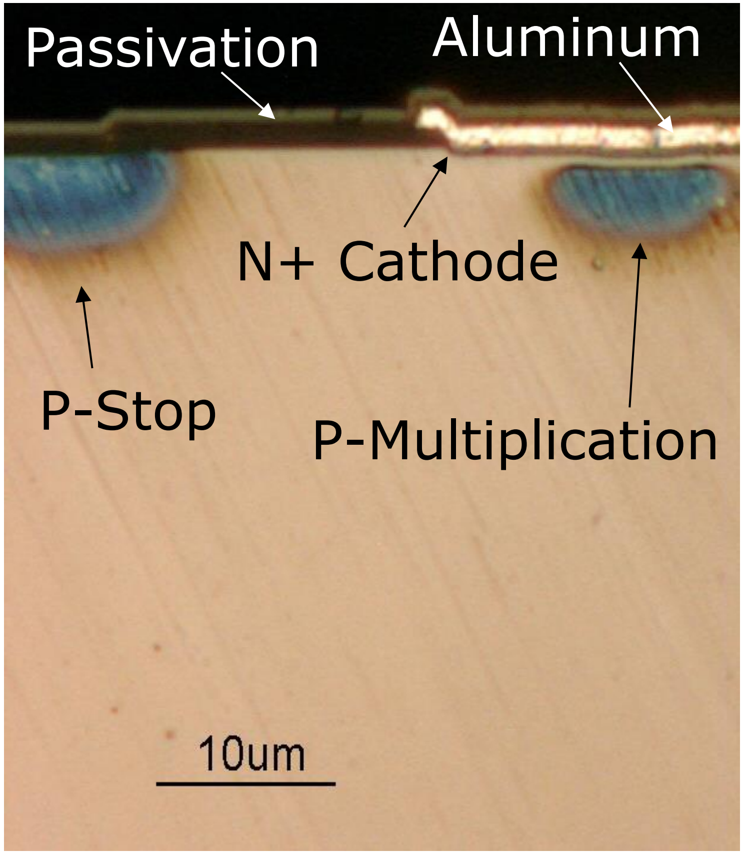
Junction termination extension not implemented for this first run => lower breakdown voltage may be expected.

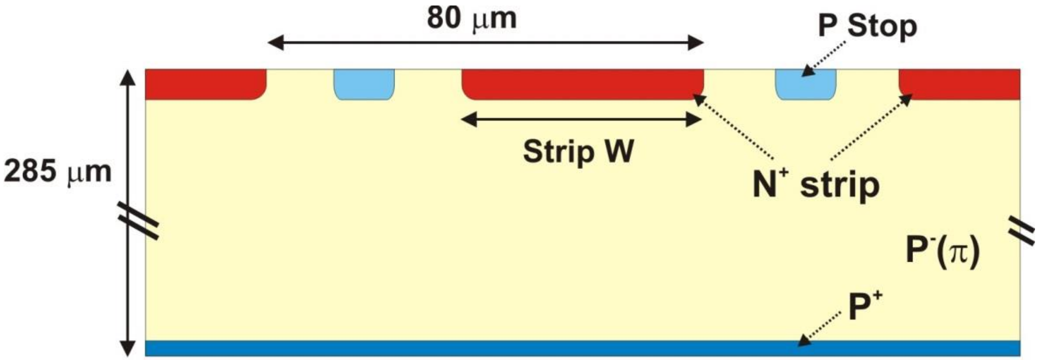


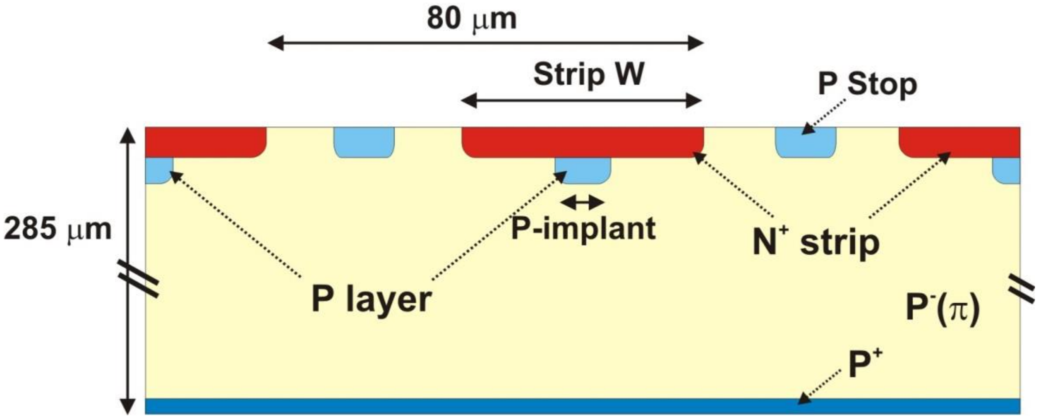
14 p-type wafers

Thick (μm)	Resistivity (Ωcm)	Substrate resistivity (Ωcm)	Substrate thickness (μm)
9.8	110.5	0.006	525
50.4	96.7	0.006	525
75.2	104.6	0.006	525
285 (FZ)	12000 ± 7000		

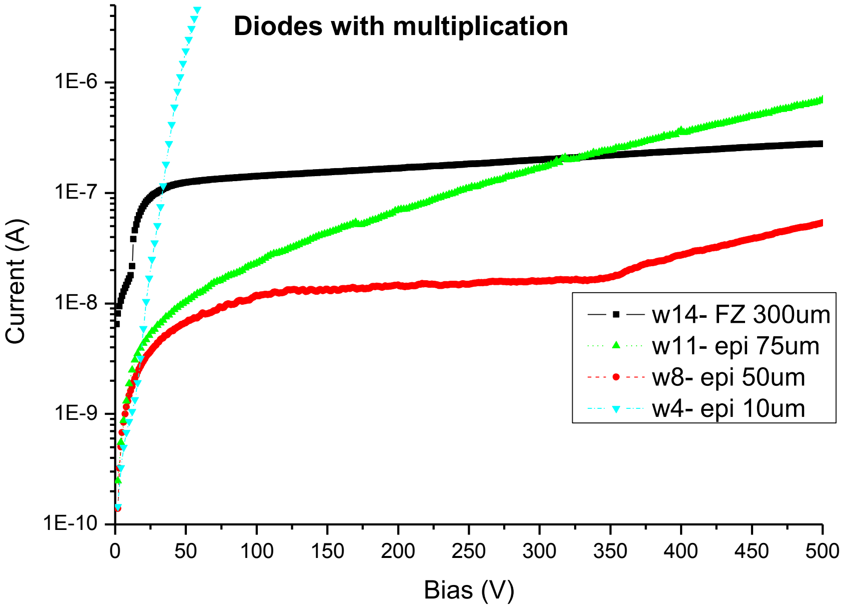
Technology

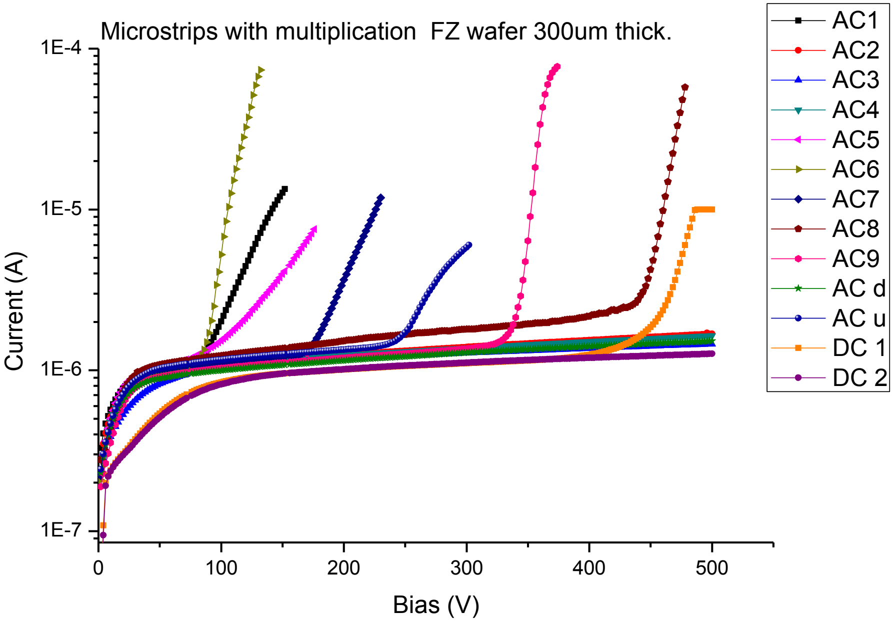

Passivation
Aluminum
N+ Cathode
P-Stop
P-Multiplication
10um


80 μm
P Stop
Strip W
285 μm
N+ strip
P-(π)
P+


80 μm
Strip W
P Stop
285 μm
P-implant
N+ strip
P layer
P-(π)
P+

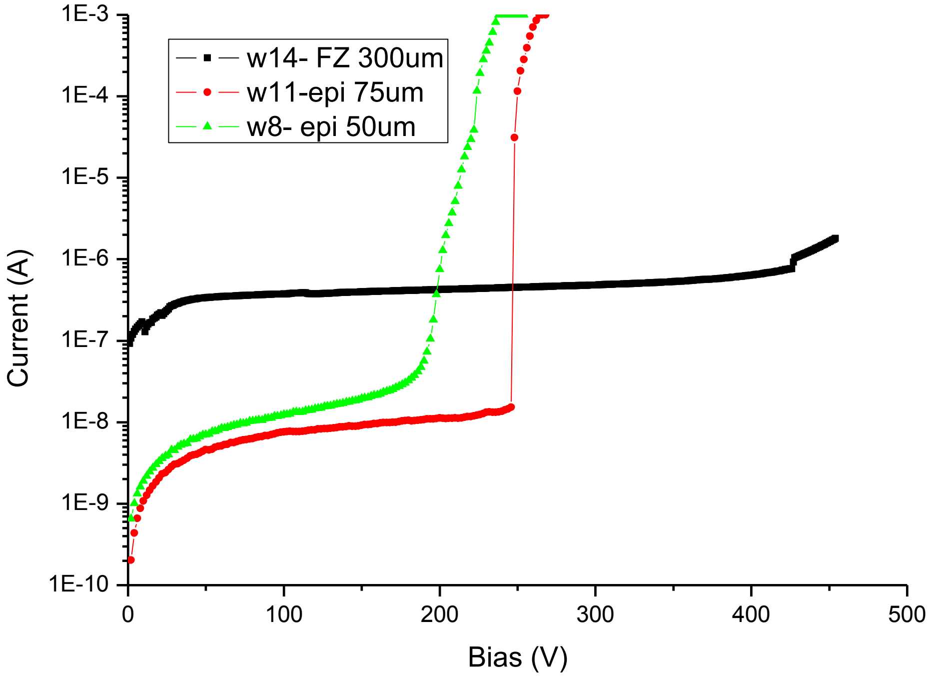
Electrical Characterization



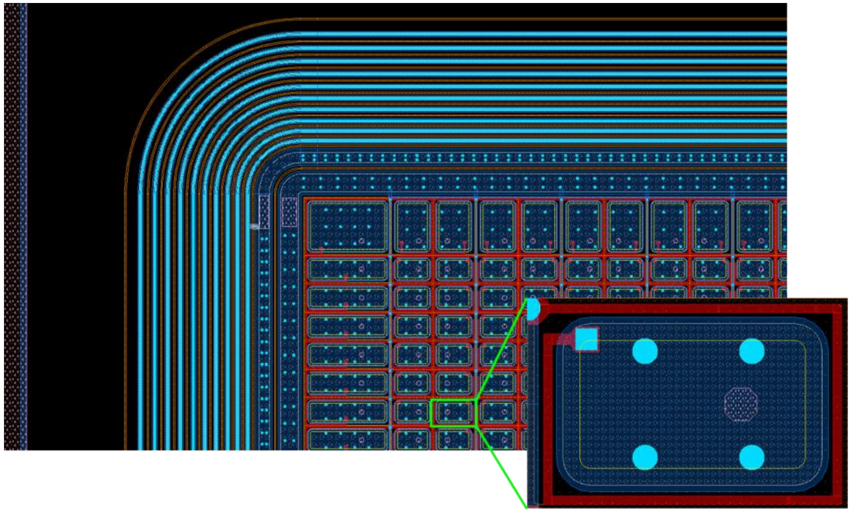


- Breakdown performance is good although the JTS were not used for these devices.
- Variation in breakdown voltage due to different metal over implant overlapping.

CMS pixel detectors



Pixels with polysilicon bias resistor.



All pixels are connected through a 1Mohm polysilicon bias resistor. Breakdown is again very good before irradiation. Current scales with volume but for thinner devices breakdown occurs at lower voltages due to higher electric fields.

Conclusions

- First LGAD detectors have been fabricated.
- Excellent break-down performance of the diodes before and after irr.
- Diodes with gain perform formidably before the irradiation with gain of ~10 for 90Sr electrons
- After irradiation the multiplication drops significantly :
  - At $2e^{15}$ cm^{-2} is around ~1.5 at 1000 V
  - Current and noise scale as expected with multiplication
- New fabrication run with strip and pixel detectors under test. Preliminary resutls are very promising.

- # Future work:
  - Charge collection test of strip and pixels detectors
  - Irradiation studies.

Thanks for your attention

Experimental Results (IV)

- ☐ **Several samples were sent out for different experimental characterizations.**

Institut “Jozef Stefan” Ljubljana (Slovenia)

Device	Type	I @ 400 V	V_{BD} (I=1µA)
W8_E10	LGAD	241 nA	550 V
W8_H11	LGAD	197 nA	490 V

- ☐ **Signal measurement**:
  - ☐ **^{90}Sr Spectrum**
  - ☐ **α-TCT**
  - ☐ **^{241}Am X-ray spectrum**
- ☐ **Irradiation at different fluences**

Santa Cruz Institute of Particle Physics (USA)

Device	Type	I @ 200 V	V_{BD} (I=1µA)
W8_I10	LGAD	472 nA	270 V
W9_E10	PiN	73 nA	> 1100 V

- ☐ **C-V and I-V**
- ☐ **1064 nm Laser & Comparison with ATLAS07 diodes**

Instituto de Física de Cantabria, Santander (Spain)

- ☐ **Laser TCT**

Device	Type	I @ 400 V	V_{BD} (I=1µA)
W6_G11	LGAD	117 nA	> 1100 V
W6_H11	LGAD	172 nA	> 1100 V
W7_K9	LGAD	732 nA	> 1100 V
W7_F11	LGAD	421 nA	> 1100 V

Device	Type	I @ 400 V	V_{BD} (I=1µA)
W8_K4	LGAD	674 nA	650 V
W8_K8	LGAD	549 nA	900 V
W9_F9	PiN	61 nA	> 1100 V
W9_G9	PiN	54 nA	> 1100 V

Why Internal Gain?

- **Increases the radiation hardness of the detector, leading to similar signals before and after irradiation:**
    - **Charge multiplication off-sets the charge lost due to trapping during the drift of the carriers [1].**
    - **Higher electric fields reduce the collection times, reducing the trapping probability.**
- **Charge Collection Efficiency is improved, keeping a proportional response.**
- **Thinner detectors are available with the same signal. Fast detectors are also foreseen [1].**
- **The noise components are not increased at the same pace than the multiplied signal. As a consequence the signal to noise ratio is improved.**

Why Low Gain?

- **High Gain implies higher levels of multiplication noise (inherent to the stochastic process of multiplication [2]), spoiling the improvement of the Signal to Noise ratio.**
- **Collection times are increased with gain (more charge to be collected), increasing the trapping efficiency and avoiding the off-setting of the charge loss.**

[1] H. Sadrozinski, et al. 20th RD50 Workshop, Bari (Italy), 2012

[2] R.J. McIntyre. IEEE TED-13, No.1 p.164-168, 1966

$$ENF = \kappa M + \left(2 - \frac{1}{M}\right)(1 - \kappa)$$

Diffused Planar Junctions

- Using a planar diffusion technology we can fabricate a large number of devices on a single wafer by selective diffusion of impurities through a silicon dioxide masking layer.
- Due to the lateral doping extension through the window periphery, we can identify three important areas at the junction formed using this technology.,
  - Plane into the diffusion window,
  - Cylindrical at the mask edges (Line A at the figure), and
  - Spherical at the sharp corners (Line B).
- This curvature effects produce a reduction in the voltage capability (till 50 % of the ideal value).

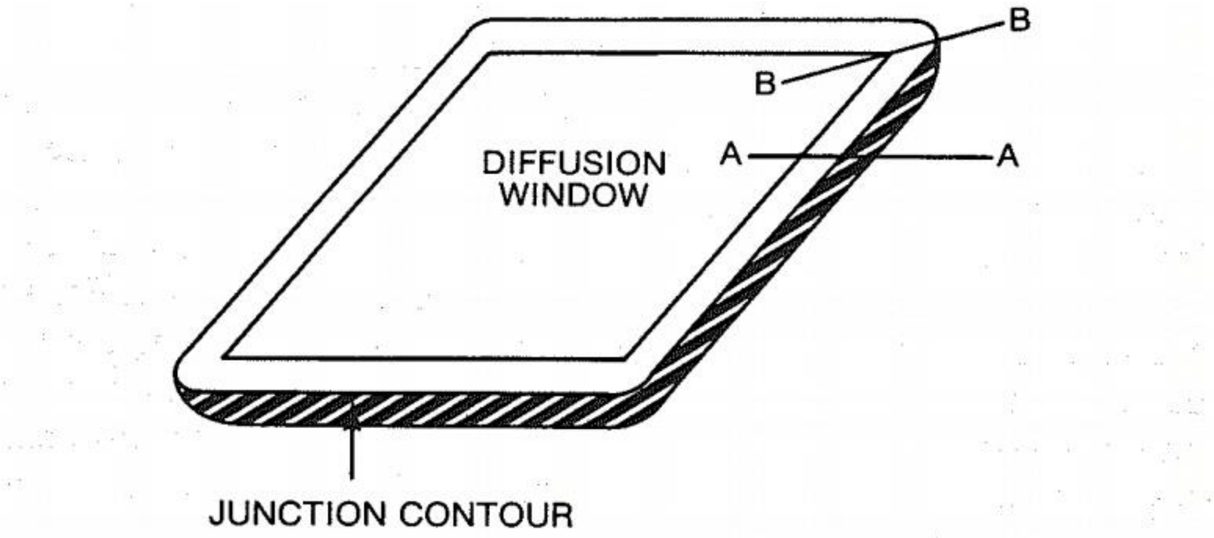


Fig. 3.11. Planar junction formed by diffusion through a rectangular diffusion window.

Cylindrical Junction

- The breakdown voltage is given by,

$$\frac{BV_{\mathrm{CYL}}}{BV_{\mathrm{PP}}} = \left\{ \frac{1}{2} \left[\left(\frac{r_{\mathrm{j}}}{W_{\mathrm{c}}} \right)^2 + 2 \left(\frac{r_{\mathrm{j}}}{W_{\mathrm{c}}} \right)^{6/7} \right] \ln \left[1 + 2 \left(\frac{W_{\mathrm{c}}}{r_{\mathrm{j}}} \right)^{8/7} \right] - \left(\frac{r_{\mathrm{j}}}{W_{\mathrm{c}}} \right)^{6/7} \right\}$$

- Expression that can be approximated by,

$$\frac{BV_{\mathrm{CYL}}}{BV_{\mathrm{PP}}} = \left[0.871 + 0.125 \ln \left(\frac{r_{\mathrm{j}}}{W_{\mathrm{c,PP}}} \right) \right]^2$$

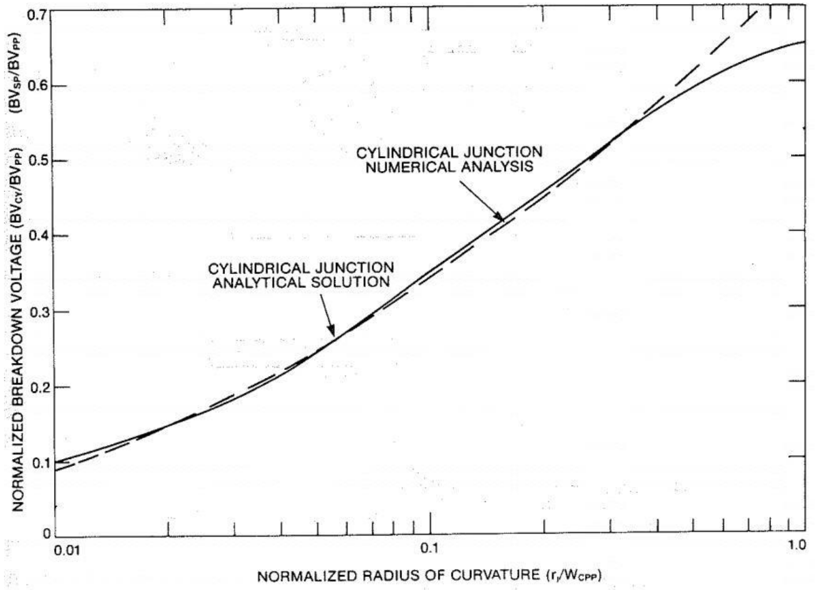
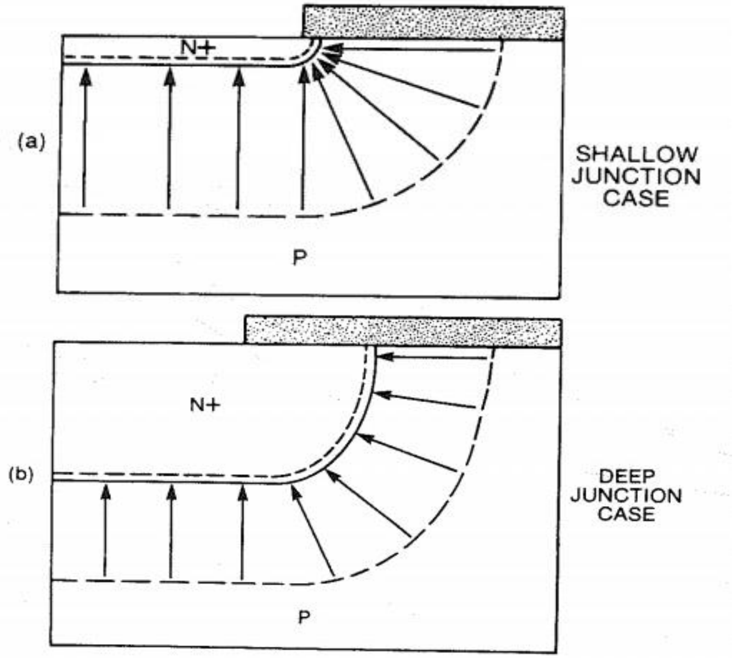


Fig. 3.16. Normalized breakdown voltage of cylindrical and spherical junctions as a function of the normalized radius of curvature.



3.17. Electric field crowding at the edges of (*a*) shallow and (*b*) deep junction.

- BVcyl is always less than BVpp.
- If rj increases (which implies an increase in junction depth) BVcyl increases and reduces the difference with BVpp.

Spherical Junction

- The breakdown voltage is given by,

$$\frac{BV_{SP}}{BV_{PP}} = \left(\frac{r_j}{W_c}\right)^2 + 2.14\left(\frac{r_j}{W_c}\right)^{6/7} - \left[\left(\frac{r_j}{W_c}\right)^3 + 3\left(\frac{r_j}{W_c}\right)^{13/7}\right]^{2/3}$$

- BVsp is always less than BVcyl.

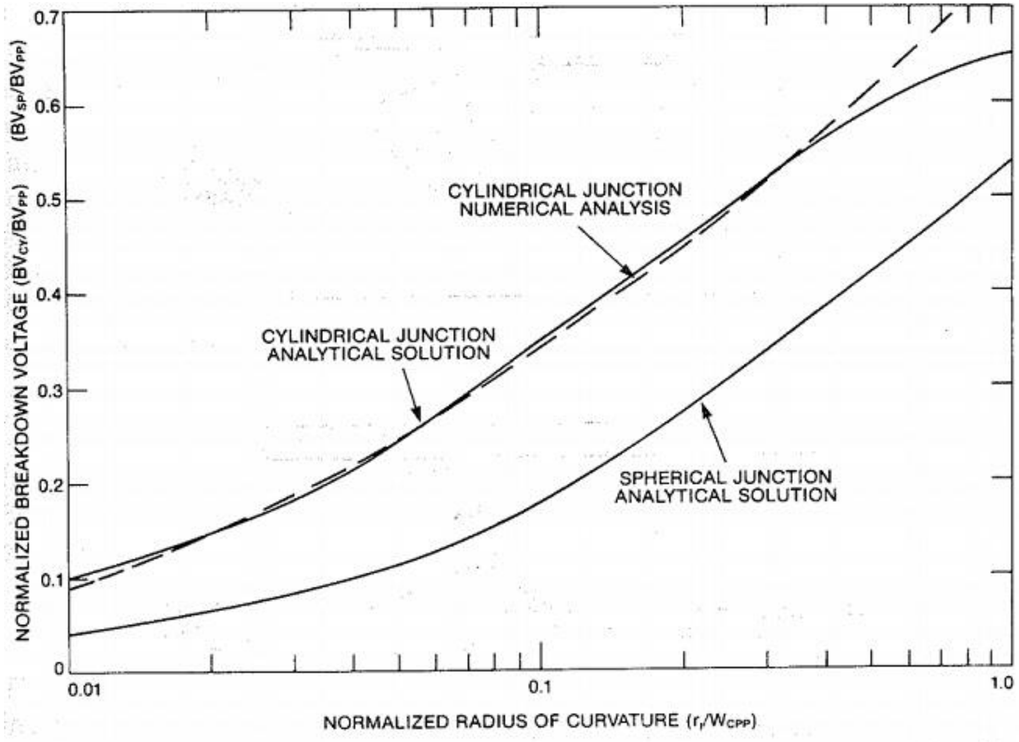


Fig. 3.16. Normalized breakdown voltage of cylindrical and spherical junctions as a function of the normalized radius of curvature.

Fabrication of new p-type pixel detectors with enhanced multiplication effect in the n-type electrodes.

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1)Thin p-type epitaxyal substrates

Detector proposed by Hartmut Sadrozinski and Abe Seiden (UCSC) , **Ultra-Fast Silicon Detectors** (UFSD).

Provide in the same detector and readout chain

- Ultra-fast timing resolution [10’s of ps]
- Precision location information [10’s of µm]

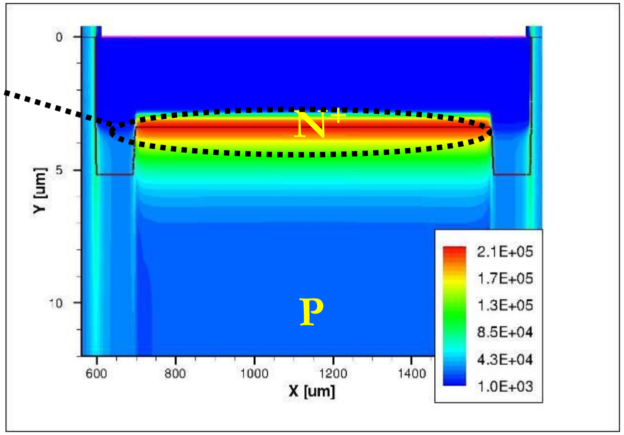
We propose to achieve high electric field is to use thin p-type epitaxyal substrates [1] grown on thick support wafers, p+-type doped, that acts as the backside ohmic contact. Different thicknesses will be used to study the multiplication effect induced by the high electric field at the collecting electrodes, depending on availability we propose to use: 10, 50, 75µm. ***Need very fast pixel readout***.

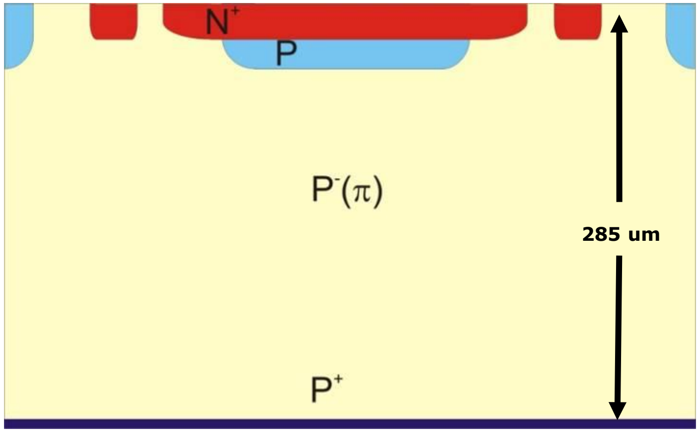
H. Sadrozinski, “Exploring charge multiplication for fast timing with silicon sensors” 20th RD50 Workshop, Bari 2012

2)Low gain avalanche detectors (LGAD)

Crating an n++/p+/p- junction along the centre of the electrodes. Under reverse bias conditions, a high electric field region is created at this localised region, which can lead to a multiplication mechanism.

High Electric Field region leading to multiplication





P. Fernandez et al, "Simulation of new p-type strip detectors with trench to enhance the charge multiplication effect in the n-type electrodes" , Nuclear InstrumentsandMethodsinPhysicsResearchA658(2011) 98–102.