CERN

the ATLAS Experiment

# Overview of the ATLAS Insertable B-Layer (IBL) Project

ATLAS Pixel Detector Collaboration

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on behalf of
the ATLAS
Collaboration

5th Sept. 2013,
9th International
"Hiroshima"
Symposium,
Hiroshima, Japan.

# Introduction

- Motivation
- Overview

# Layout

- Sensors: Planar & 3D
- Testbeam Results
- FE-I4 Readout Chip

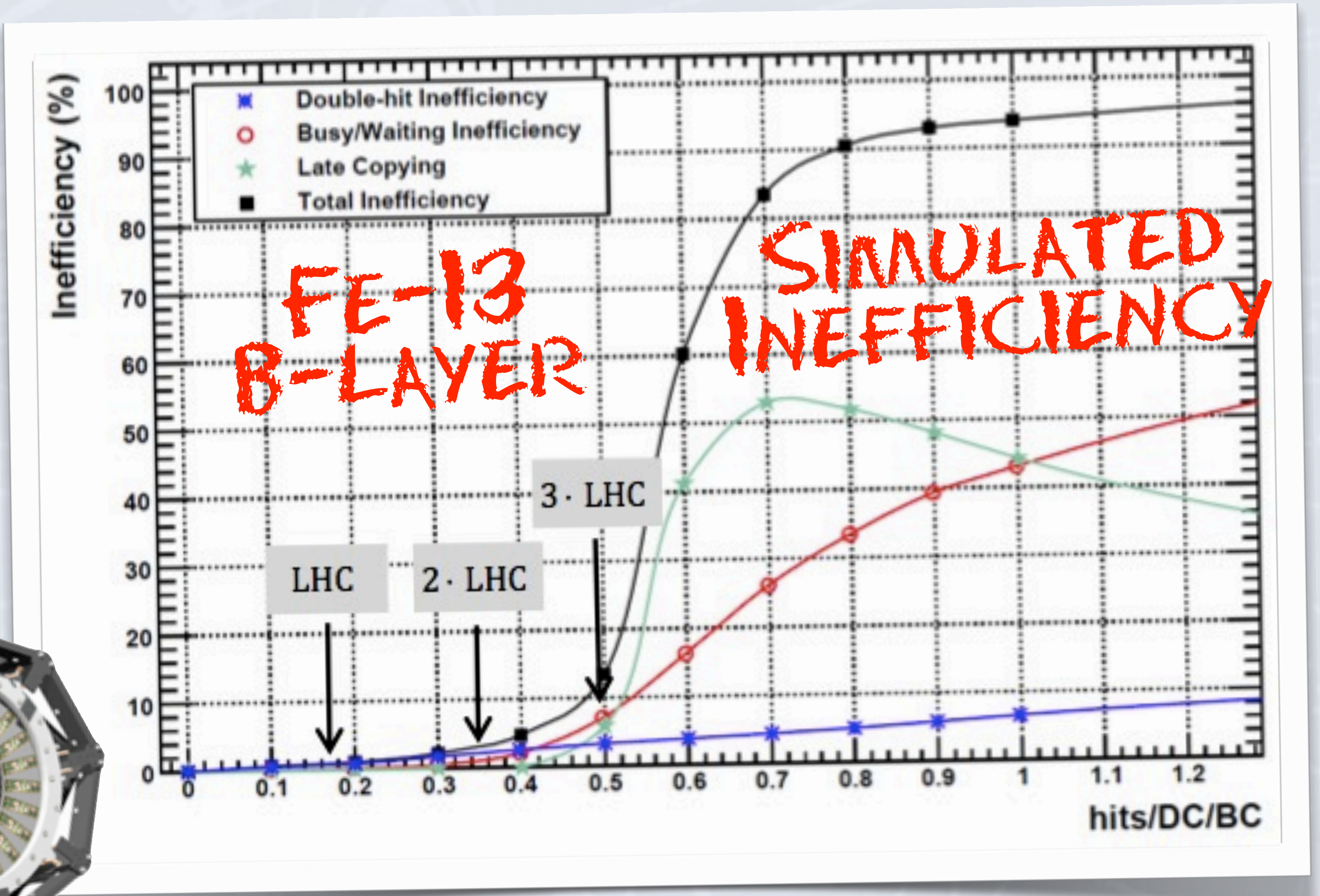
# Production

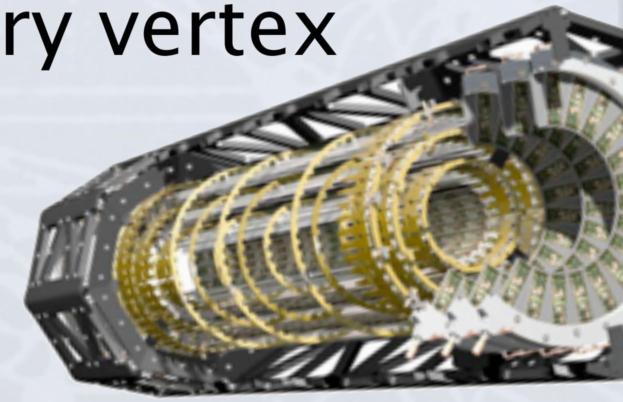
- Modules & Staves
- Quality Assurance

# Conclusions

# Insertable B-Layer Motivation TELL ME WHY!

- Pixel Detector showed great performance over last years (see Timon Heims talk)
- Essential for:
    - b-tagging,
    - tracking and
    - primary vertex

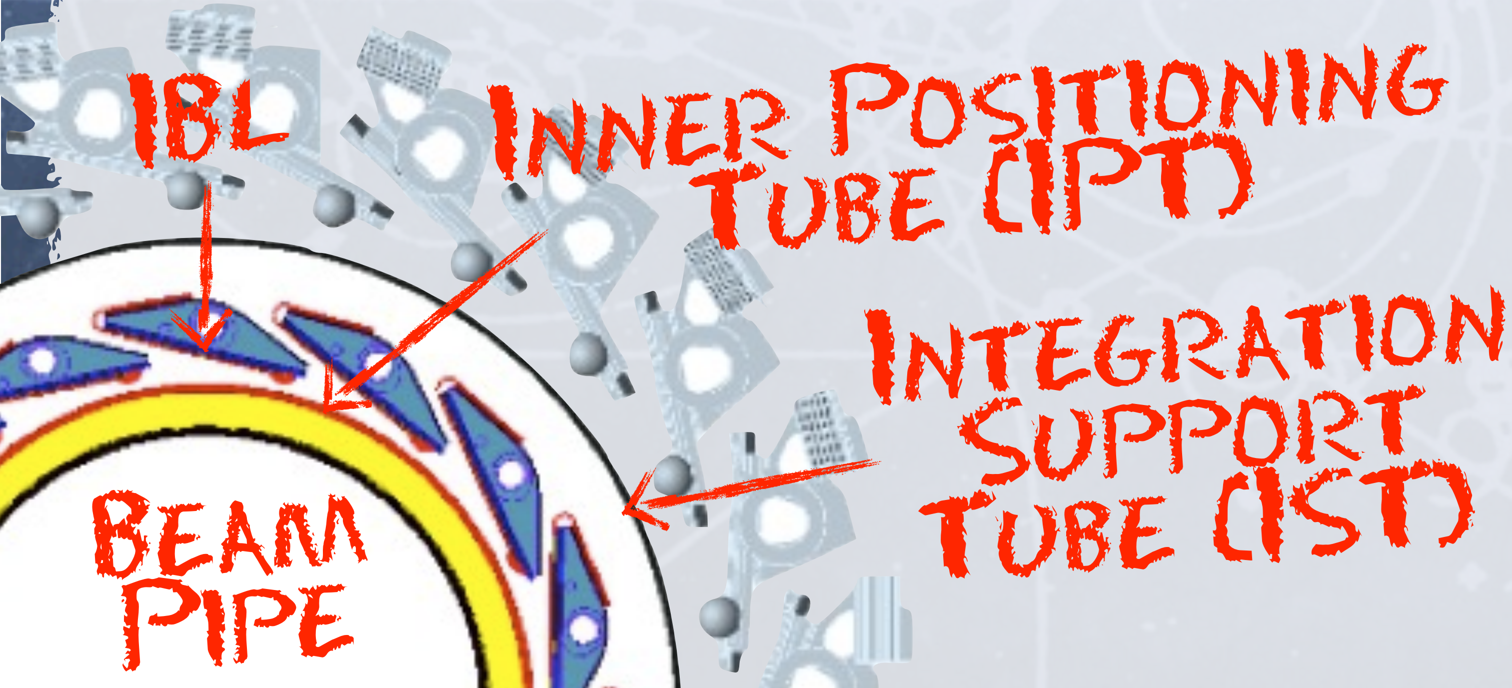


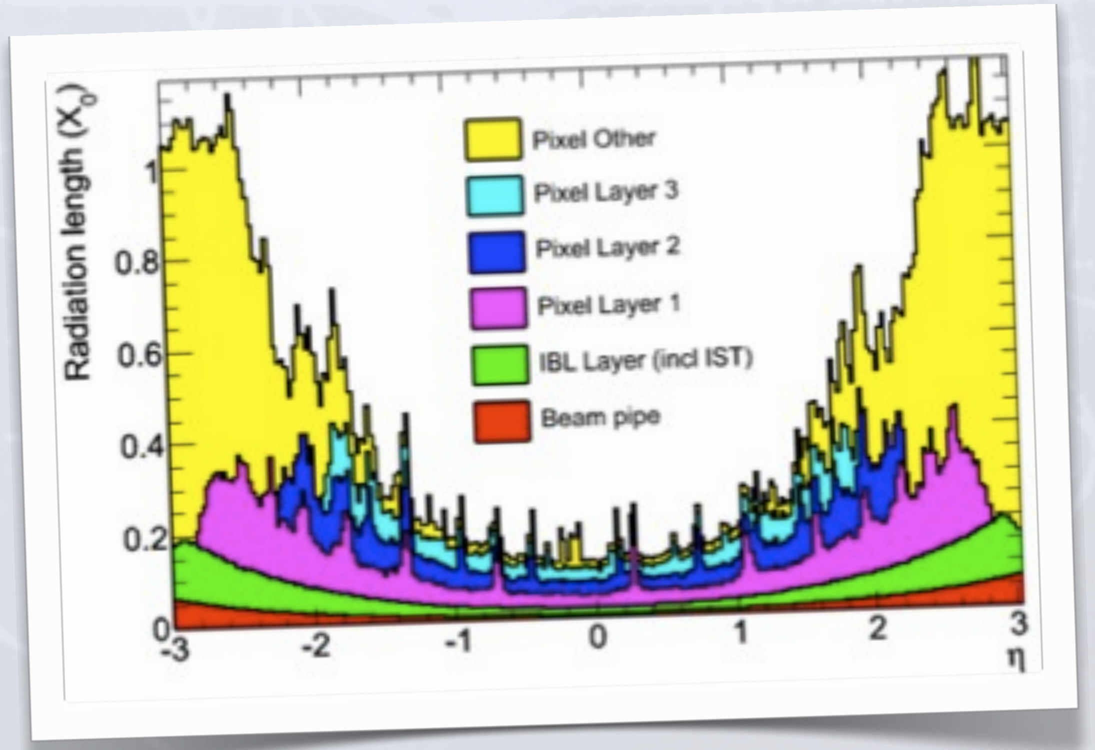


- Large Hadron Collider upgrade: √s 8 TeV → 14 TeV
    - LHC luminosity of $10^{34}$cm$^{-2}$s$^{-1}$ will increase by factor 2-3
    - FE-I3 inefficiency in B-Layer will reach 5% to 10%
- IBL aim: compensate inefficiency & radiation damage losses

# Insertable B-Layer Overview THE BASICS

- New 4th pixel silicon barrel layer with $r = 3.3$ cm, 12 MegaPixel
- Needs small radius ($r = 2.35$ cm) beam pipe
- Inner & outer carbon support tubes (IPT & IST)
- 14 staves with $\Phi = 14^\circ$ tilt angle & no z overlap
- Radiation Length $< 1.9\%\ X/X_0$ using: carbon foam support, Titanium cooling tubes, $CO_2$ cooling
- High track density small radius & high luminosity:
  - increase radiation hardness: $5\cdot10^{15}\ n_{eq}/cm^2$ & 250 MRad TID
  - investigate new sensor technologies: 3D & planar slim edge
  - use new pixel readout chip: FE-I4

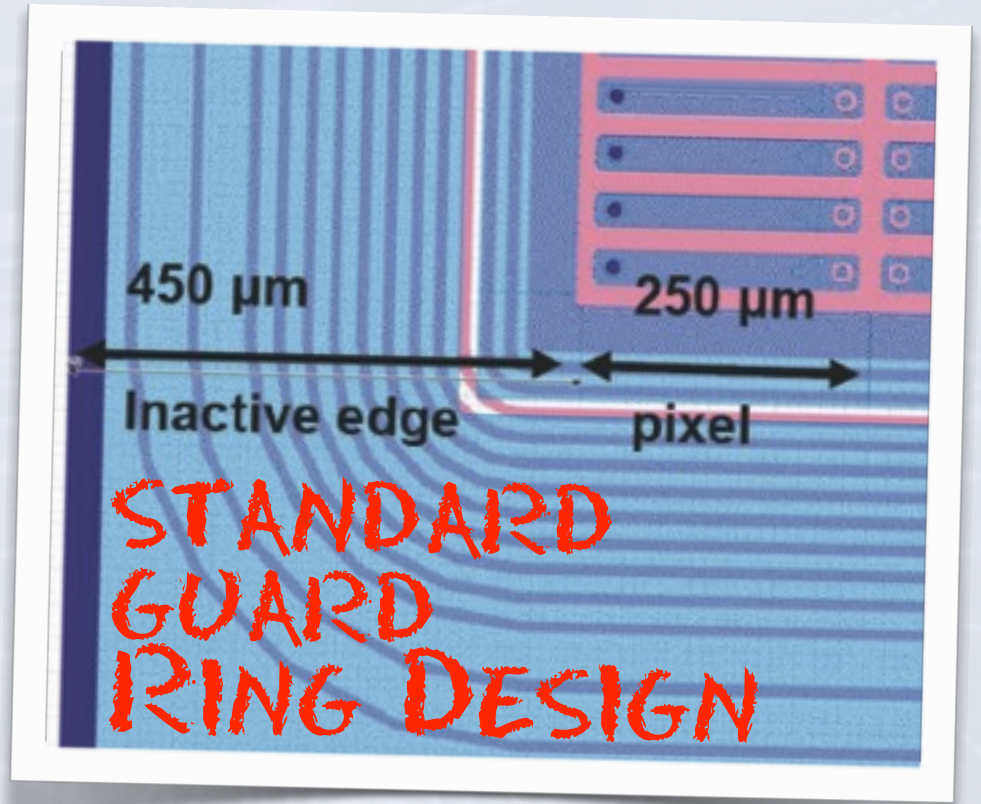


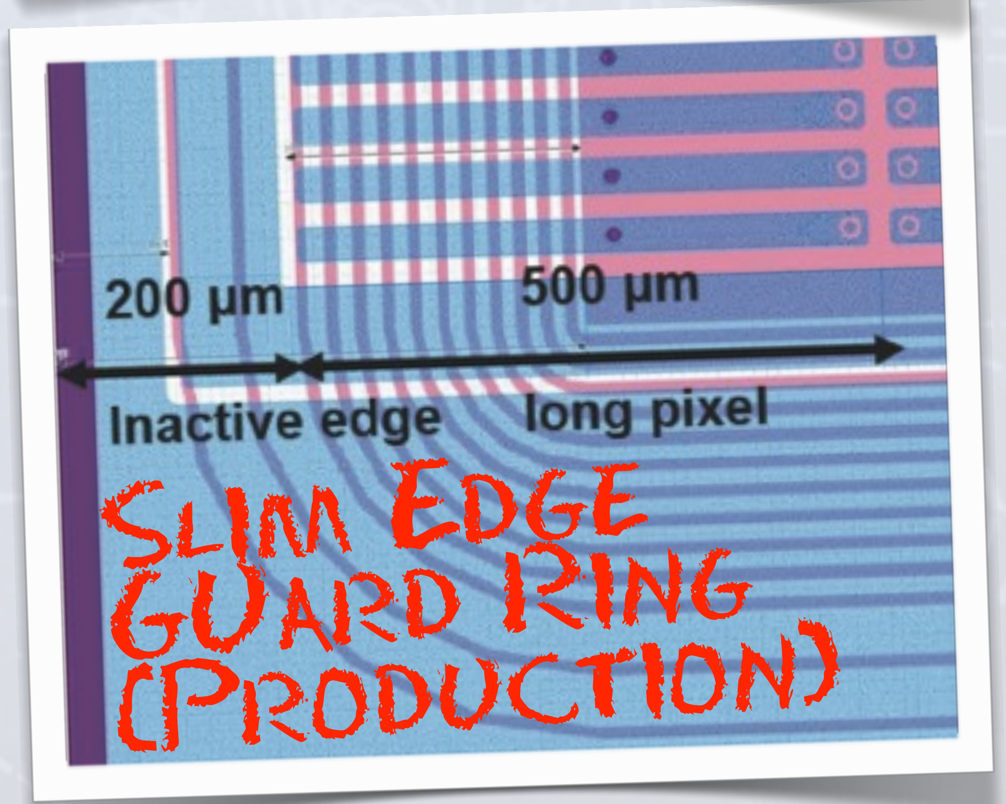


# IBL Planar Sensors

SHORT PIXELS & SLIM EDGE

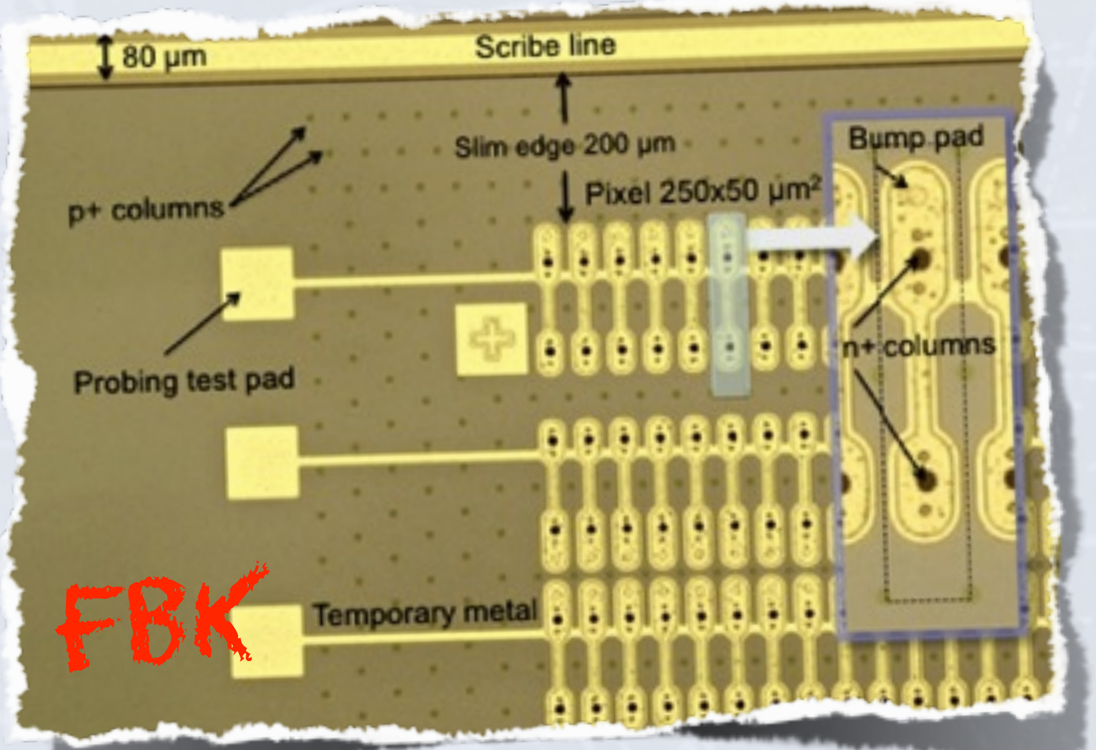
- Planar n-in-n oxygenated Si sensor
- Pixel electrodes on surface of bulk
- Proven ATLAS Pixel Detector technology and vendor: CIS
- Very high yield (90% accepted for IBL production)
- Reduced:
  - Pixel size 400 μm → 250 μm
  - Thickness 250 μm → 200 μm
  - Inactive edge 450 μm → 200 μm
  - Depletion voltage: 35 V
- Increased radiation hardness: $5 \cdot 10^{15}$ $n_{eq}/cm^2$ & 250 MRad TID
- 26880 pixel per FE-I4 readout chip

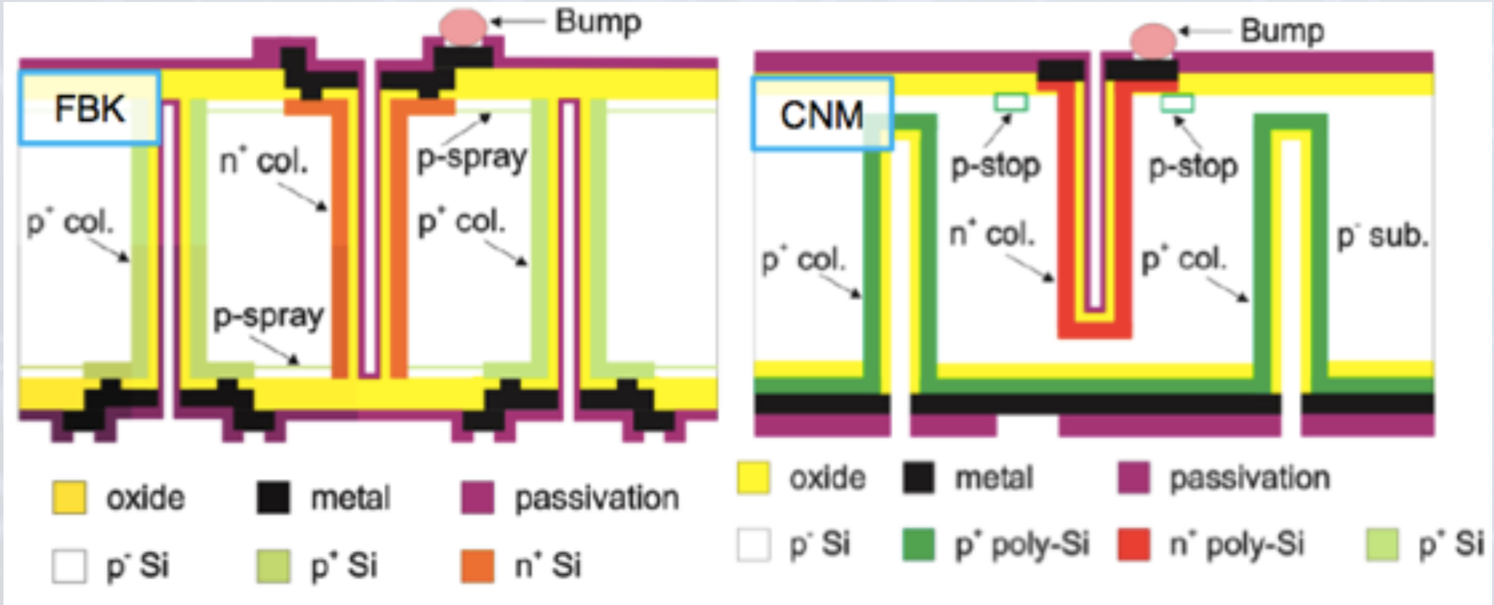


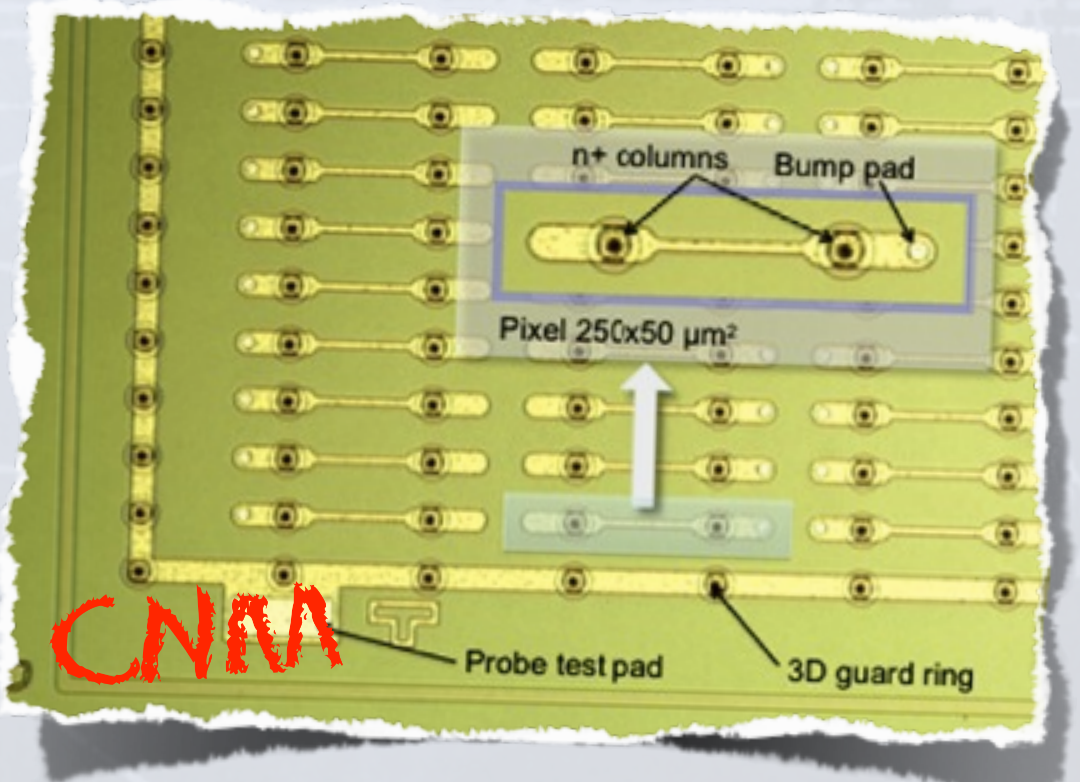


# IBL 3D FBK & CNM Sensors

- 3D double sided silicon sensors with vertical 2E electrodes used at high eta reduce collection time & depletion voltage
- 230 µm thickness
- Depletion voltage: 15 V
- Two 3D sensor vendors
- Acceptable yield (60% for IBL)

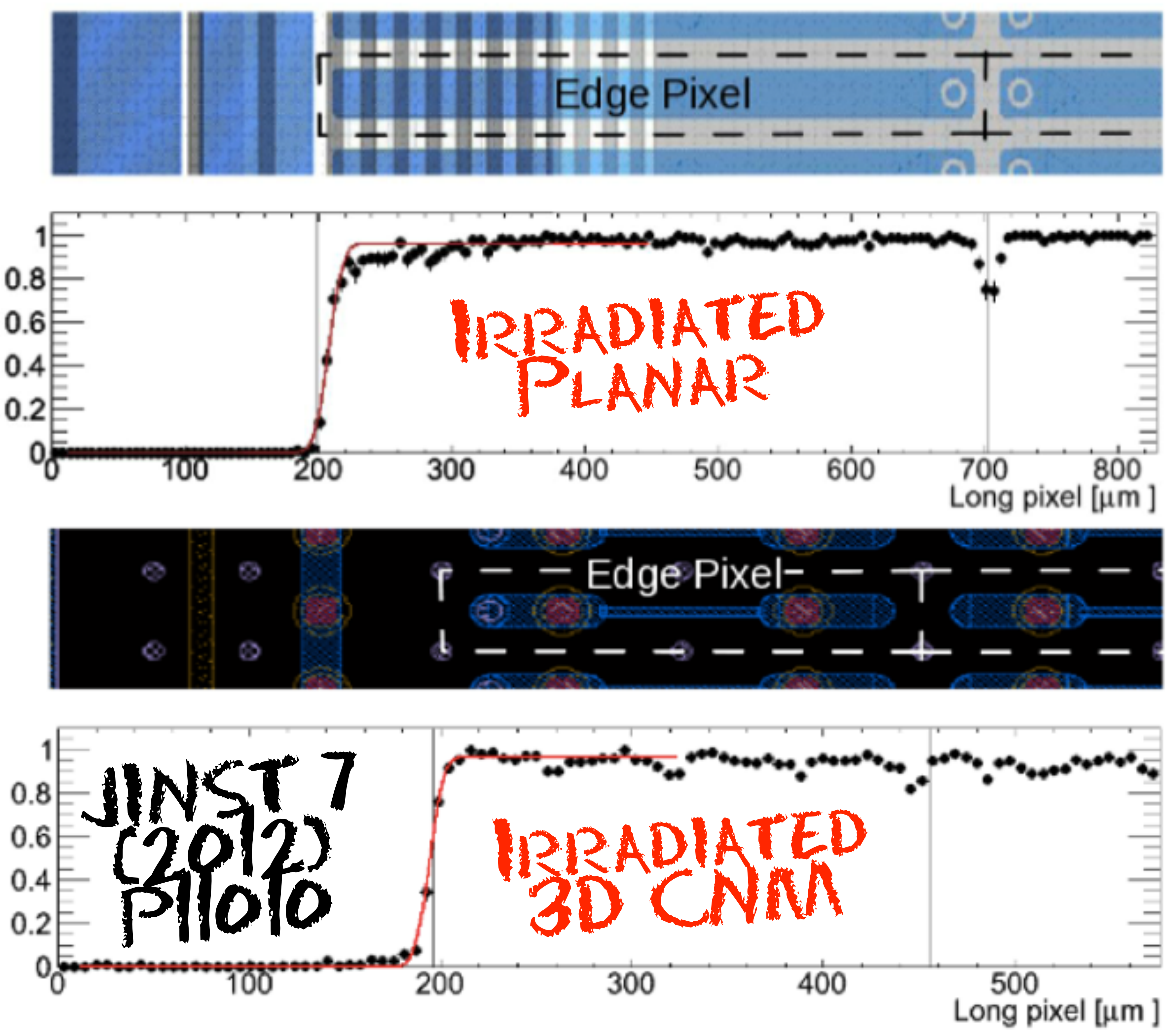






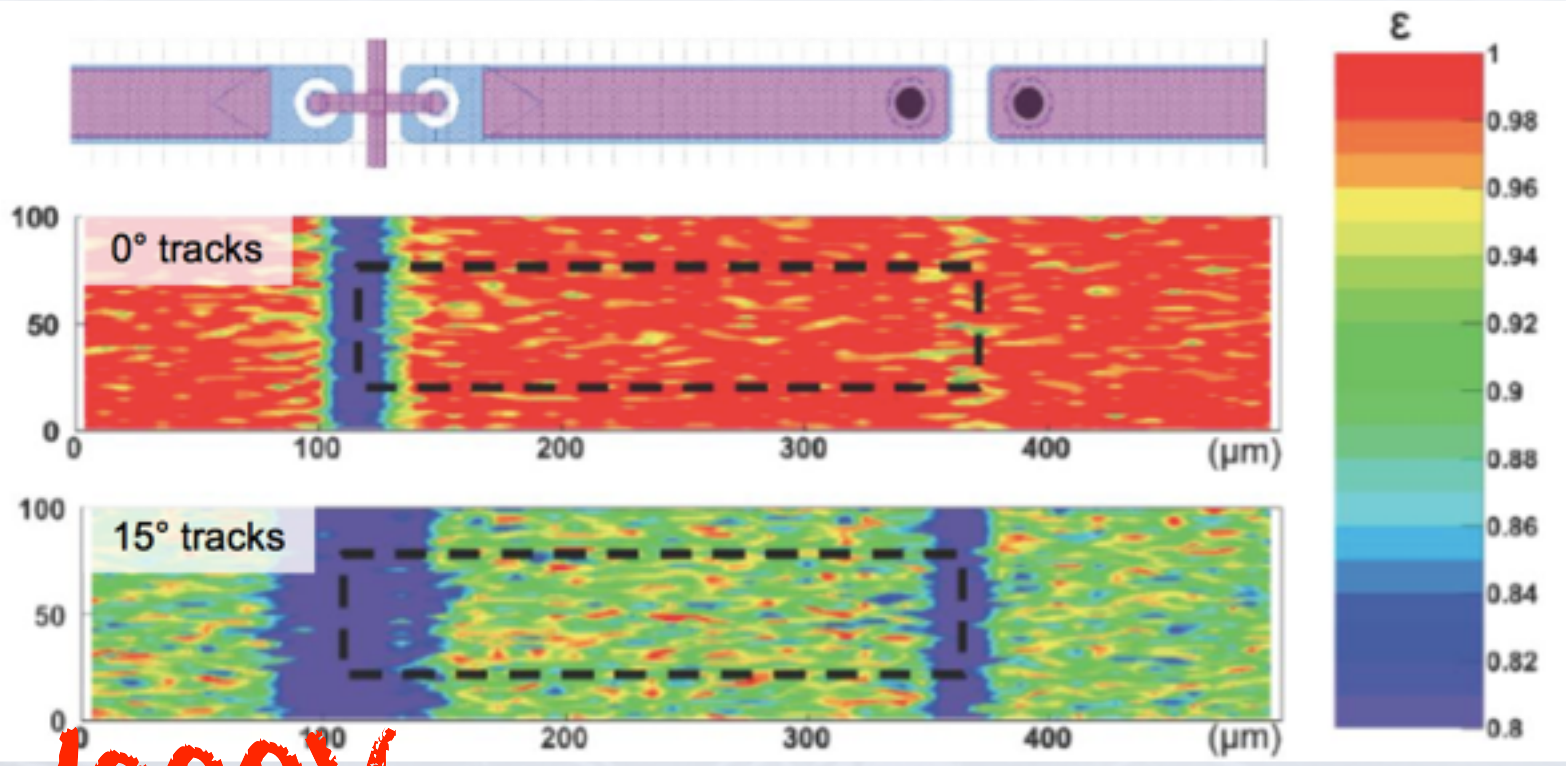
# Testbeam Slim Edges Planar & 3D

- Several testbeams at DESY & CERN
- High efficiency confirmed with EUDET telescope runs
- results as expected for resolution, cluster size, and time-over-threshold (TOT) based Landau shape



JINST 7 (2012) P11010

# Testbeam Efficiencies PLANAR & 3D



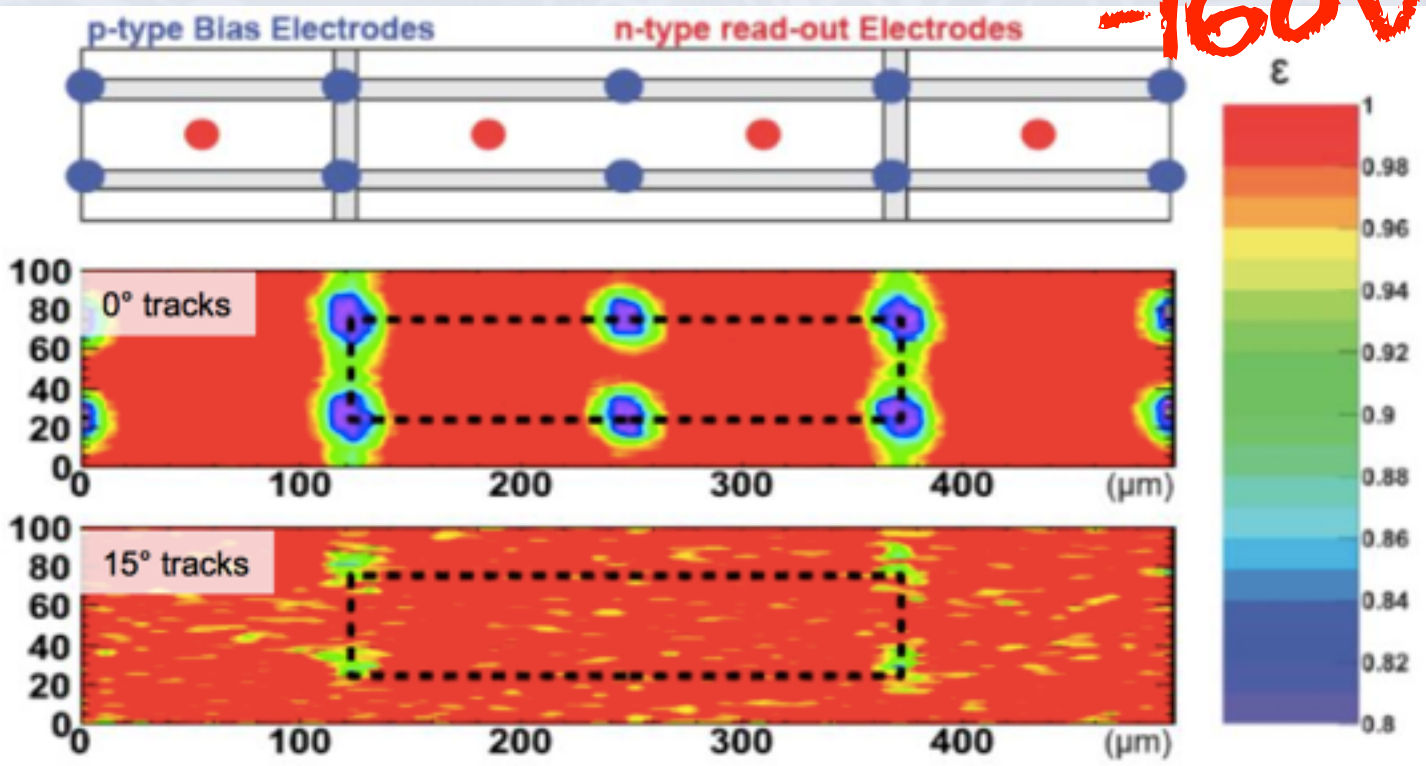
-1000V

## IRRADIATED PLANAR

- $6 \cdot 10^{15}$ $n_{eq}/cm^2$
- 96.9% overall efficiency at 0°
- 86.4% overall efficiency at 15°

## IRRADIATED 3D CNM

- $5 \cdot 10^{15}$ $n_{eq}/cm^2$
- 97.5% overall efficiency at 0°
- 99.0% overall efficiency at 15°



-160V

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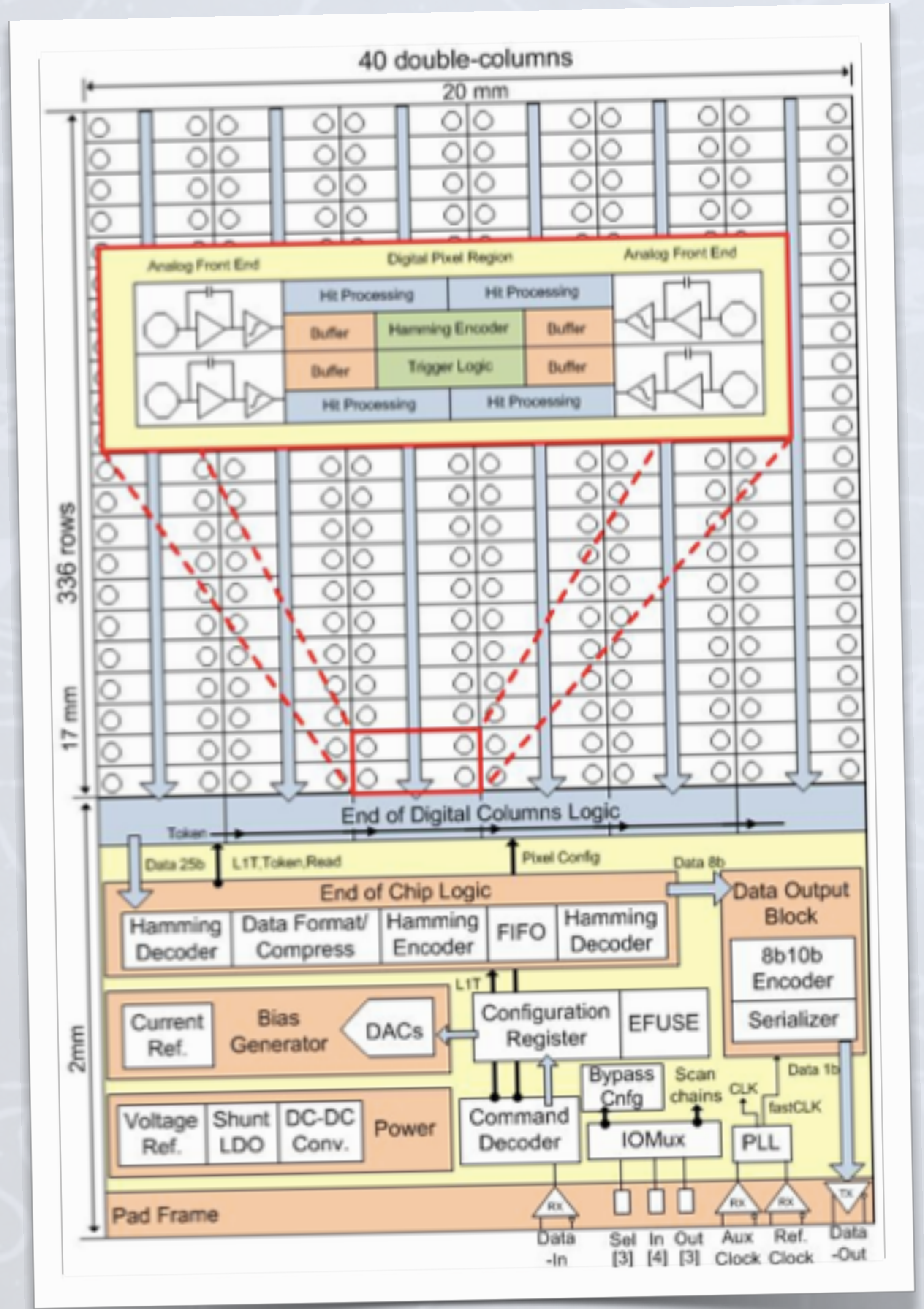
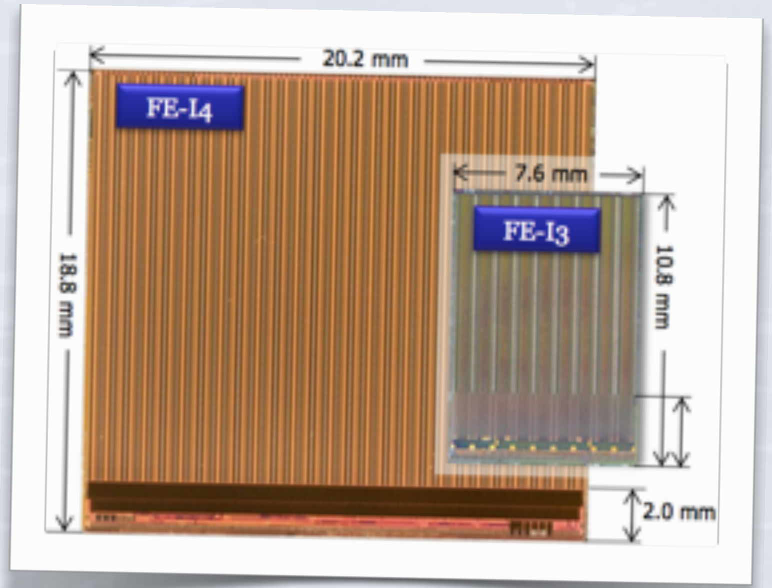
# New Readout Chip FE-I4



- ~ 2 x 2 cm$^2$
- 87M transistors
- 26880 pixels
- 89% active area



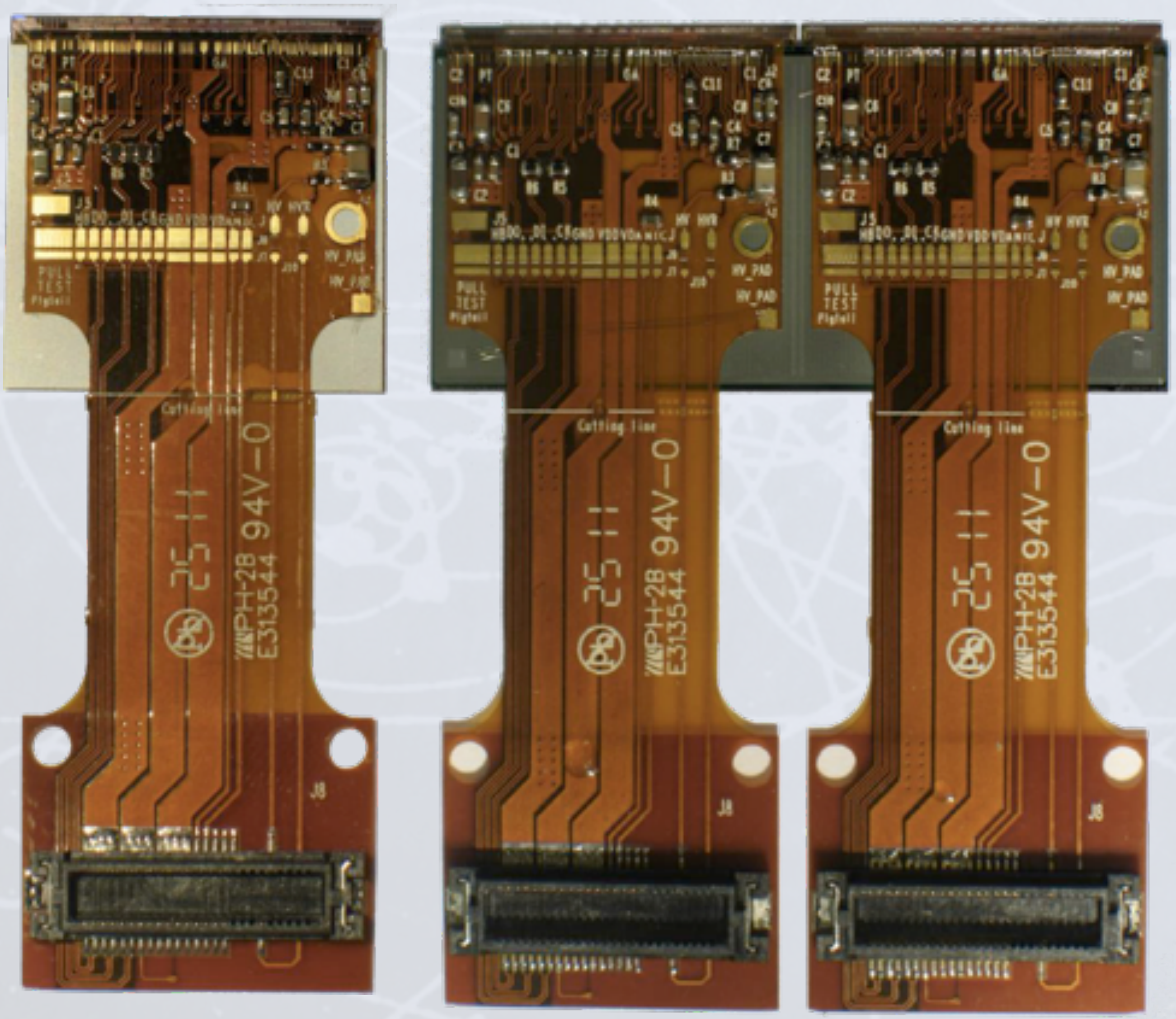
- 130nm front-end chip can cope with higher radiation levels (750 MRad) and larger occupancies
- Local hit storage (four pixel region) supports higher occupancies without saturation
- Balanced outputs allow higher data transmission rates
- Low drop out regulators (LDO)

# IBL Modules and Staves

Silicon & Kapton

Single Chip (SC) 3D

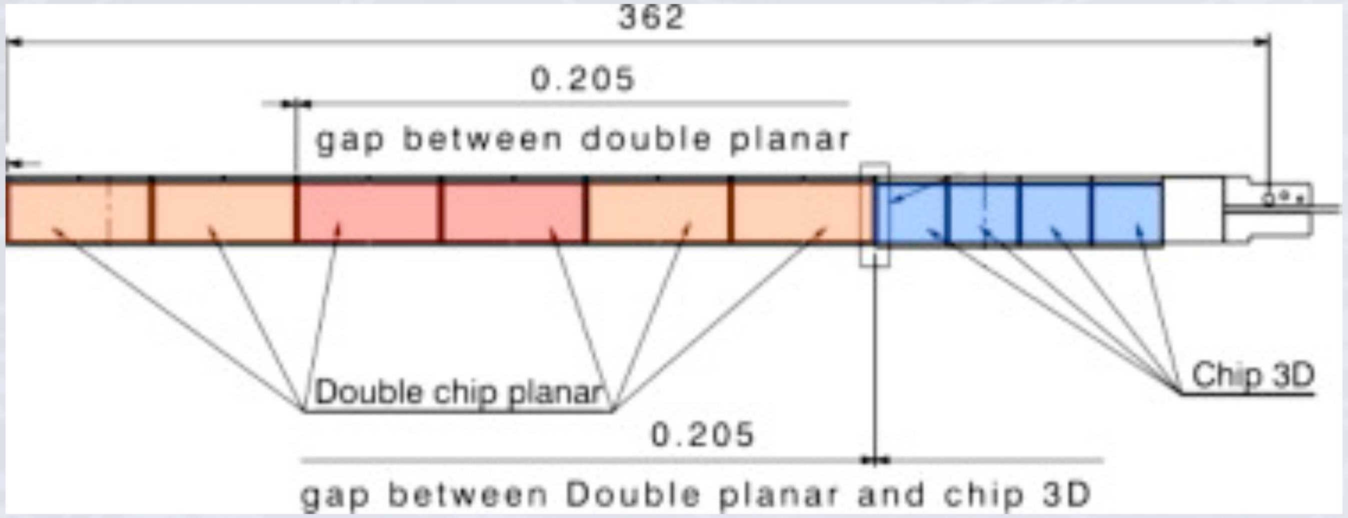
Double Chip (DC) Planar



- Bare module assembly (IZM, Berlin)
  - 150 µm thinning of FE-I4 with glass handling wafer
  - Dicing
  - Bump bonding of sensor and FE(s)
  - Laser release of glass
- Module assembly (Bonn & Genova)
  - Flex to bare module glueing
  - Wire bonding
  - Quality assurance & burn-in

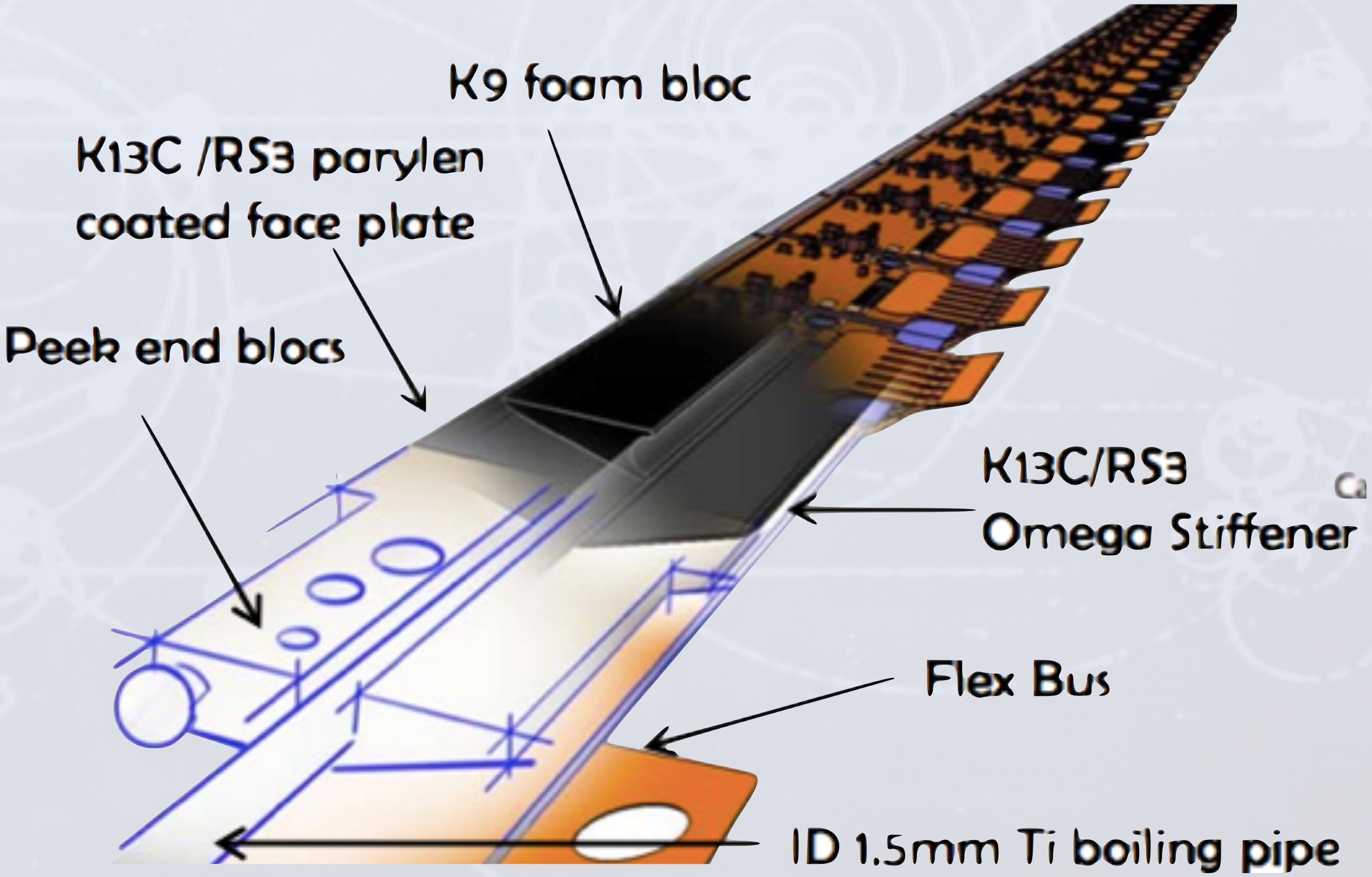
# IBL Modules and Staves

CARBON & TITANIUM

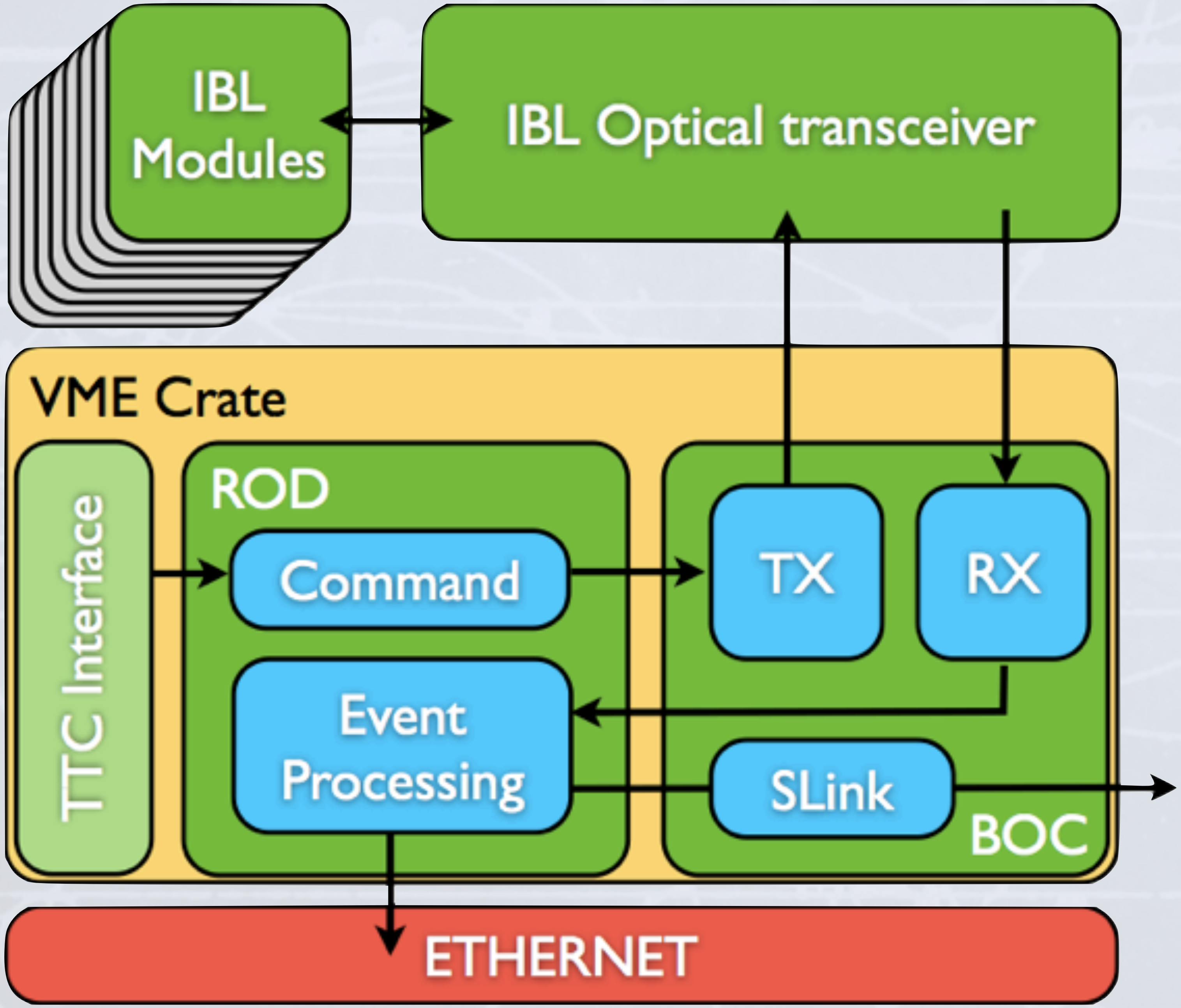


- carbon foam with carbon fibre laminate bare stave
- embedded Titanium $CO_2$ cooling tube
- Flex PCB bus with Cu (signal & HV) & Al (power) lines
- Flex module wings
- Module loading in Geneva

- 14 staves a 32 FE-I4s
- 25% 3D single chip (SC) modules
- 75% planar double chip modules (DC)
- 2DC/4SC = power group

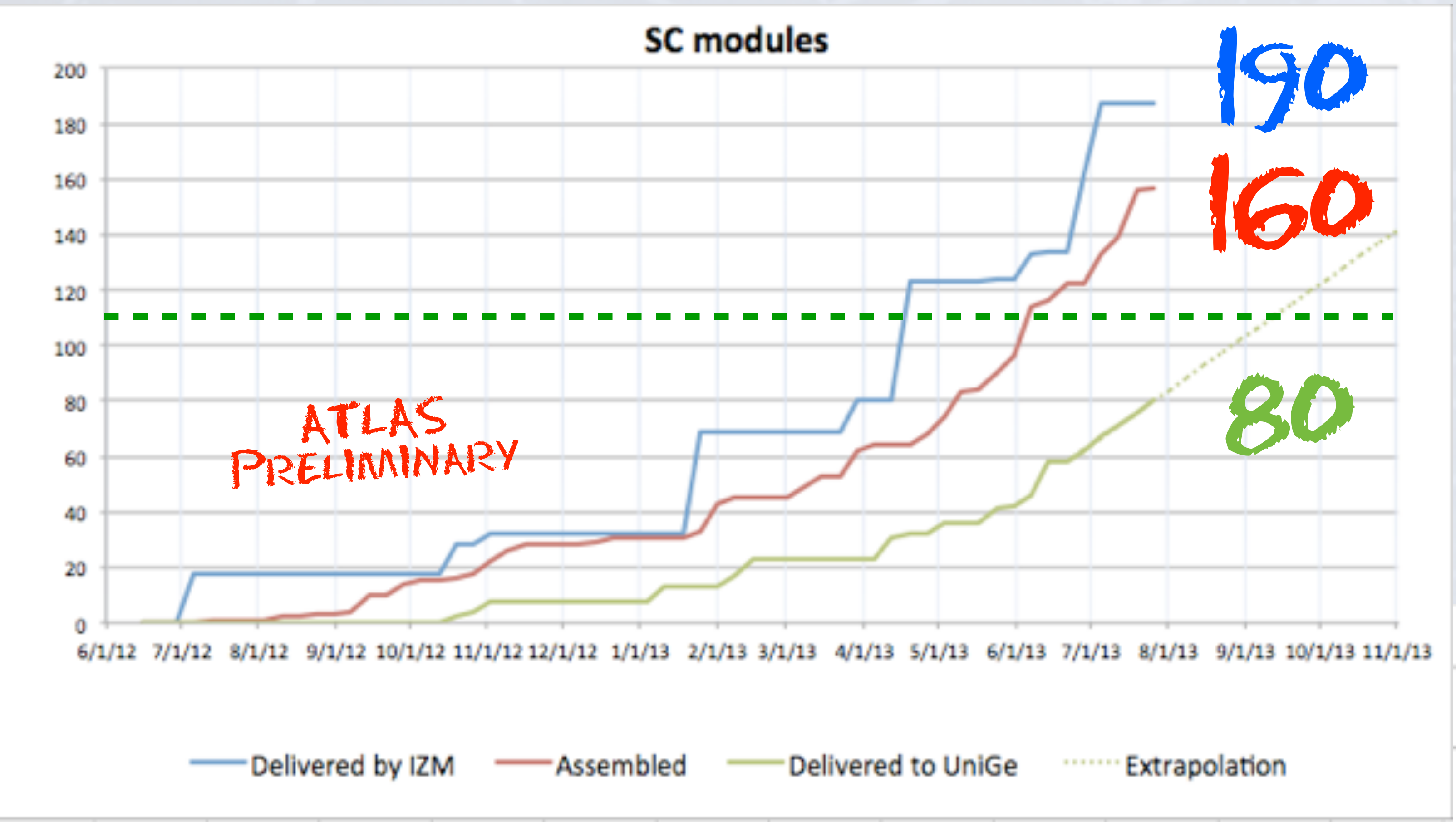


# Readout Structure RODs & BOCs



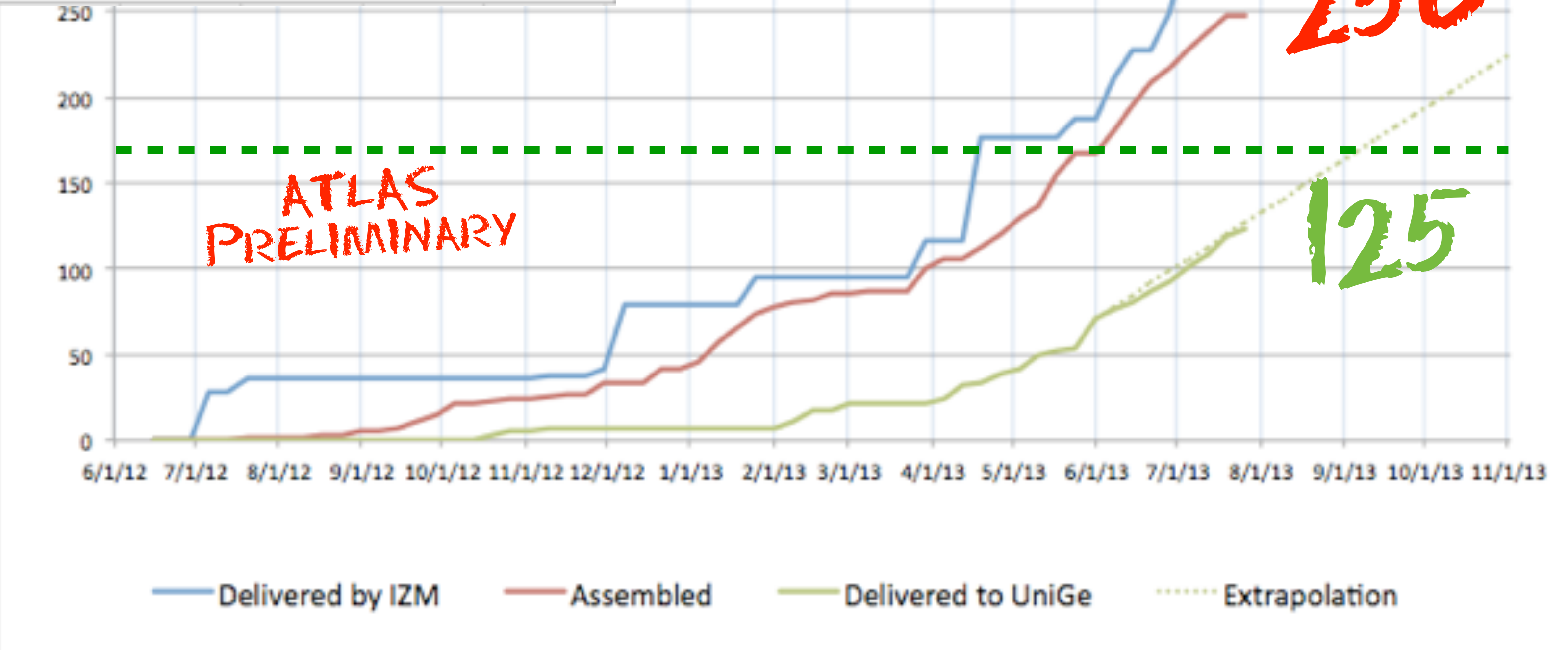
- New Readout Driver (ROD), new Back-of-Crate Card (BOC)
- Higher data flow density, ~ 6Gbit/s per card
- Off-the-shelve transceiver components for detector communication
- Ethernet base-layer for control and calibration to overcome VME bottleneck

# Module Production BONN & GENOVA

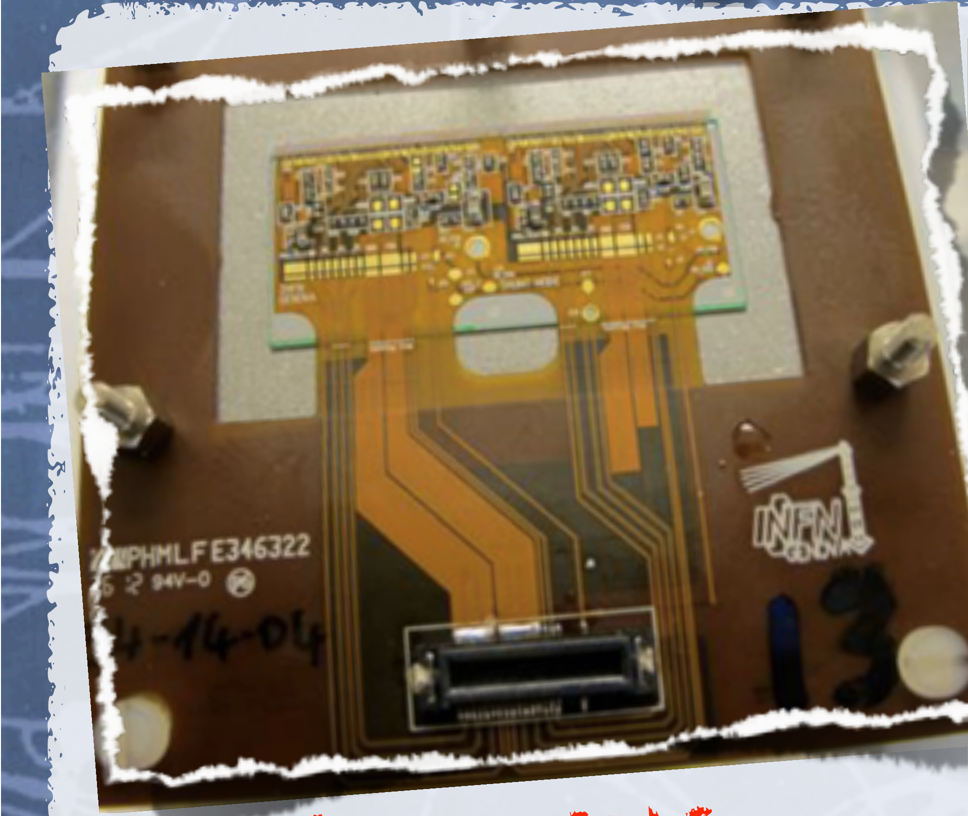


- Module production more than half way done (of 168+112 total modules)
- Should be finished in September

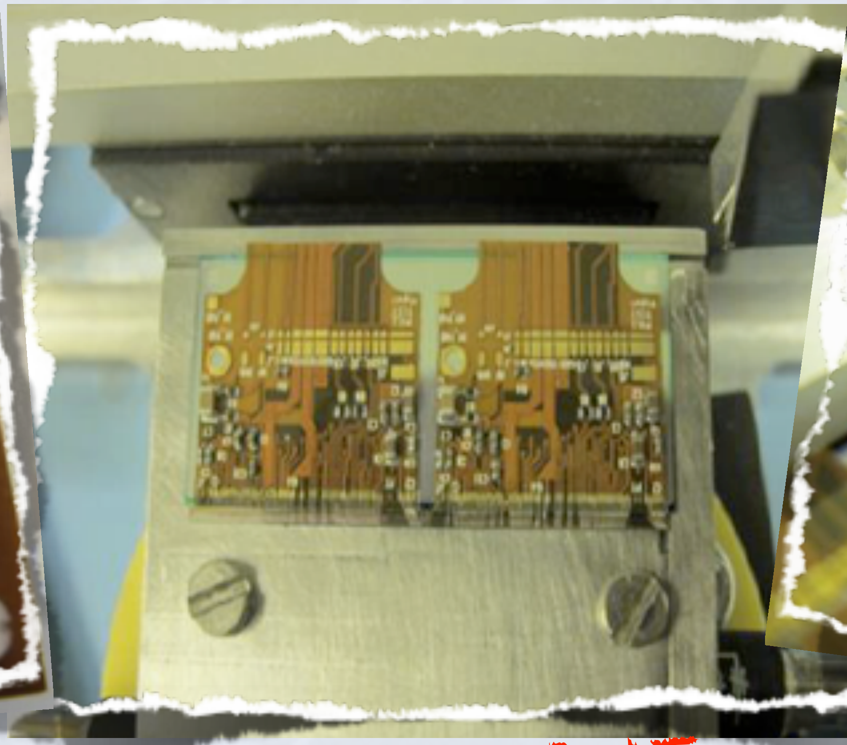
- Assembly test at 15˚C
- 10x -40…+40˚C thermal cycling during burn-in
- Qualification at -20˚C
- Ranking



# Stave Loading GENEVA

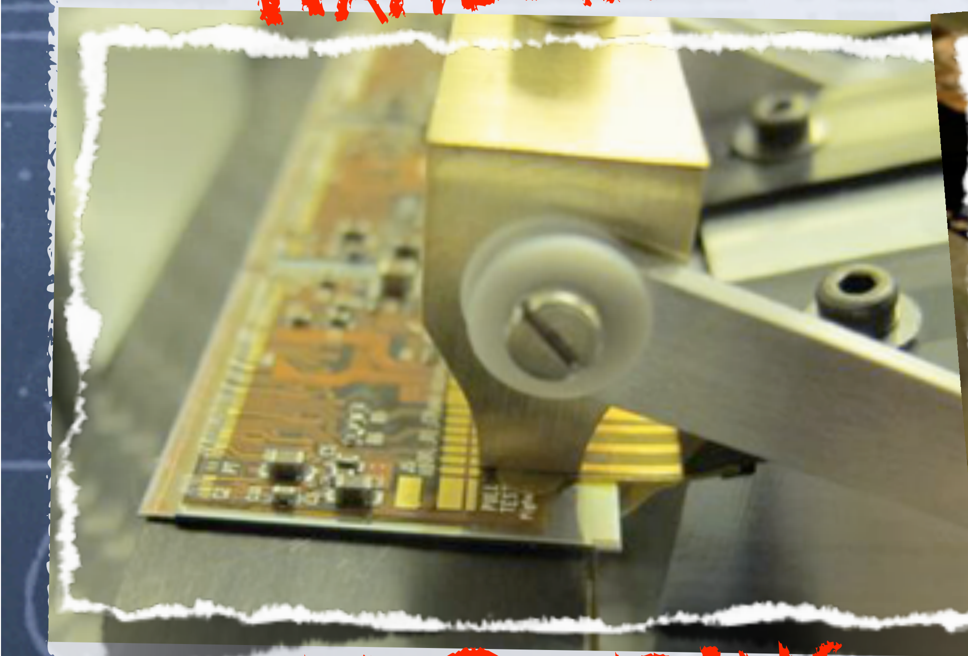


HANDLING



GUILLOTINE

LOADING



WING BENDING

WIRE BONDING

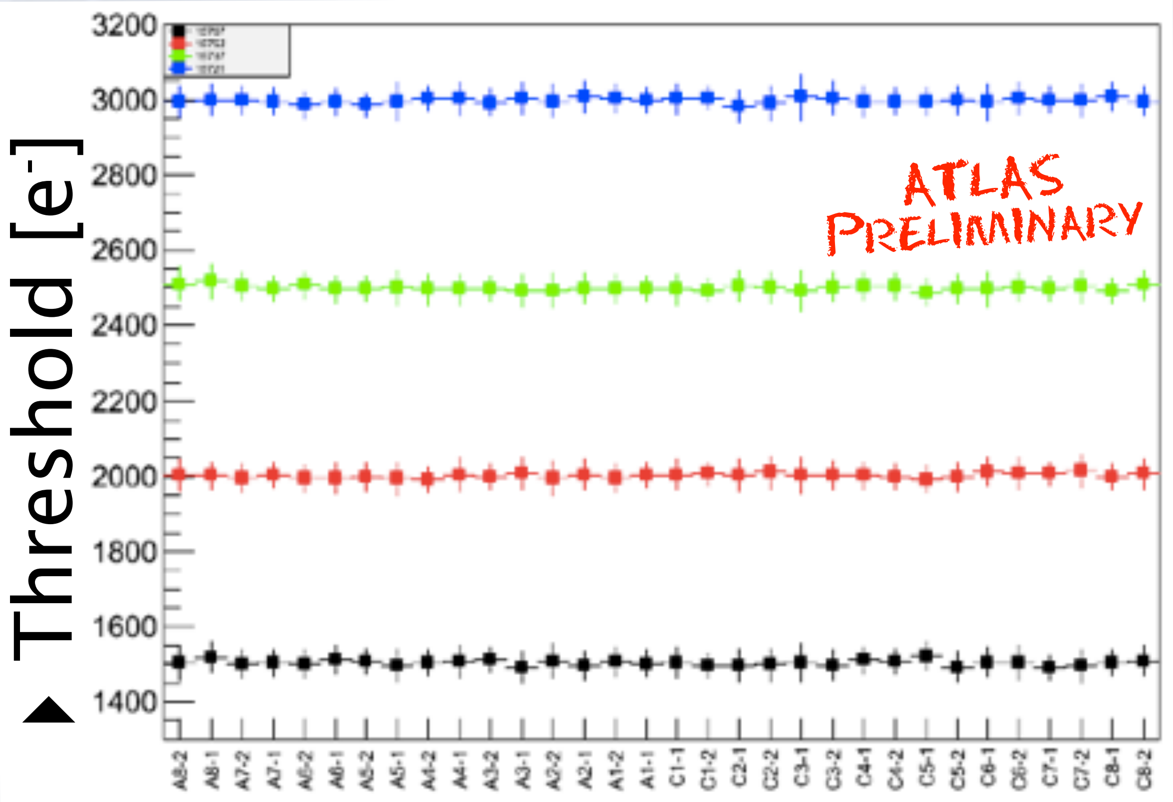
WIRE PULL TEST

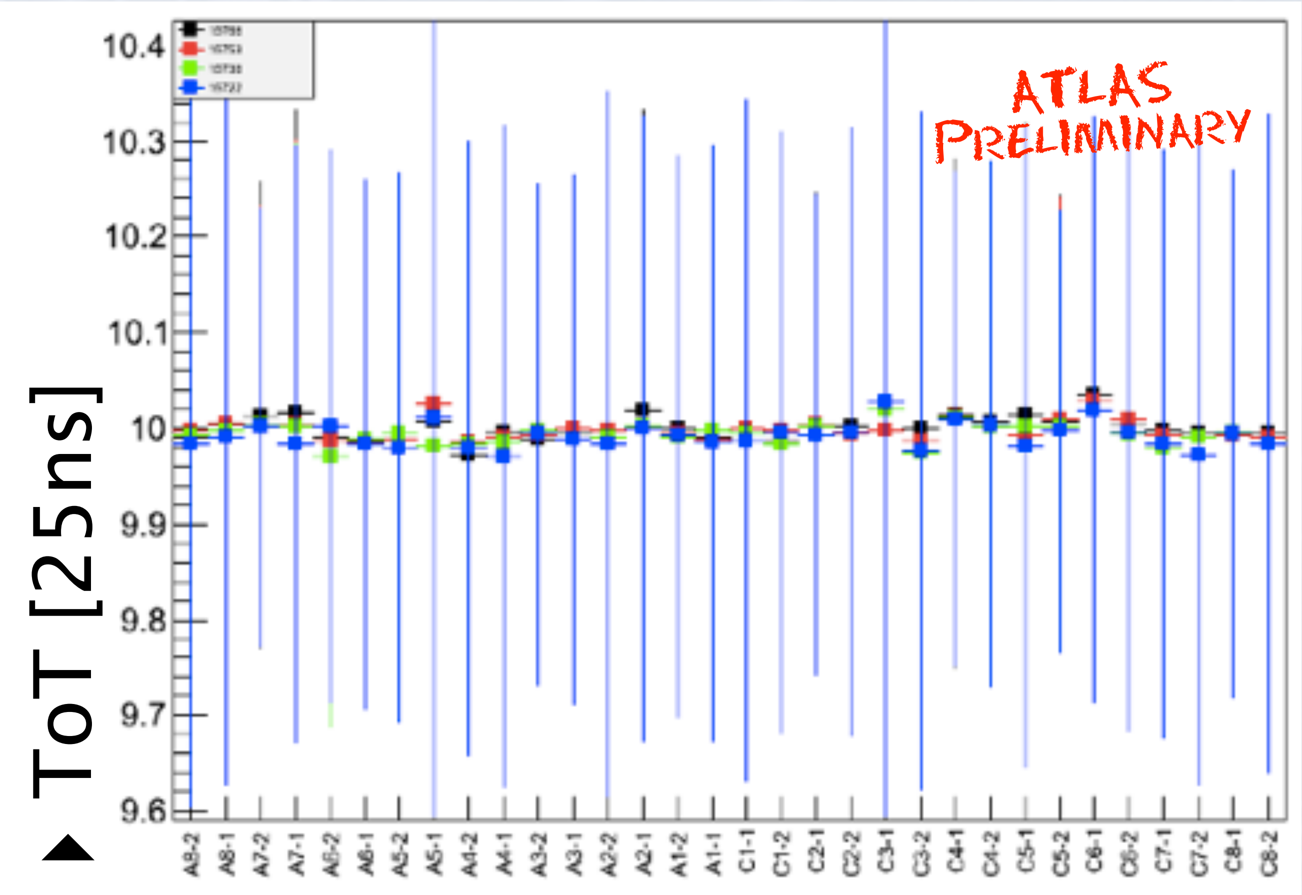
# Stave Quality Assurance AT CERN

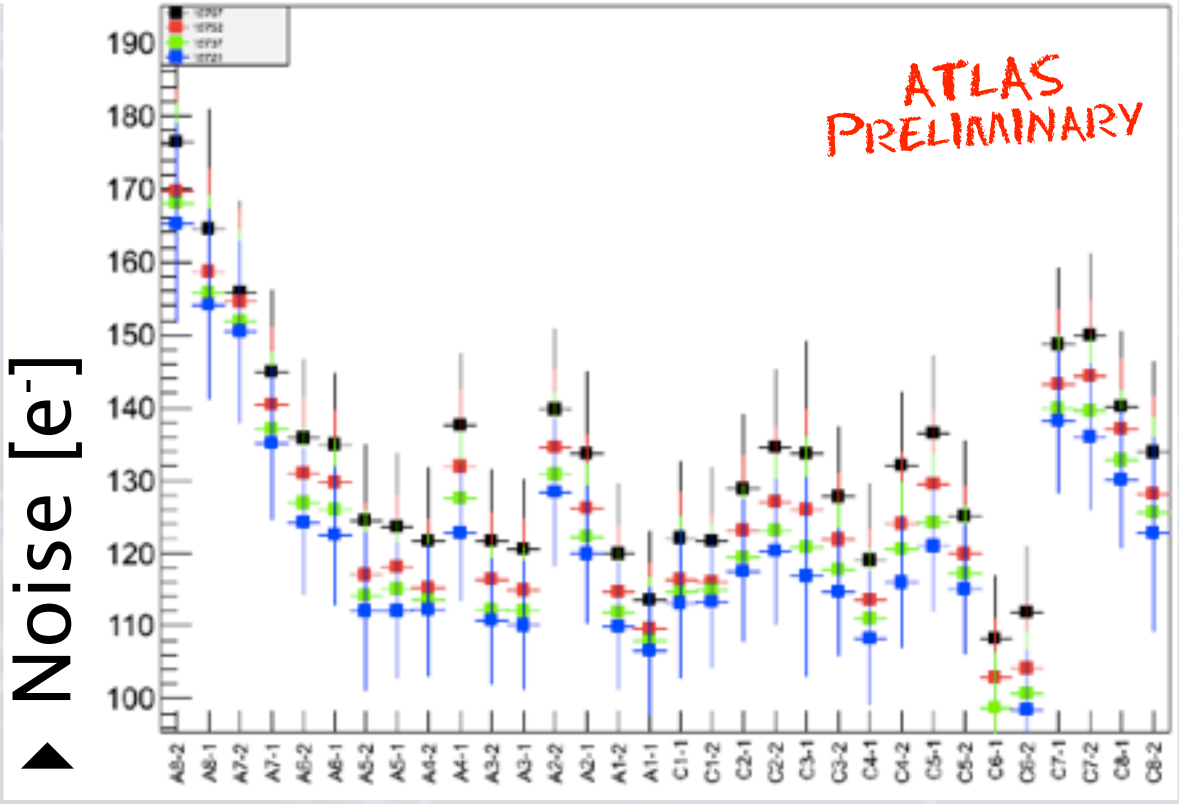
- Reception tests (10°C)
    - Communication (eye diagrams, register tests)
    - Power up studies
    - Comparison with Geneva results
    - Sensor IVs & warm tunings
- Operation tuning (-20°C)
    - 10 TOT @ 16 $\text{ke}^-$
    - 3, 2.5, 2, 1.5 $\text{ke}^-$ threshold
    - Noisy and stuck pixel masks

- Operation (-20°C)
    - $^{241}$Am and $^{90}$Sr source scans with self-trigger
    - Cosmic run (with trigger scintillator)
    - Double trigger
    - ...

# Highlights from the STAVE Quality Assurance





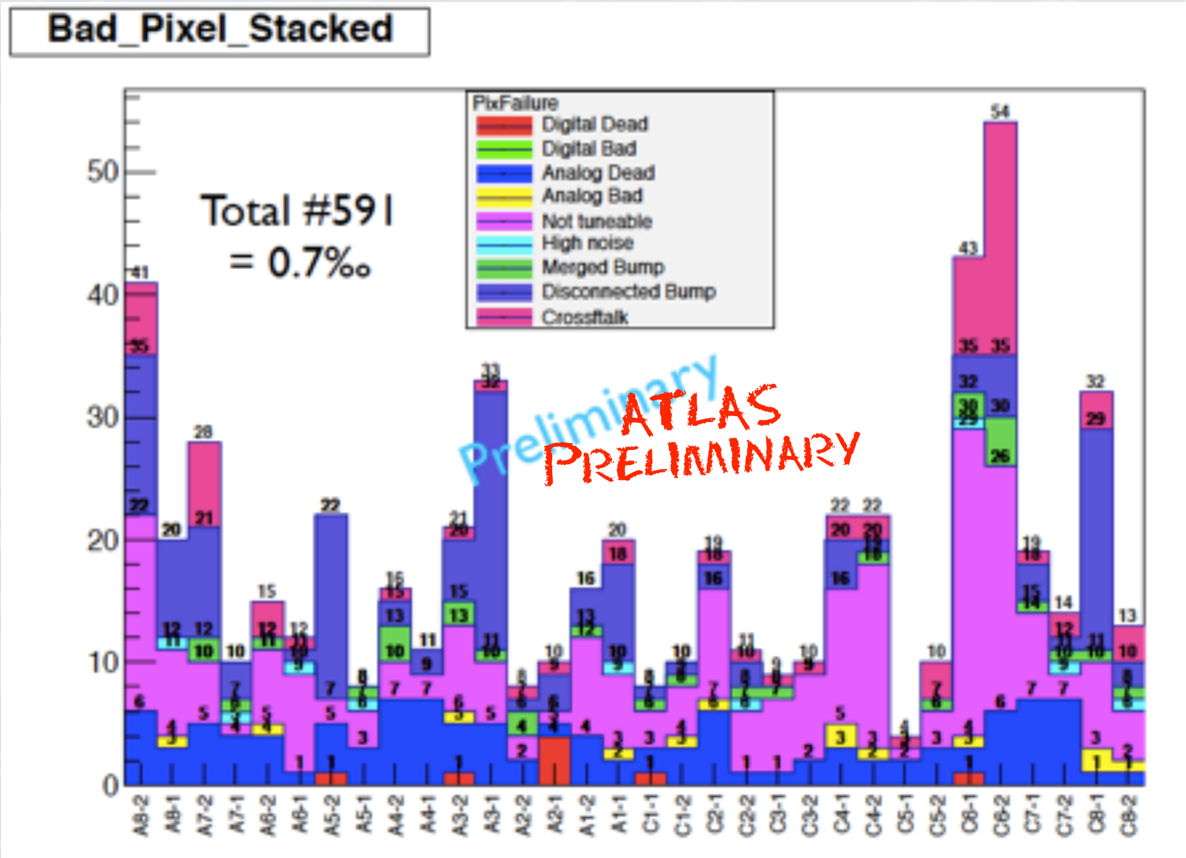


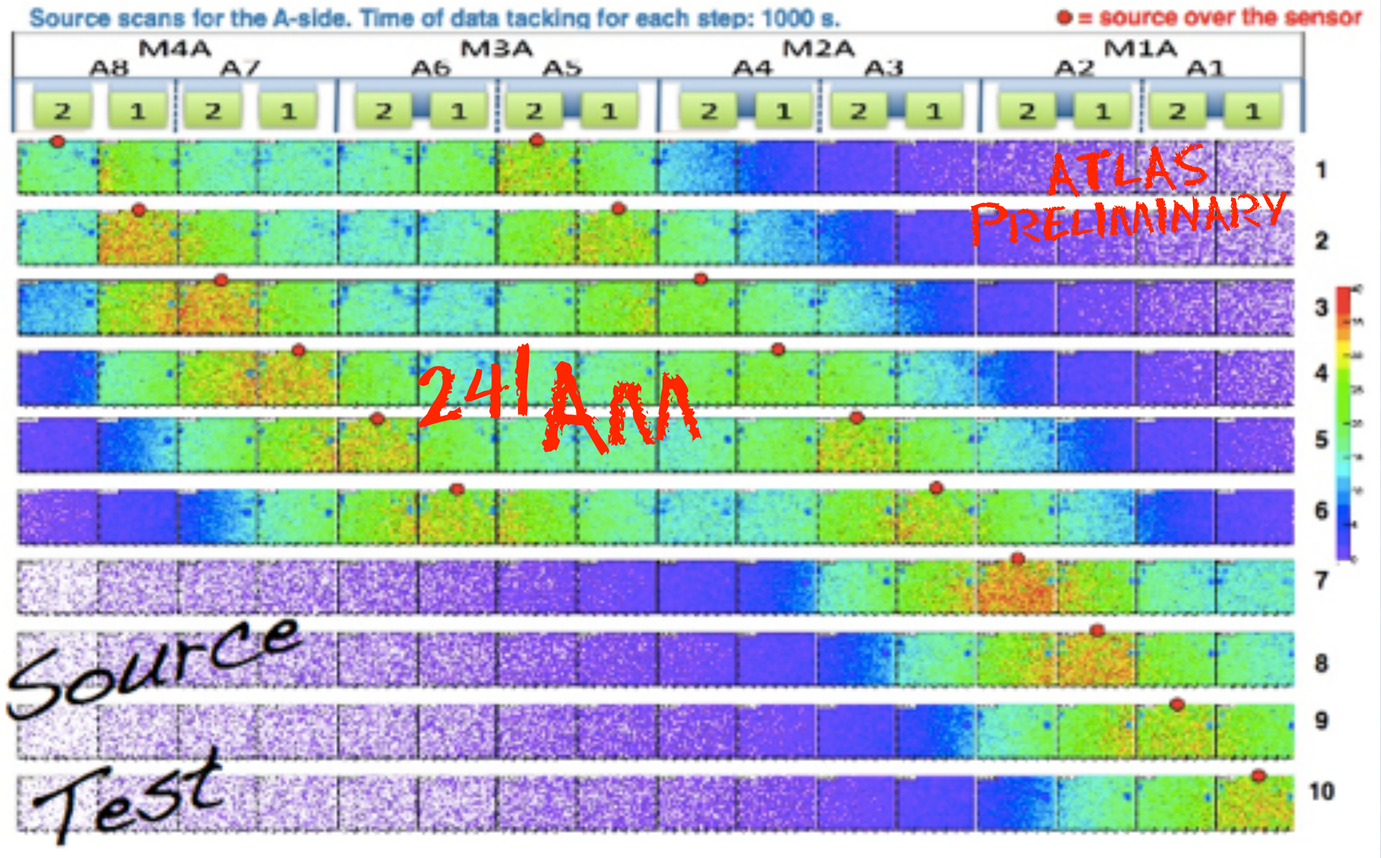
- 8 Staves assembled and 6 fully qualified up to now

3000E-
2500E-
2000E-
1500E-

THRESHOLD WITH 10 TOT AT 16KE-

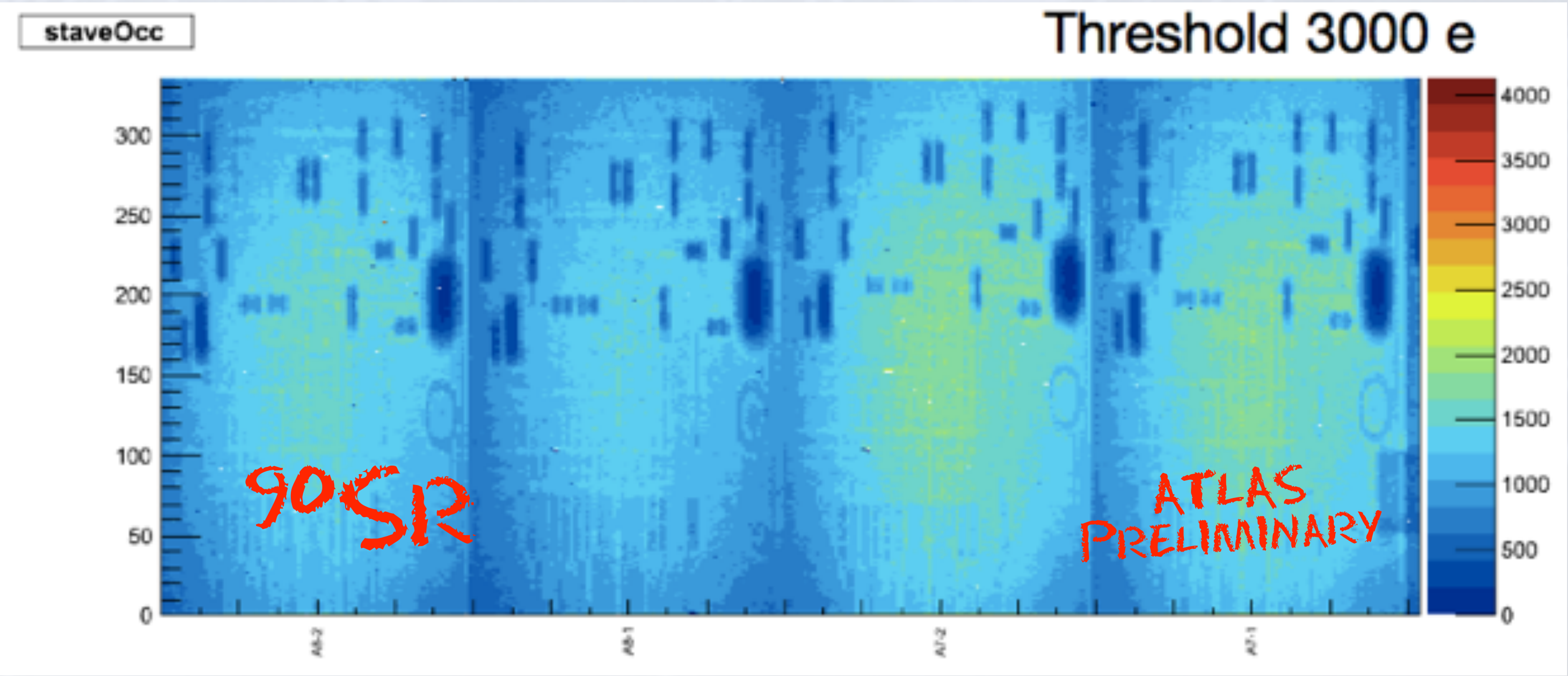
# Highlights from the STAVE Quality Assurance




Source scans for the A-side. Time of data tacking for each step: 1000 s.

● = source over the sensor

- Source scans with $^{241}$Am & $^{90}$Sr as well as cosmics runs show pixel functionality and allow charge calibration



# IBL Stave Integration AT CERN

# Conclusions

## Summary

- New innermost ATLAS silicon layer using 3D and planar slim edge sensors
- Chip and sensor show good yields
- Module production and stave loading currently ongoing
- Stave integration about to start

## Outlook

- September: Finish module testing
- November: Finish stave loading and testing
- April 2014: Integration to Pixel Detector

# Backup Slide

## IV Curves