Design and characterization of novel monolithic pixel sensors for the ALICE ITS upgrade

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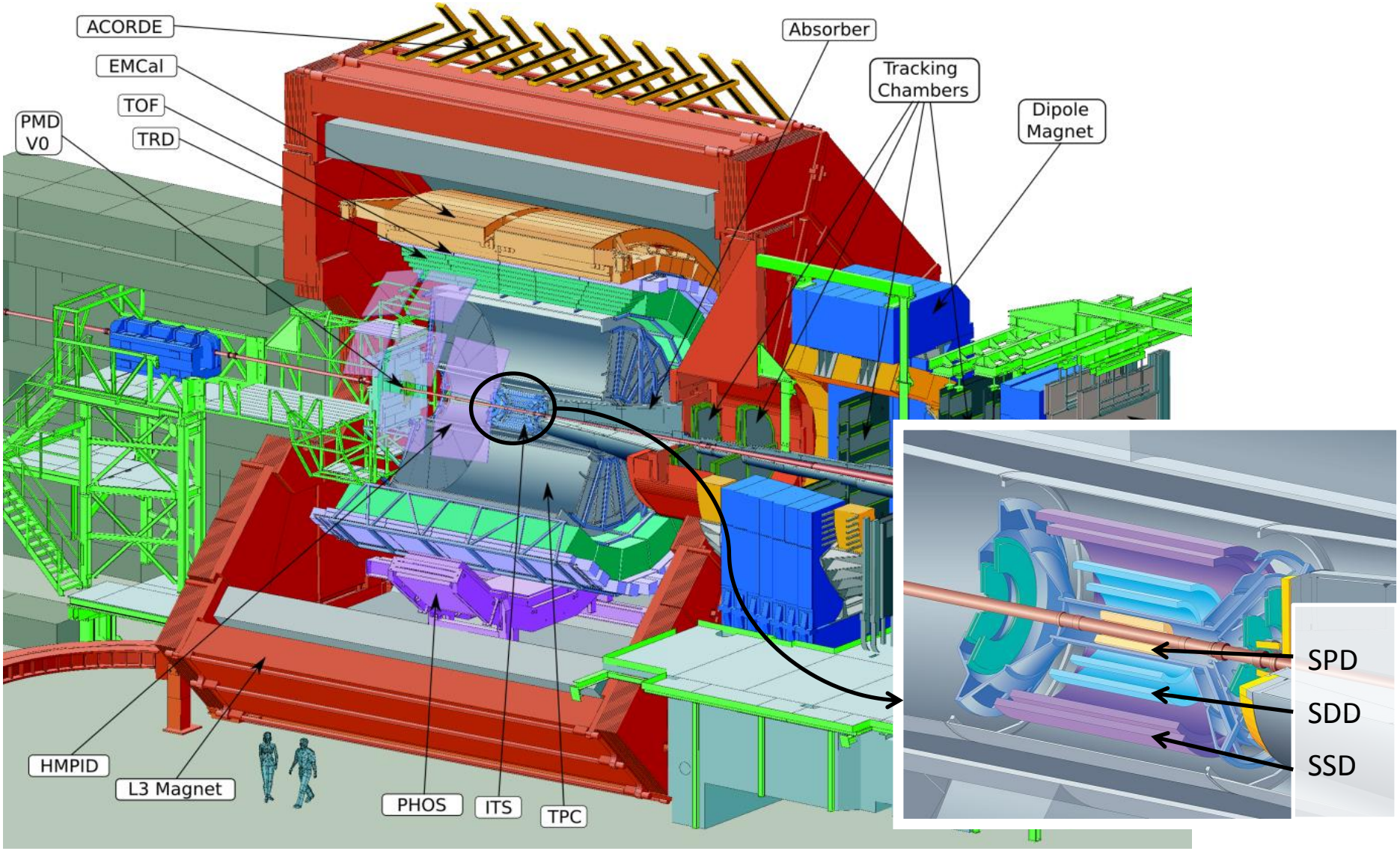
CERN - for the ALICE Collaboration

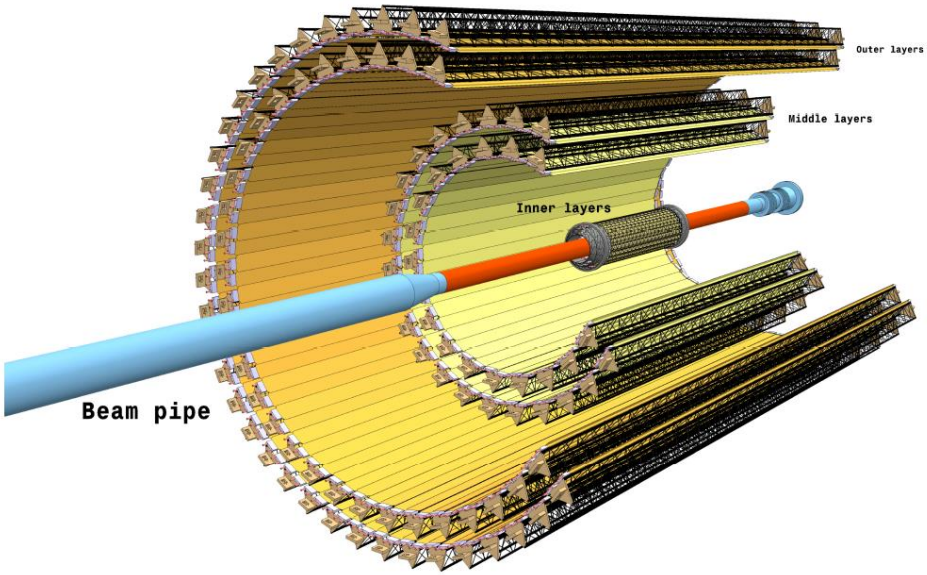
ALICE Inner Tracking System



ITS upgrade

Design objectives

- record Pb-Pb collisions at a rate of 50 kHz and pp collisions at a rate of 200 kHz
- improve impact parameter resolution by a factor 3
- improve standalone tracking efficiency and p_T resolution
- fast insertion/removal for yearly maintenance
- installation 2017-2018



New layout

- layers: 7 (3 inner, 4 middle+outer)
- beam pipe outer radius: 19.8 mm
- first layer radius: 22 mm
- $|\eta| < 1.22$ over 90% of luminous region

Specifications

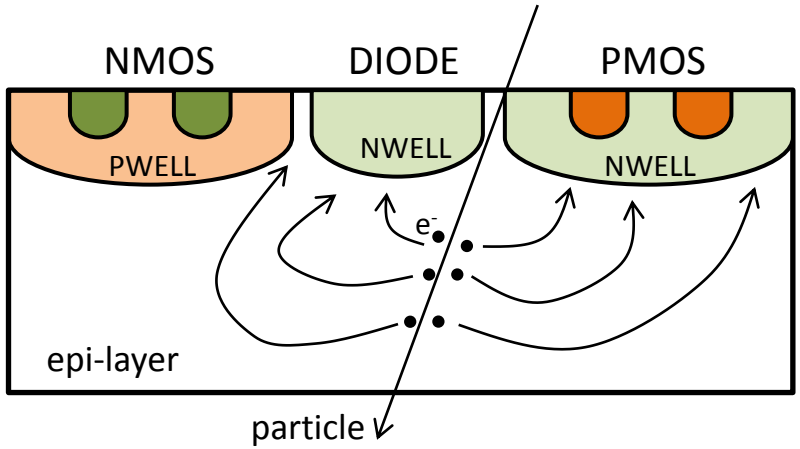
	Inner Barrel	Outer Barrel
Silicon thickness	50 µm	
Material thickness	0.3% X_0	0.8% X_0
Chip Size	15 mm x 30 mm	
Pixel Size	O(30 x 30) µm^2	O(30x30) ÷ O(50x50) µm^2
Integration Time	< 30 µs	
Power density	< 300 mW / cm^2	
Hit density (Pb-Pb)	~ 115 / cm^2	~ 1.5 / cm^2
Radiation Load (TID)	< 700 krad	< 10 krad
1 MeV n_{eq} fluency	1.1 x 10^{13} cm^{-2}	3 x 10^{10} cm^{-2}
Data throughputs	1.5 Gbit sec^{-1} chip^{-1}	16 Mbit sec^{-1} chip^{-1}

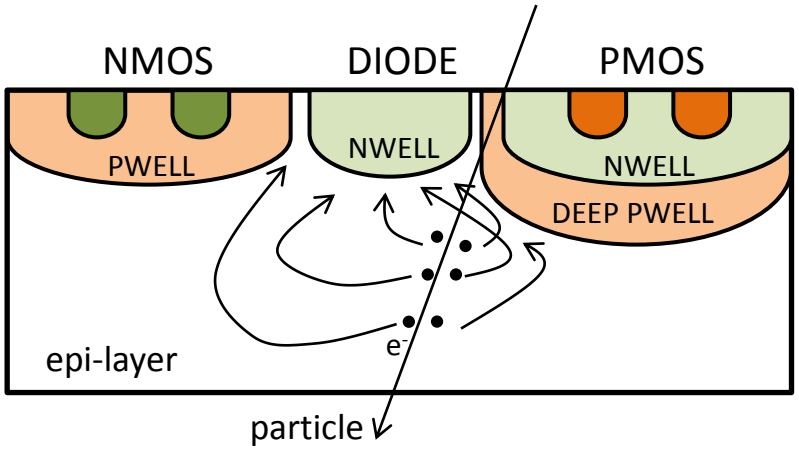
- Nr of bits to code a hit : 35
- Fake hit : 10^{-5} /event

Technology

TowerJazz 180 nm CMOS technology, monolithic detectors

- gate oxide thickness < 4 nm ⇨ robust to TID
- up to 6 metal layers ⇨ good for high density, low power digital circuits
  (small periphery , small dead material)
- standard epi layer 15-18 µm ⇨ large part of epi depleted @ 1-2 V reverse bias
  (S/N ratio increases, higher resistance to non-ionizing radiation)
- standard resistivity between 1 and 5 kΩ cm
- quadruple-well option ⇨ PMOS + NMOS can be used inside pixel
- possible stitching ⇨ up to a single die per 200 mm diameter wafer
  (less insensitive gaps, easier alignment of chips)

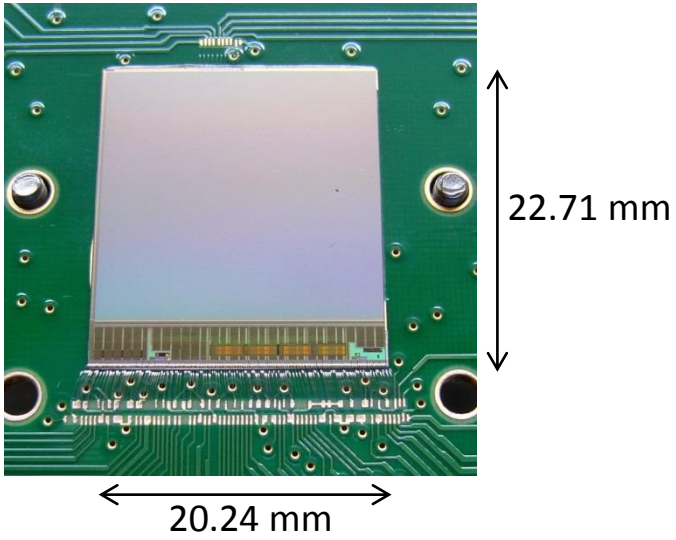




State of the art - STAR PXL

ULTIMATE chip

- developed by IPHC Strasbourg
- AMS 0.35 µm OPTO process
- rolling shutter + correlated double sampling (CDS) inside each pixel
- 20.7 x 20.7 µm^2 pixel size
- 15 µm thick epi layer, ≥ 400 Ω cm resistivity
- consumption 130 mW/cm^2



	STAR PXL	ALICE ITS (inner layers)
Readout time	190 µs	< 30 µs
TID radiation hardness	150 krad (35 °C)	700 krad (28 °C)
NIEL radiation hardness	few 10^{12} 1 MeV n_{eq} /cm^2 (35 °C)	1.1 x 10^{13} 1 MeV n_{eq} /cm^2

Further developments needed

Developments

MISTRAL

- by IPHC, Strasbourg
- rolling shutter with comparator at end of column
- amplification + CDS inside each pixel
- 2 columns read at once = 2x readout time
- integration time ~30 µs
- pixel size 22 x 22 µm^2 to 22 x 33 µm^2

CHERWELL-2

- by RAL (UK)
- rolling shutter with "strixel" structure
- comparator + processing electronics in the column pixel area
- memories also inside the strixel
- integration time ~30 µs
- pixel size 20 x 20 µm^2

ASTRAL

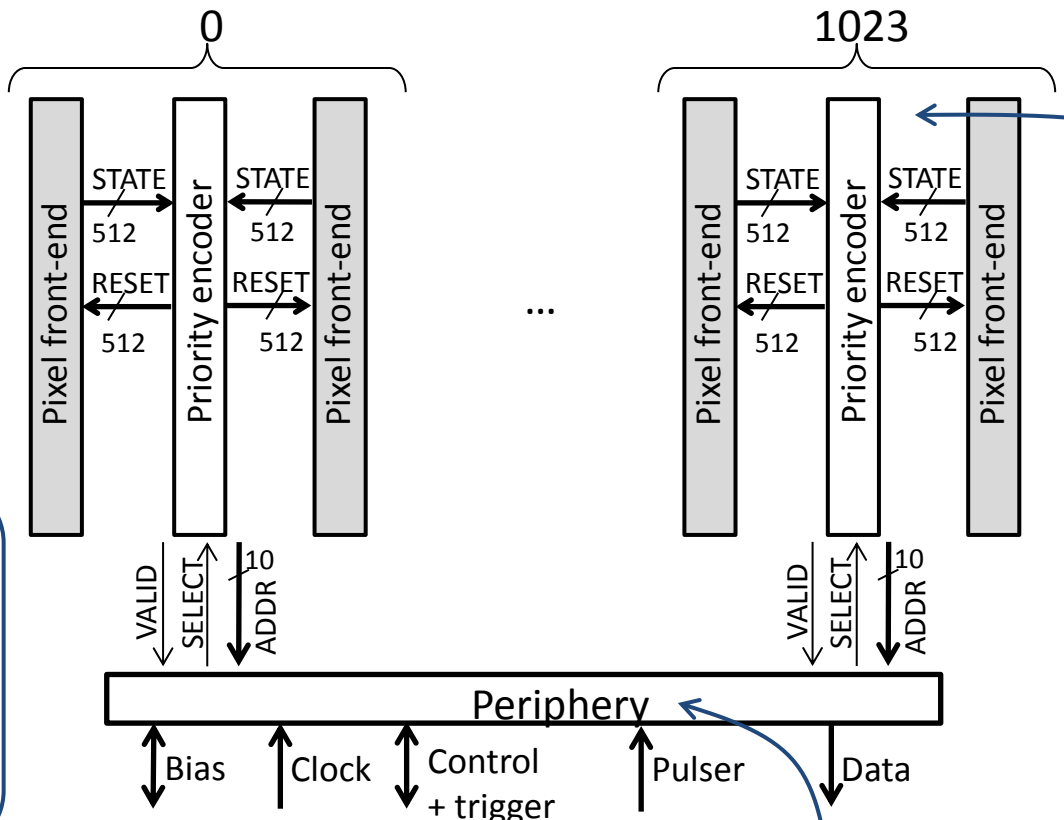
- by IPHC, Strasbourg
- rolling shutter with in-pixel comparator
- short analog lines, smaller power consumption
- reduction of peripheral circuitry
- integration time ~10 µs
- pixel size 22 x 22 µm^2 to 22 x 33 µm^2

ALPIDE

- by CERN, INFN (IT), CCNU (China)
- data-driven readout, address encoder used also for reset
- integration time 4 µs (shaping time of front-end)
- pixel size O(30 x 30 µm^2)

pALPIDE (prototype ALice PIxel DEtector)

Collaboration between CERN, INFN (Italy), CCNU (China)

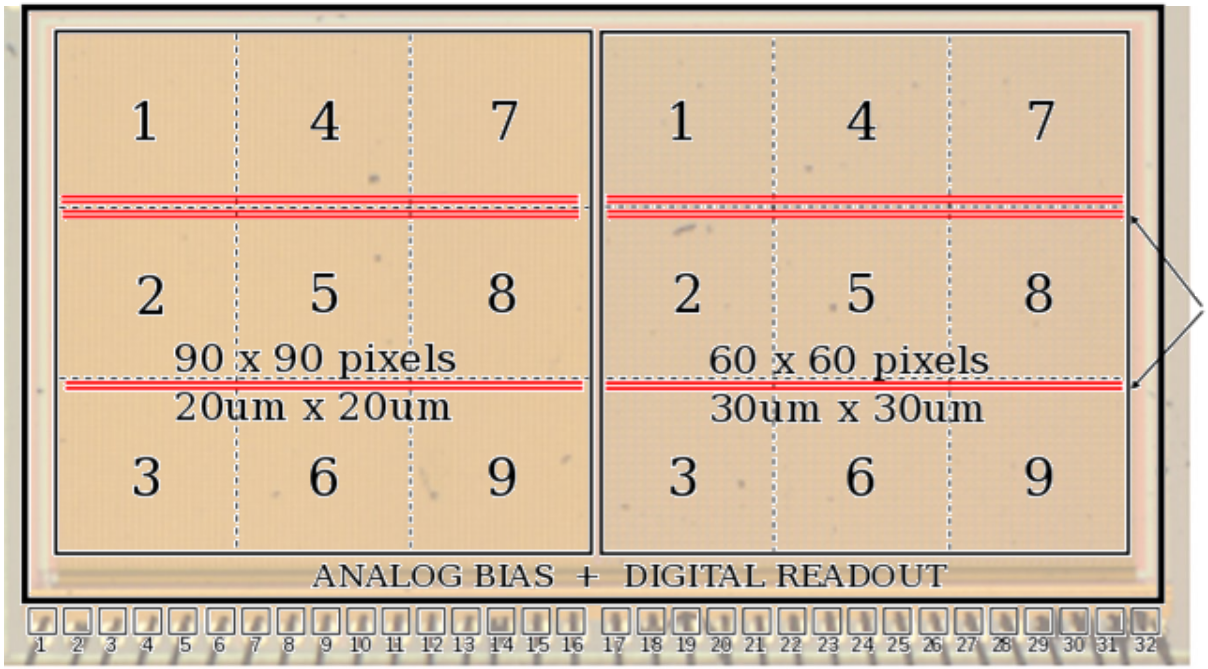


- low power in-pixel discriminator
- current comparator (bias of ~20 nA)
- storage element for hit information

- in-matrix address encoder
- tree structure to decrease capacitive load of lines
- outputs pixel address and resets pixel storage element

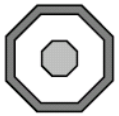
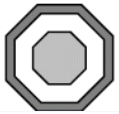
- loss-less data compression de-randomizing circuit
- compresses cluster information in the column
- multi-event memory

ALPIDE prototype: Explorer



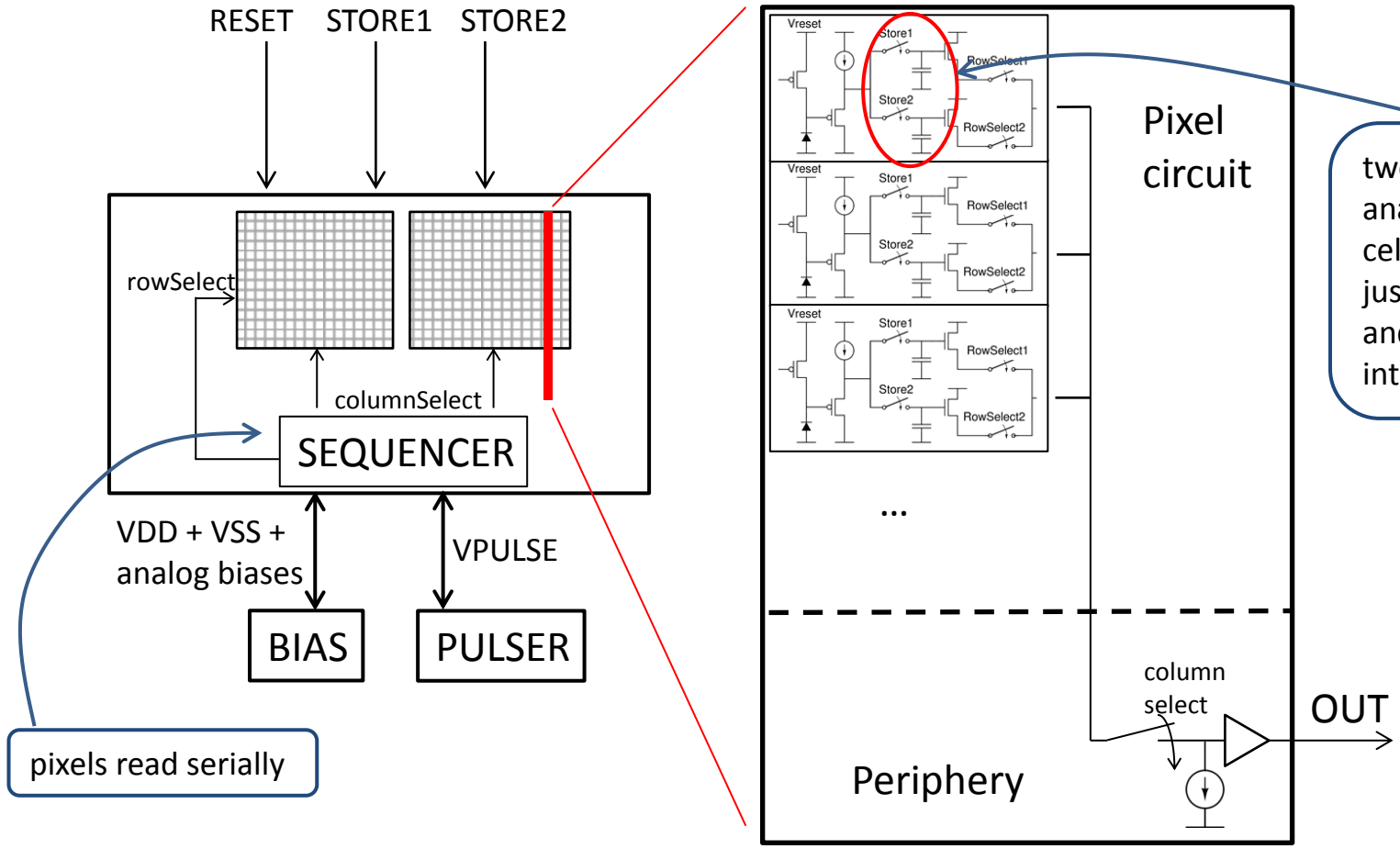
- study the electrode layout
  - pixel pitch
  - spacing between electrode and electronics
  - collection electrode shape / size, Q/C …
- study the effect of back bias on substrate
- Explorer-0, July 2012 (9 variants, 18 µm epi, high res.)
- Explorer-1, April 2013 (16 layout variants on different materials)

Explorer-0 variants

Sector	Type	Diameter [µm]	Spacing [µm]	
1		2	0	smallest diode, lower collection eff.
2		3	0	intermediate performance, S/N lower
3		4	0	larger diode, no spacing, more noise
4		3	0	performance similar to sector 2
5		3	0.6	small spacing, lower efficiency
6		3	1.04	better S/N increasing spacing
7		2	1.54	better collection eff., better S/N, TW
8		3	0	triple well
9		3	1.04	triple well

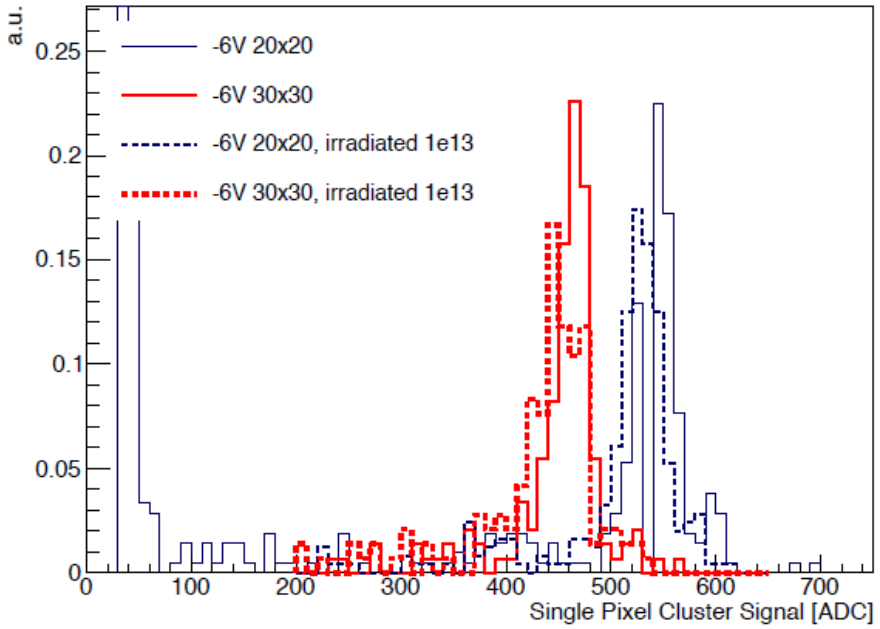
Explorer – block diagram

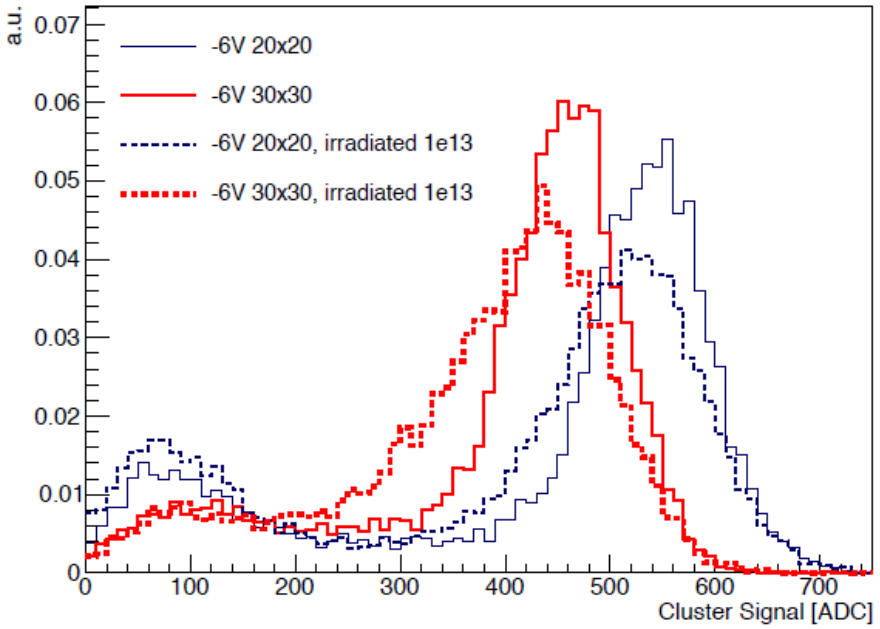
- analog read-out for characterization studies
- readout time decoupled from integration time
- double readout in CDS mode



Explorer-0 charge collection efficiency

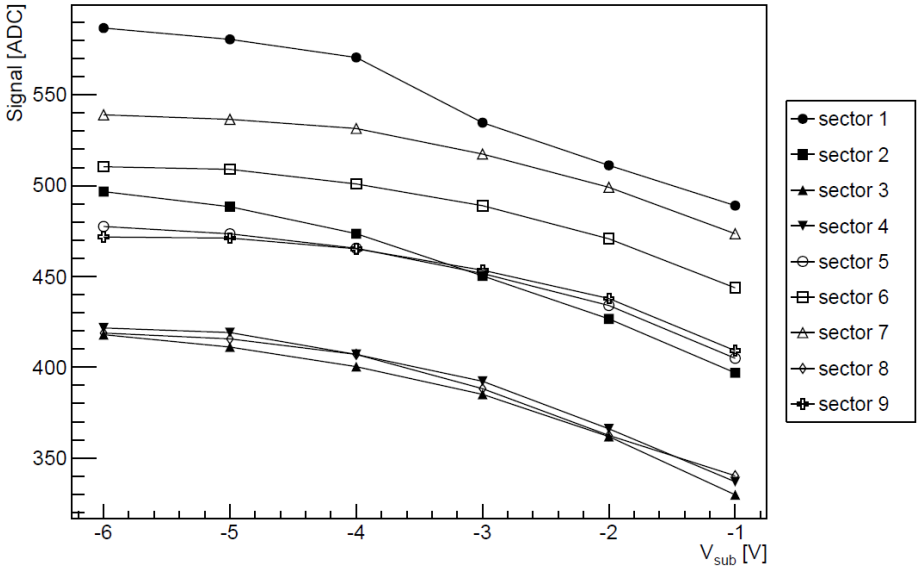
- ^{55}Fe X-ray source used
- response checked for seed (highest signal in 5x5 matrix) and for cluster (5x5 pixels around seed)
- ^{55}Fe calibration peak → charge calibration (1640 electrons in single pixel)
- example of seed (left) and cluster (right) signals below

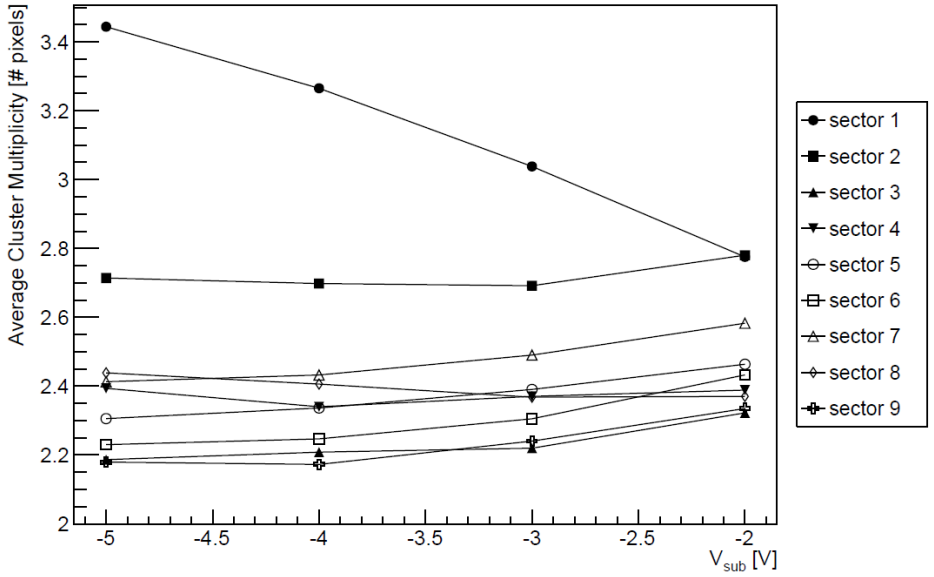




Back bias effect

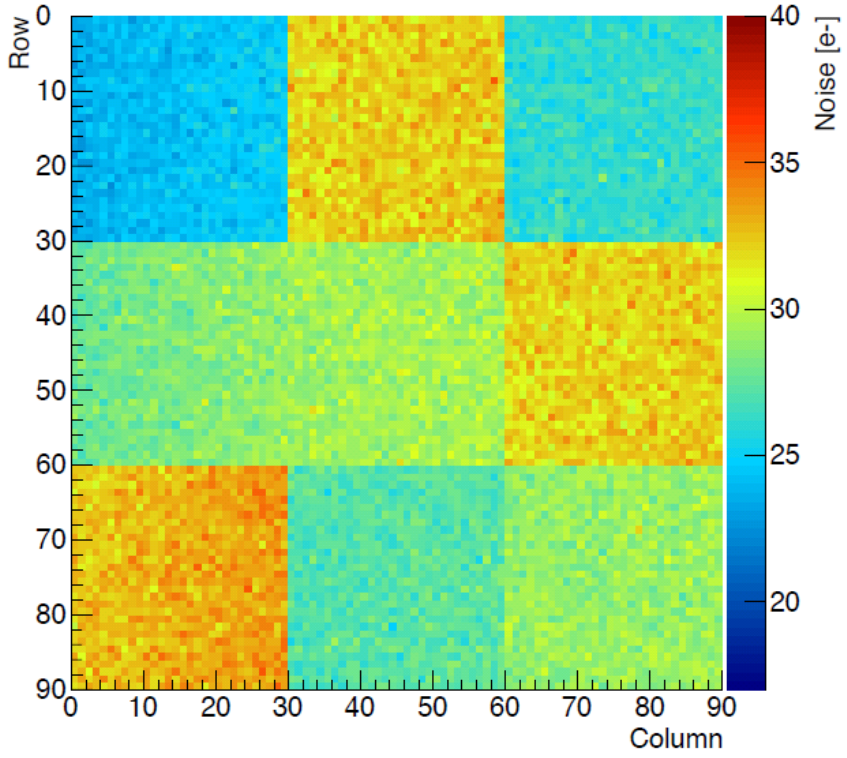
- seed pixel signal (left) and cluster multiplicity (right) as function of the back bias voltage, for 20 x 20 μm^2 pixels
- increase of back bias voltage → increase of depletion volume → drop of the input pixel capacitance → increase of single pixel signal
- increase of depletion volume → reduction of cluster multiplicity (with less active pixels the chip readout time decreases)

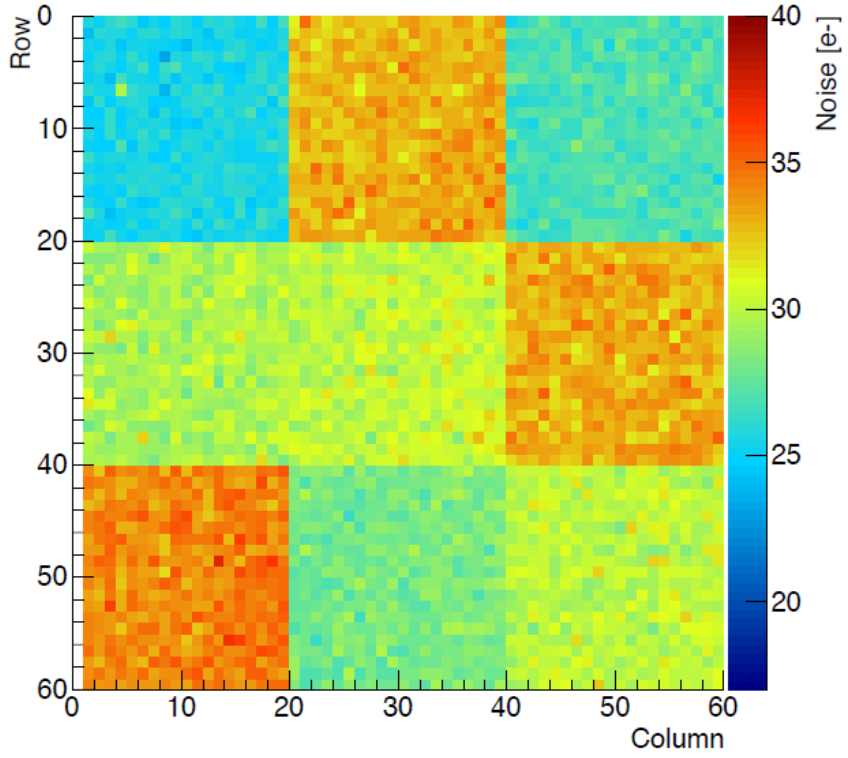




Explorer-0 noise

- uniformity studied in space: sector-to-sector variation observed due to different structures implemented
- below plots for 20 x 20 μm^2 pixels (left) and 30 x 30 μm^2 pixels (right)
- uniformity studied in time with 100 consecutive pedestal measurements (one measurements corresponds to about 30 seconds)



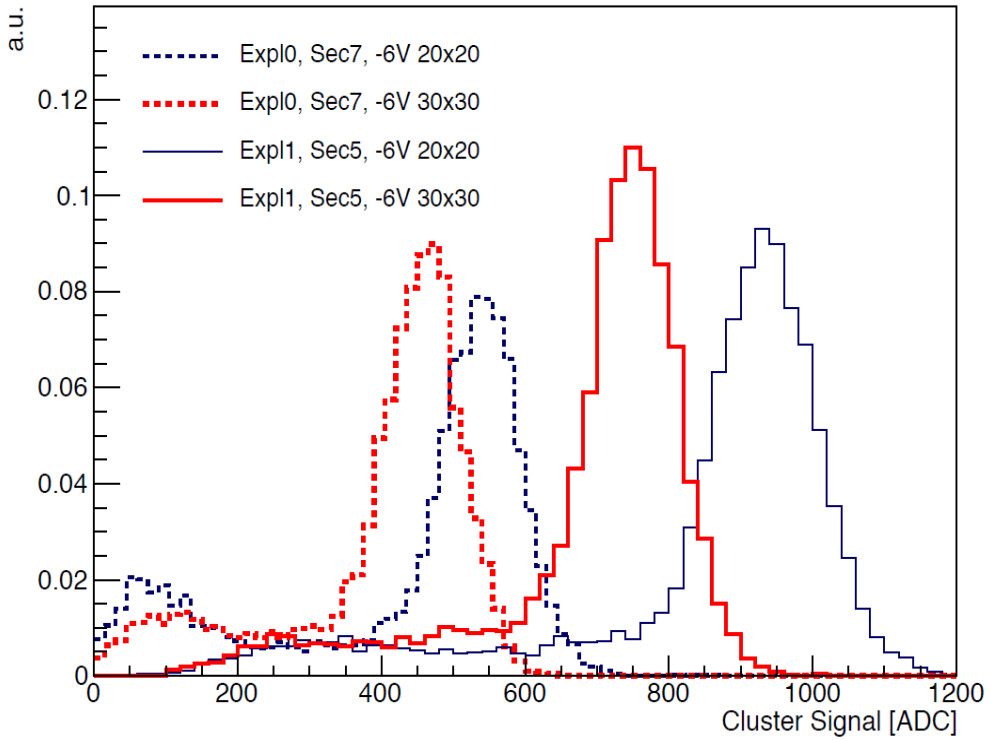


Explorer-1

From Explorer-0 to Explorer-1 diode layout and input capacitance optimized (from 5 fF to 2 fF)

16 different Explorer-1 structures submitted, used to scan the parameter space

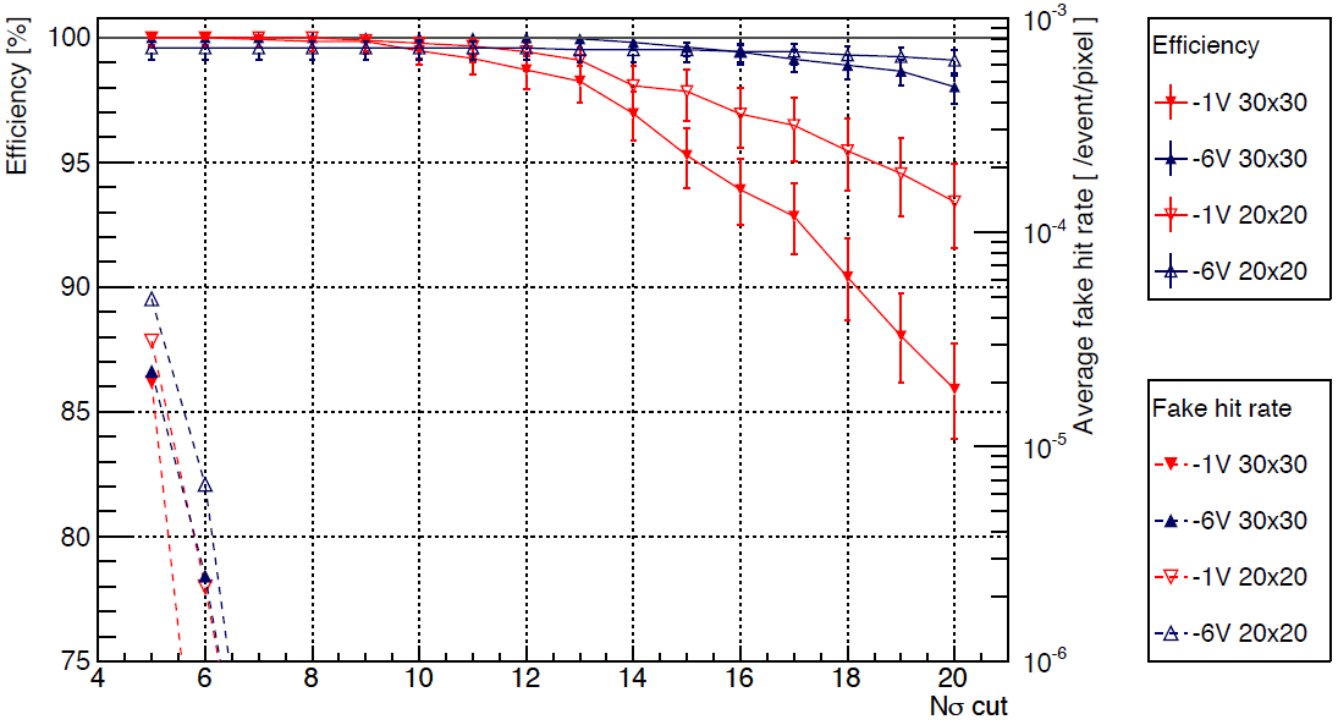
- Comparison of ^{55}Fe cluster signal for Explorer-0 and Explorer-1
- Explorer-1 shows signal increase, and similar noise level



Explorer-1 detection efficiency

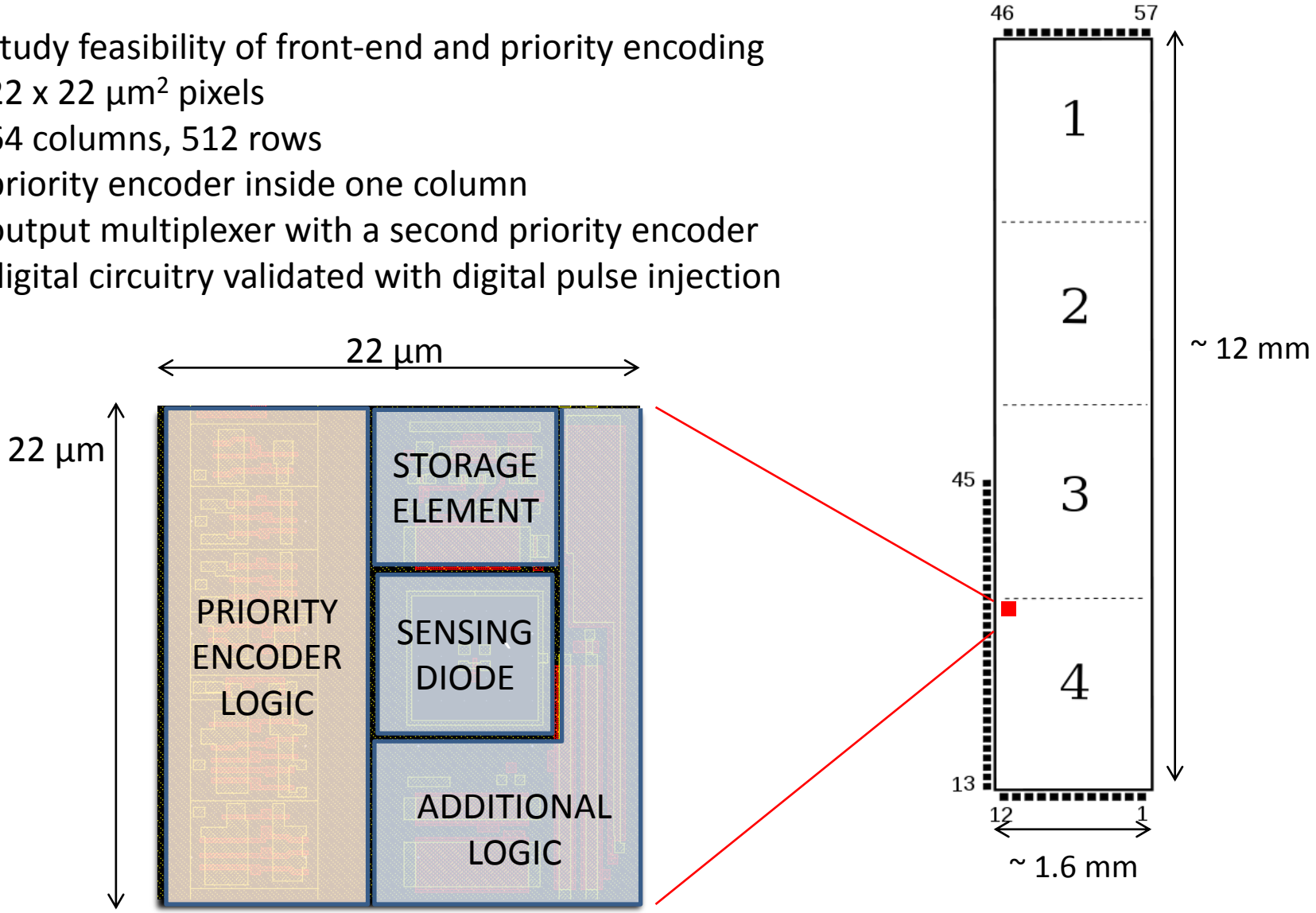
- after irradiation drop of 10 - 20% in CCE, recovered with back bias
- better performance of larger diodes with larger spacing to electronics
- wider distance → wider depletion volume → lower input capacitance
- better performance of 20 x 20 μm^2 at low back bias voltage
- detection efficiency above 99% up to 10σ cut, also after irradiation

Explorer-1 results after tests with 4 GeV/c electrons at DESY, averaged on all diode geometries



pALPIDE (prototype ALice PIxel DEtector)

- study feasibility of front-end and priority encoding
- 22 x 22 µm^2 pixels
- 64 columns, 512 rows
- priority encoder inside one column
- output multiplexer with a second priority encoder
- digital circuitry validated with digital pulse injection

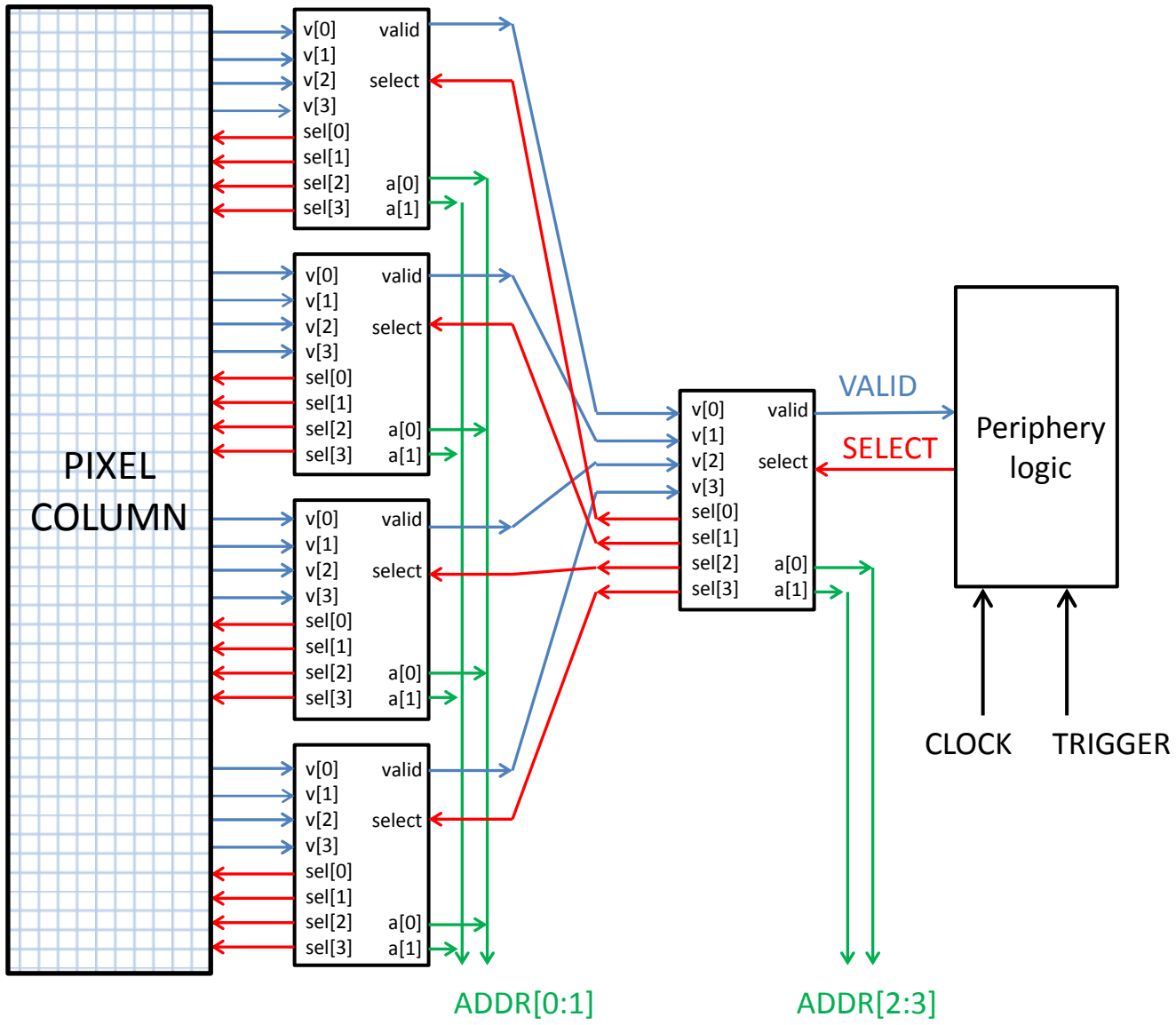


Priority encoder

- hierarchical readout
- 4 inputs basic block repeated to create a larger encoder
- 1 pixel read per clock cycle

- forward path (address encoder) in blue
- feed-back path (pixel reset) in red

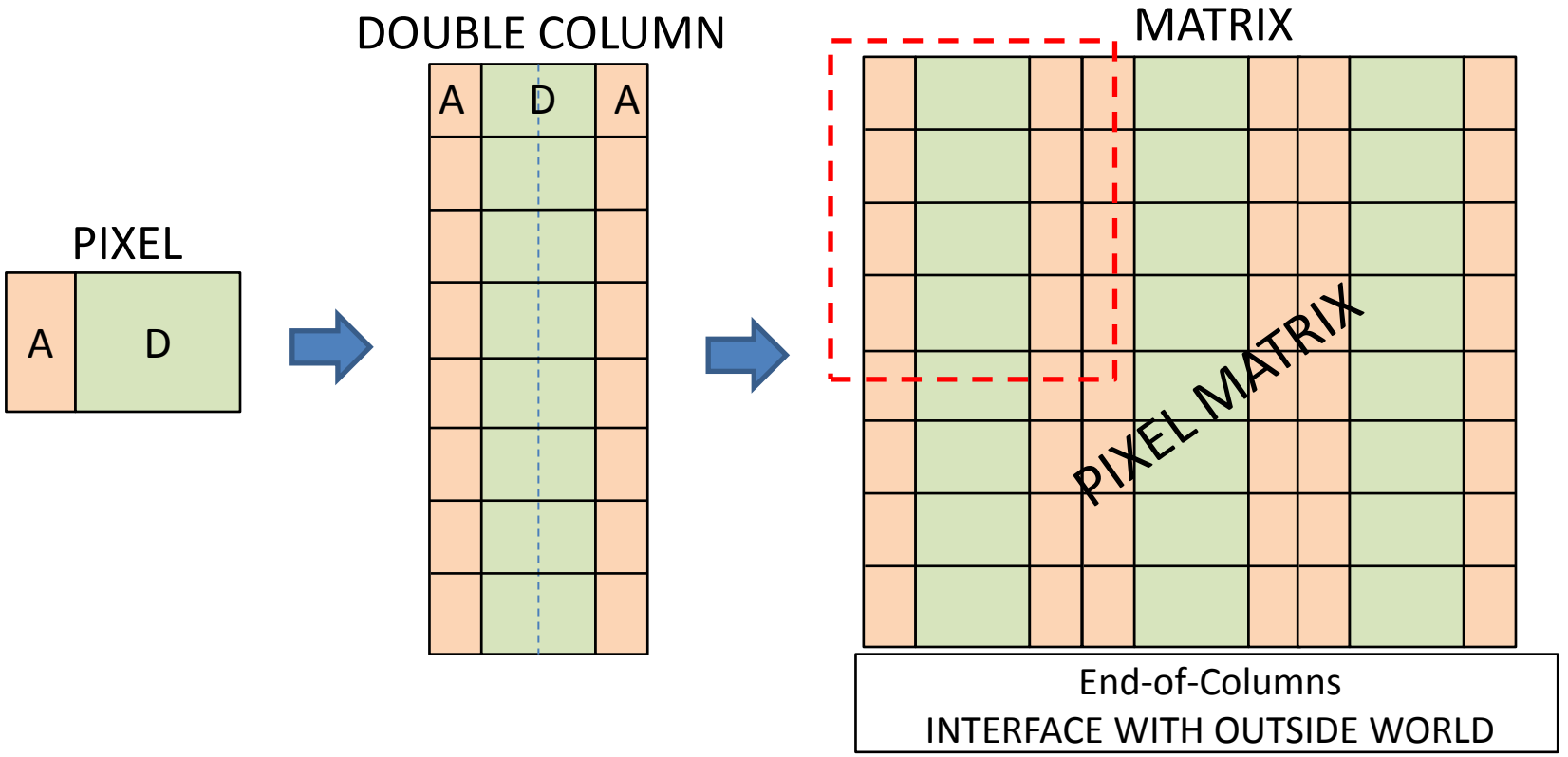
- asynchronous (combinatorial) logic
- clock only to periphery, synchronous select only to hit pixels



Conclusions

- ALICE ITS upgrade, entirely based on a new monolithic pixel detector, to record Pb-Pb collisions up to 50 kHz with improved vertexing capabilities
  - < 30 μs integration time
  - 0.3% X_0 material budget for innermost layers
  - < 300 mW / cm^2 power consumption
- Explorer prototype chips fabricated in TowerJazz 180 nm CMOS technology
  - very good charge collection efficiency, noise, S/N measured with radioactive source and test beams
  - Explorer-1 fabricated in 16 variants on different materials, to scan parameter space
- pALPIDE prototype fabricated, characterization started
  - in-pixel discriminator and storage element
  - sparsified readout with priority encoder scheme

Sparsified readout



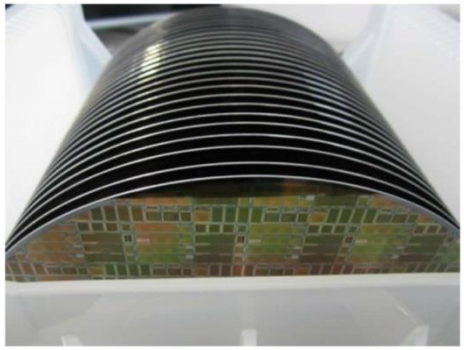
- Matrix of pixels arranged in columns: 2 adjacent, mirrored, columns share the same digital area
- GOAL: after a trigger, read only the active pixels, and reset them
- Possible readout architecture with priority encoder -> basic cell of 4 pixels, repeated to read larger structures

April 2013 engineering run

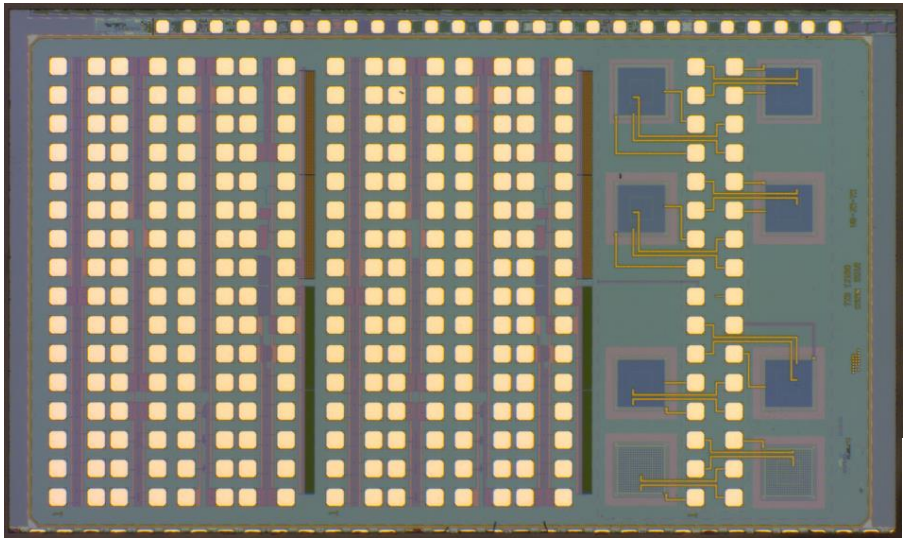
Explorer-1, pALPIDE, MISTRAL + ASTRAL families, CHERWELL

Type	# wafers	epi thickness [µm]	resistivity [Ω cm]	Δρ [Ω cm]
1	3	12	30	-
2	4	18	> 1k	-
3	3	30	> 1k	-
4	3	40	> 1k	-
5	6	20	6.2 k	1.2 k
6	3	40	7.5 k	2.3 k
7	3	CZ	> 700	-

- 18 µm epi thickness -> ~1300-1400 electrons

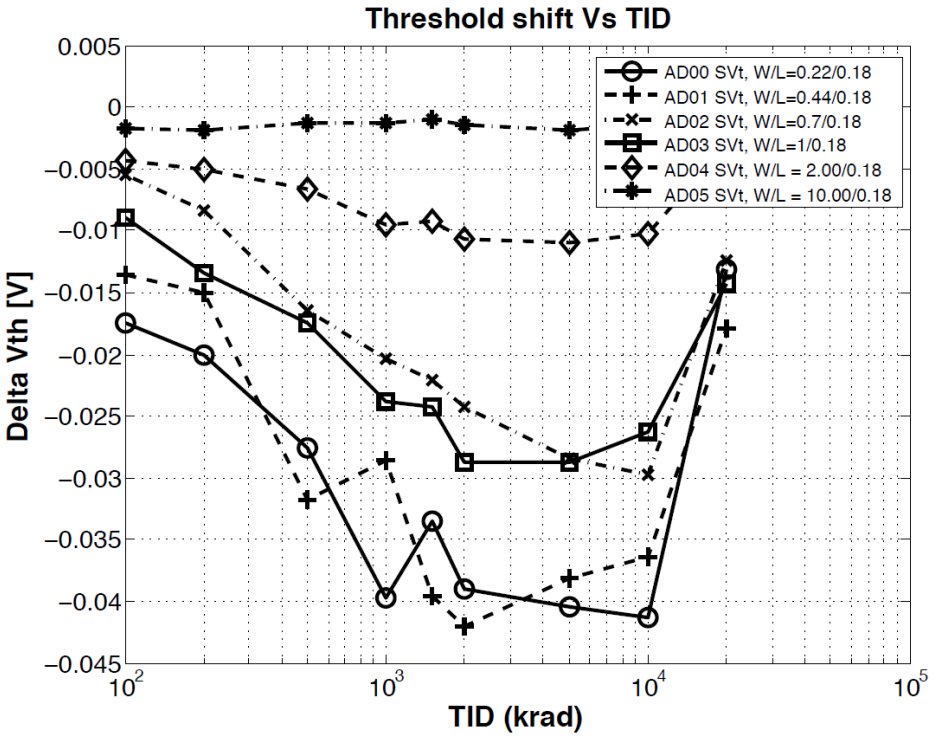


Radiation hardness 1/2

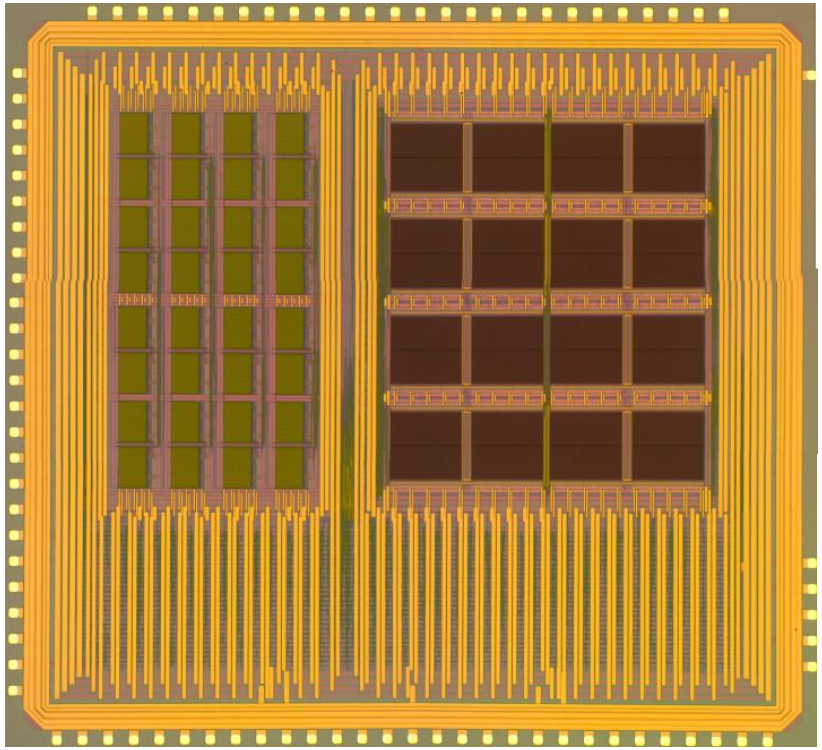


- basic structures, diodes + transistors
- studied threshold voltage, transconductance and dark current wrt radiation and dose

- measurements with 10 keV X-ray machine at CERN
- irradiation up to 10 Mrad (25 krad / minute)
- plot for threshold voltage shifts, 2 x 10^4 krad -> annealing of 24h

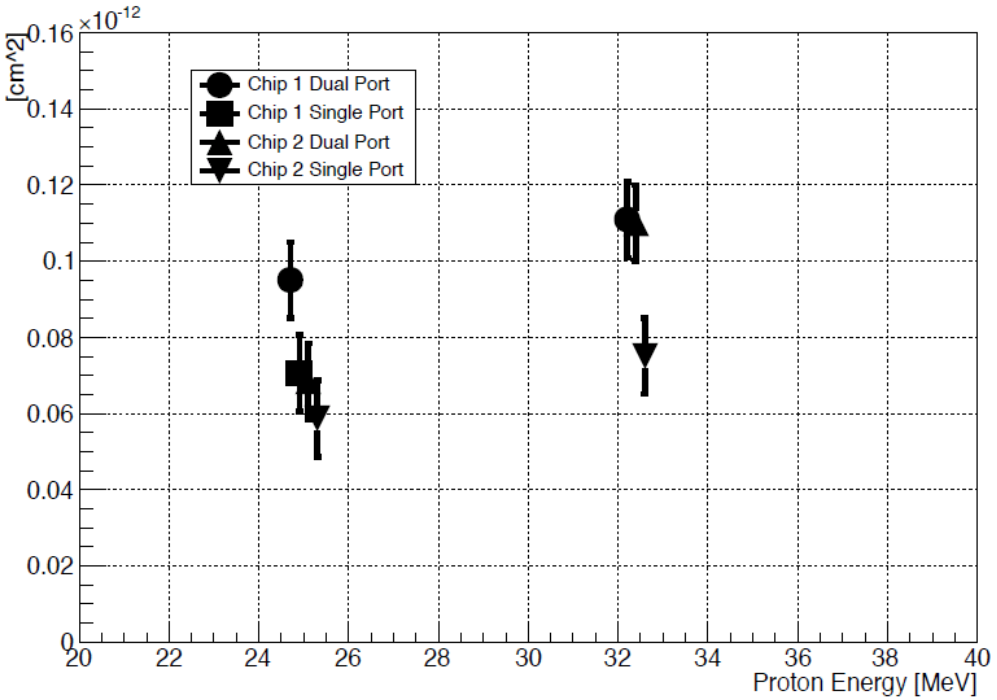


Radiation hardness 2/2



- single port RAMs, dual port RAMs, shift register
- studied SEU cross sections
- proton beam from NPI Rez cyclotron (near Prague)

- 32.2 MeV, 24.8 MeV
- 1.1 x 10^7 to 1.4 x 10^7 protons / cm^2
- static mode (written once and flips counted over time)
- results show average of different patters



Explorer-0 signal over noise

- studied with 4 GeV/c positrons at DESY (30% more signal than MIPs)
- depends on pixel noise, conversion gain, cluster area
- example of seed pixel S/N for sector 7 below