

Design and characterization of Explorer0 monolithic pixel sensor in 180 nm CMOS process

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Within the R&D activities for the upgrade of the ALICE Inner Tracking System (ITS), Monolithic Active Pixel Sensors (MAPS) are being developed and studied, due to their lower mass ($\sim 0.3\% X/X_0$ for the inner layers) and higher granularity ($\sim 20 \mu\text{m} \times 20 \mu\text{m}$ pixels) with respect to the present pixel detector.

This paper presents the design and characterization results of the Explorer0 chip, manufactured in the Tower-Jazz 180 nm CMOS Imaging Sensor process, based on a wafer with high-resistivity ($\rho > 1 \text{ k}\Omega \text{ cm}$) and 18 μm thick epitaxial layer.

The chip is organized in two sub-matrices with different pixel pitches (20 μm and 30 μm), each of them containing several pixel designs. The collection electrode size and shape, as well as the distance between the electrode and the surrounding electronics, are varied; the chip also has the possibility of decoupling the charge integration time from the readout time, and of changing the sensor bias.

The charge collection properties of the different pixel variants implemented in Explorer0 have been studied using a 55Fe X-ray source and Minimum Ionizing Particles (5 GeV/c π^-). The sensor capacitance has been estimated, and the effect of the sensor bias has also been examined in detail, including a reverse bias option.

Following these results, a second version of the Explorer0 chip has been submitted for production in March 2013, together with a novel circuit with in-pixel discrimination and a sparsified readout.

Primary author: CAVICCHIOLI, Costanza (CERN)

Co-authors: JUNIQUE, Antoine (CERN); MARIN TOBON, Cesar Augusto (Valencia Polytechnic University (ES)); PANTANO, Devis (Padova); REIDT, Felix (Ruprecht-Karls-Universitaet Heidelberg (DE)); HILLEMANN, Hartmut (CERN); MUGNIER, Herve (Unknown); VAN HOORNE, Jacobus Willem (Vienna University of Technology (AT)); ROUSSET, Jerome; MUSA, Luciano (CERN); MAGER, Magnus (CERN); MARTINENGO, Paolo (CERN); RIEDLER, Petra (CERN); GIUBILATO, Piero (Universita e INFN (IT)); CHALMET, Pierre Laurent (Unknown); YANG, Ping (Central China Normal University CCNU (CN)); MATTIAZZO, Serena (Universita e INFN (IT)); KUGATHASAN, Thanushan (CERN); SNOEYS, Walter (CERN)

Presenter: CAVICCHIOLI, Costanza (CERN)

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