Contribution ID: **73** Type: **ORAL**

The Silicon Vertex Locator for the LHCb Upgrade

Thursday 5 September 2013 11:20 (20 minutes)

The upgrade of the LHCb experiment, planned for 2018, will transform the entire readout to a triggerless system operating at 40 MHz. All data reduction algorithms will be executed in a high level software farm, with access to all event information. This will enable the detector to run at luminosities of 1-2 x10ˆ33 /cmˆ2 /s and explore New Physics effects in the beauty and charm sector with unprecedented precision.

The upgraded silicon vertex detector (VELO) must be light weight, radiation hard, and compatible with LHC vacuum requirements. It must be capable of fast pattern recognition and track reconstruction and will be required to drive data to the outside world at speeds of up to 3 TB/s.

This challenge is being met with a new VELO design based on hybrid pixel detectors positioned to within 5 mm of the LHC colliding beams. The sensors have 55 x 55 square pixels and the VELOPix ASIC which is being developed for the readout is based on the Timepix/Medipix family of chips. The ASIC will operate in data driven mode, time stamp the hits and will operate with a fast front end in order to eliminate timewalk at 40 MHz trigger rate. The hottest ASIC will have to cope with pixel hit rates of up to 900 MHz. Work is in progress to optimise the sensor guard ring design to cope with the irradiation levels, which are highly non uniform and reach 8 x 10ˆ15 at the innermost regions.

The material budget will be optimised with the use of evaporative CO2 coolant circulating in microchannels within a thin silicon substrate. Microchannel cooling brings many advantages: very efficient heat transfer with almost no temperature gradients across the module, no CTE mismatch with silicon components, and low material contribution. This is a breakthrough technology being developed for LHCb, and work is in progress to demonstrate the robustness of the substrate and connector against the high pressures which may be developed in a CO2 cooled system.

LHCb is also focussing effort on the construction of a lightweight foil to separate the primary and secondary LHC vacuua, the development of high speed cables, and the metallisation and radiation qualification of the module.

The 40 MHz readout will also bring significant conceptual changes to the way in which the upgrade trigger is operated. Work is in progress to incorporate momentum and impact parameter information into the trigger at the earliest possible stage, using the fast pattern recognition capabilities of the upgraded detector.

The current status of the VELO Upgrade will be described together with a presentation of recent test results, and a discussion of the R&D on alternative solutions which has been carried out within the LHCb VELO upgrade programme.

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Session Classification: Session 6

Track Classification: Applications in High Energy Physics