Status and perspectives of pixel sensors based on 3D vertical integration

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Ninth International **“Hiroshima” Symposium** on the **Development** and **Application** of **Semiconductor Tracking Detectors**

Outline

- What is 3D integration? Why did it trigger a wide interest in our community?
- Evolution from 2D devices to 3D integration for advanced pixel sensors and readout electronics in high energy physics experiments
- Expectations, experience, plans: current status and future promise (a personal view)

Advancing the state of the art of pixel sensors for a next generation of HEP experiments

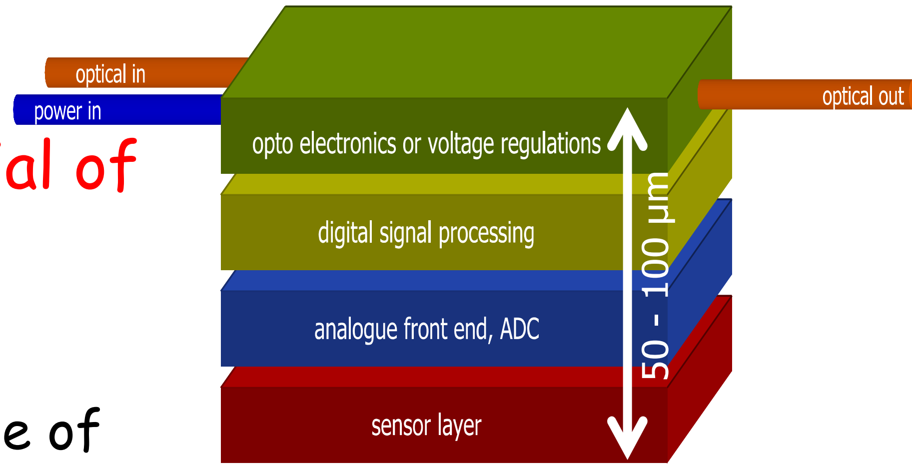
New demanding specifications for experiments at new machines (HL-LHC, International Linear Collider,…):

- **Improve resolution ⇒ shrink pixel size and pitch**, down to 20 μm or even less
- **Preserve or even increase pixel-level electronic functions**

  handling of high data rates (hit rates > 10 MHz/mm^2), analog-to digital conversion, sparsification, intelligent data processing…: presently this also contributes to limiting the minimum size of pixel readout cells
- **Decrease amount of material ⇒ thin sensor and electronics** chips, "zero mass" cooling
  - Necessary to reduce errors in track reconstruction due to multiple scatterings of particles in the detector system
  - 50 -100 μm total thickness

What is 3D integration?

- 3D electronics: "the vertical integration of thinned and bonded silicon integrated circuits with vertical interconnects between the IC layers."[1]

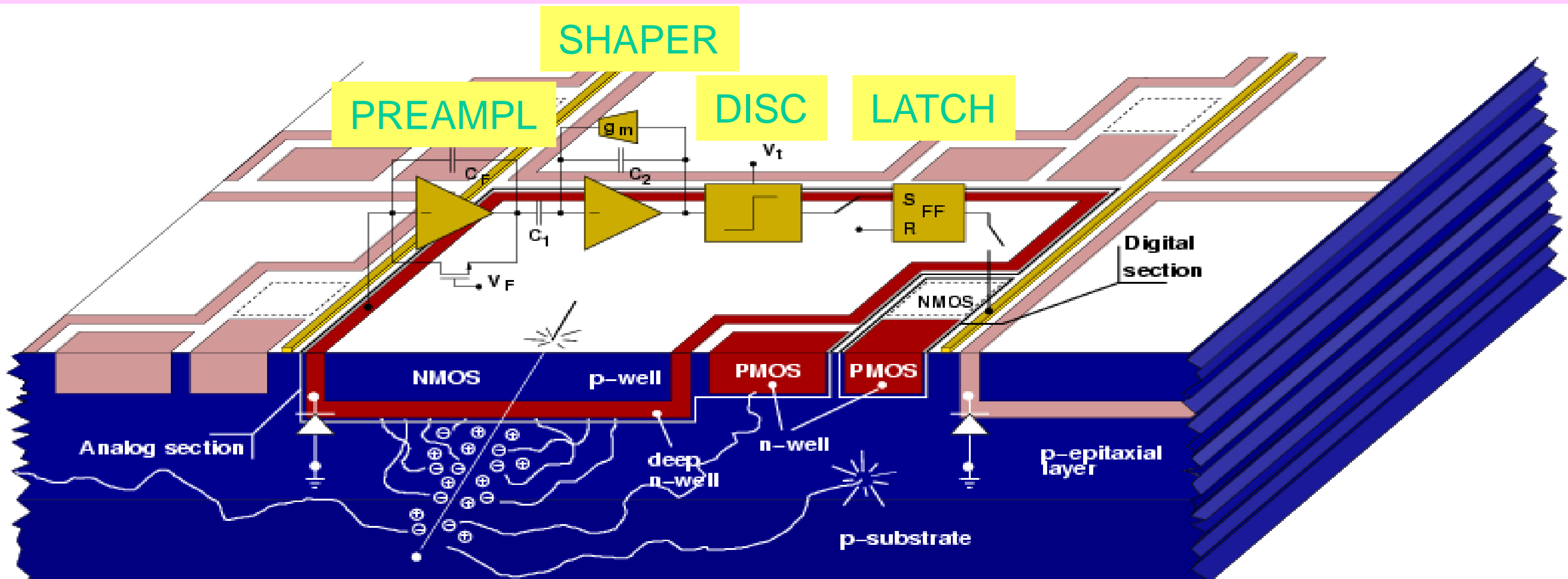


- 3D electronics has the potential of being:
  - Denser (smaller form factor)
  - Faster (reduced delay because of shorter interconnects)
  - Lower power (smaller interconnect capacitance)
  - Lower cost (sizably less expensive than aggressive CMOS scaling)
  - Integration of dissimilar technologies (sensor, analog, digital, optical)

1) Philip Garrou, Christopher Bower, Peter Ramm, Handbook of 3D Integration Technology and Applications of 3D Integrated Circuits, Wiley-VCH, 2008.

A case study:
Deep N-Well (DNW) CMOS pixel sensors

New approach in CMOS MAPS design with the goal of achieving **"hybrid pixel-like" functionalities in monolithic devices** (pixel-level sparsification and time stamping).



Classical optimum signal processing chain for capacitive detectors at pixel level:

- Charge-to-Voltage conversion done by the charge-sensitive preamplifier
- The collecting electrode (Deep N-Well) can be extended to obtain higher single pixel collected charge (the gain does NOT depend on the sensor capacitance), reducing charge loss to competitive N-wells where PMOSFETs are located

The first generation of CMOS sensors with in-pixel sparsification and time stamping
(DNW MAPS in the 130 nm STM CMOS process)

Available prototypes of DNW sensors with two different architectures:

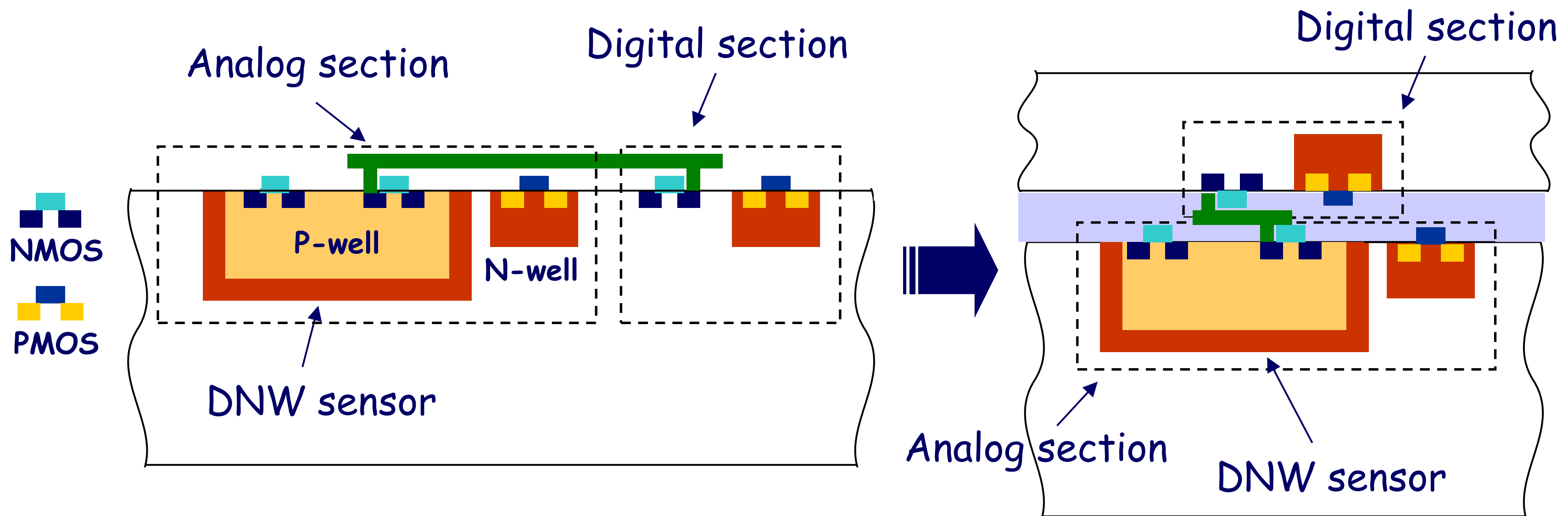
- APSEL: continuously operating sparsified readout, 50x50 μm^2 pitch
- SDR0: intertrain readout (ILC-like), 25x25 μm^2 pitch

✓ **These 2D devices proved the deep N-well concepts, with some limitations:**

- With a binary readout scheme, ILC VTX demands a **pixel pitch** < 20 μm to achieve required single point resolution < 5 μm
- **Detection efficiency** does not meet requirements (> 99 %) because of competitive n-wells (PMOS) decreasing the fill factor
- Capability of **handling multiple pixel hits** for an ILC sensor has to be included without degrading efficiency and pitch
- **Digital-to-analog interferences** are critical for continuous operation in APSEL devices
- Discriminator **threshold mismatch** is difficult to control without a local adjustment

The approach to 3D within the deep N-well sensor concept

- Guideline: move the digital section to a second layer, at the same time reducing the area of competitive PMOS N-wells in the sensing layer and the size of the pixel

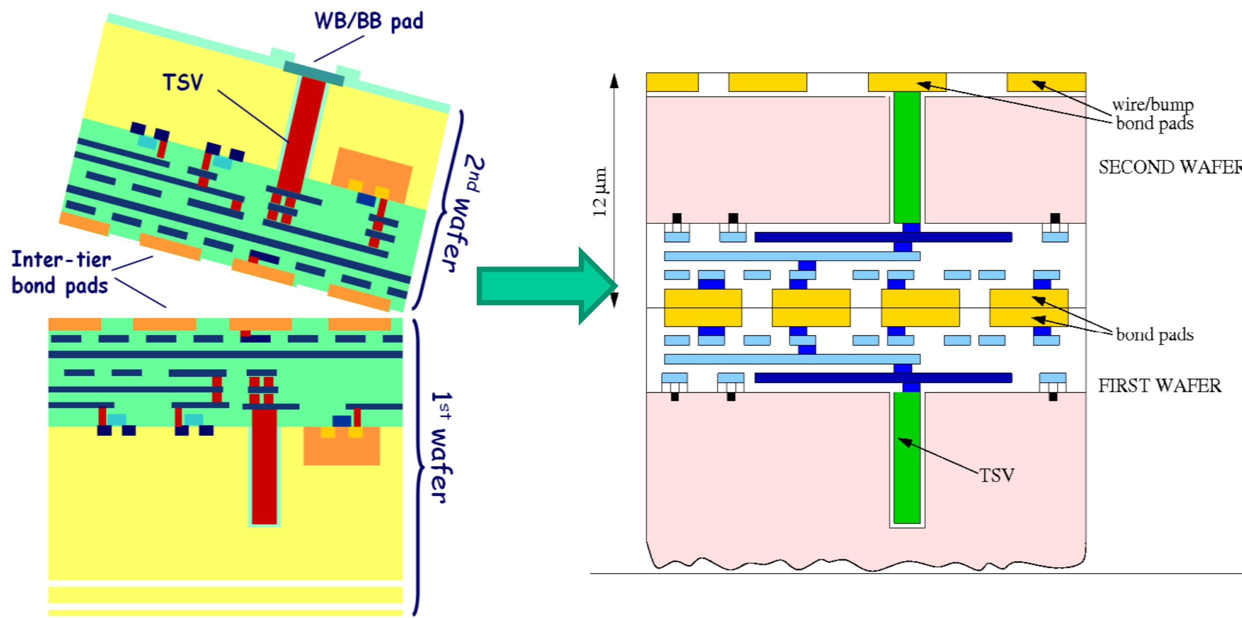


- Tier 1: collecting electrode (deep N-well/P-substrate junction), analog front-end and first discriminator stage
- Tier 2: digital front-end (latches for hit storage, pixel-level digital blocks for sparsification, time stamp registers, kill mask,…) and digital back-end (X and Y registers, time stamp line drivers, serializer,…)

A "via first" process as an aggressive variant of 3D integration

Tezzaron 3D process (Fermilab 3D-IC Consortium)

- Through-Silicon Vias (TSV) are etched at early stages of a 130nm CMOS process (after transistor fabrication) at the silicon foundry. High density vertical interconnections are possible. High-density, low-mass bonding of CMOS layer is achieved by a Cu-Cu thermocompression process.
- Potentially, this might open the way to 3D integrated circuits for pixel readout with a large number of pixel-level interconnections, enabling advanced signal processing architectures, large memory size, digital calibration of analog circuits,…

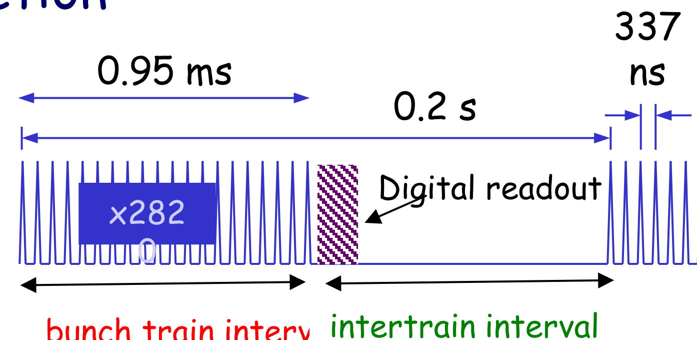


Tezzaron vias are very small: Φ_{via}=1.2 µm, $\Phi_{landing_pad}$=1.7 µm, d_{min}=2.5 µm

Wafer bonding pads are nominally on a 4 µm pitch

Advantages of going 3D for an ILC-like DNW sensor

- Pixel-level functionalities: a double-hit detection capability (two flip-flops) is included
- Pixel pitch: reduced from 25 μm to 20 μm
- Pixel "fill factor": increased by a sizable reduction of the area of PMOS N-wells in the sensor layer



shaperless FE (SFE)

discriminator

Inter-tier bond pads

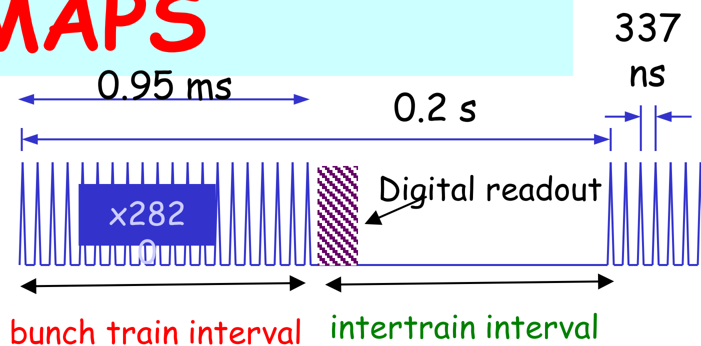
Token passing core

TIER 1 (BOTTOM)

TIER 2 (TOP)

Intertrain Readout Architecture for an "ILC-like" MAPS

Suggested by FNAL IC design group, first implemented in the VIP chip



Readout CK
MUX
X
Y
T
Serial data output
Cell CK
X=1
X=2
Time Stamp Buffer 1
Time Stamp Buffer 2
Time Stamp Buffer 16
First token in
Last token out
Y=1
Y=2
Cell (1,1) gXb TS Tkin Tkout gYb
Cell (1,2) gXb TS Tkin Tkout gYb
Cell (1,16) gXb TS Tkin Tkout gYb
Cell (2,1) gXb TS Tkout Tkin gYb
Cell (2,2) gXb TS Tkout Tkin gYb
Cell (2,16) gXb TS Tkout Tkin gYb
Cell (16,1) gXb TS Tkout Tkin gYb
Cell (16,2) gXb TS Tkout Tkin gYb
Cell (16,16) gXb TS Tkout Tkin gYb

gXb=get_X_bus

gYb=get_Y_bus

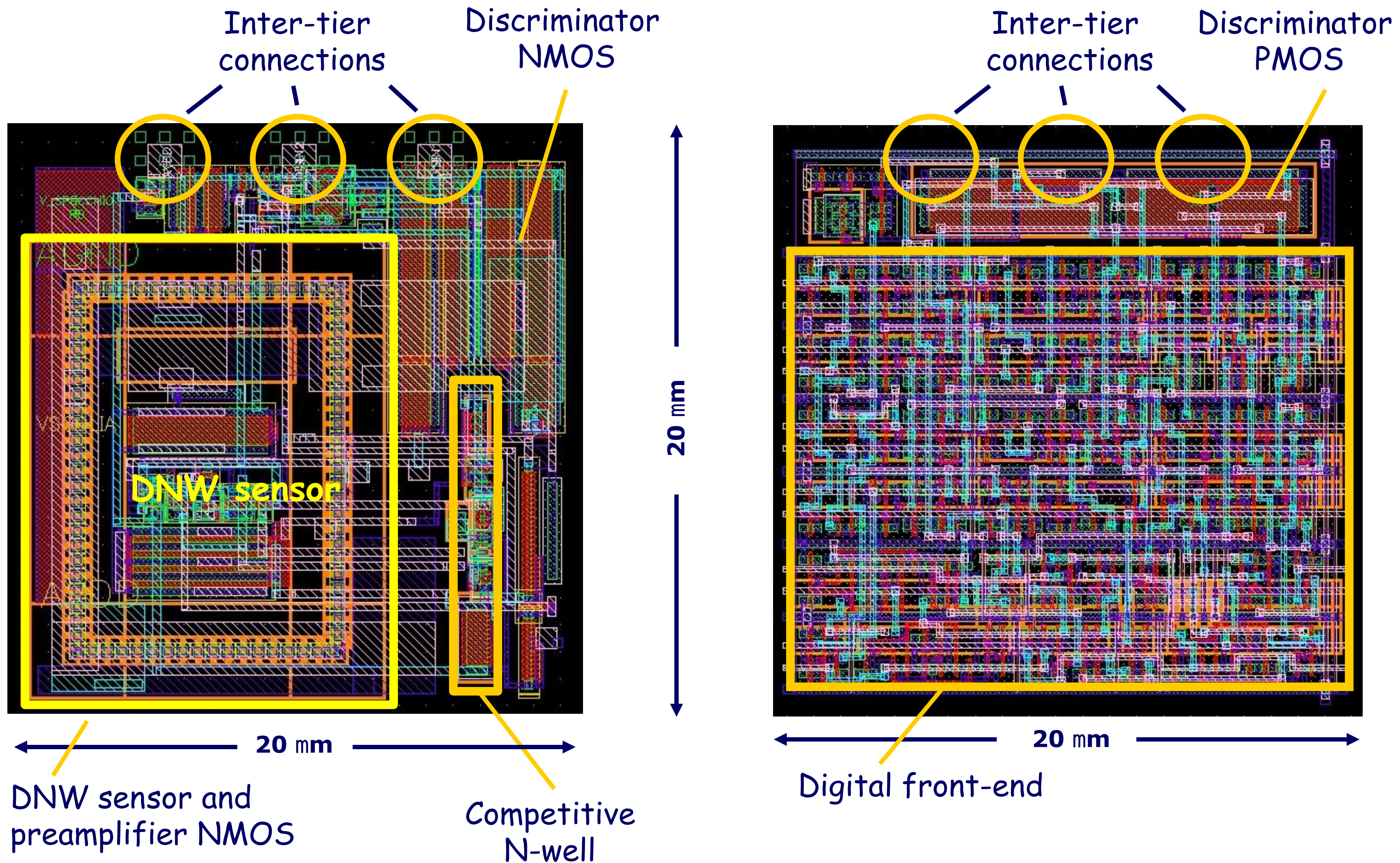
TS=Time_Stamp

Tkin=token_in

Tkout=Token_out

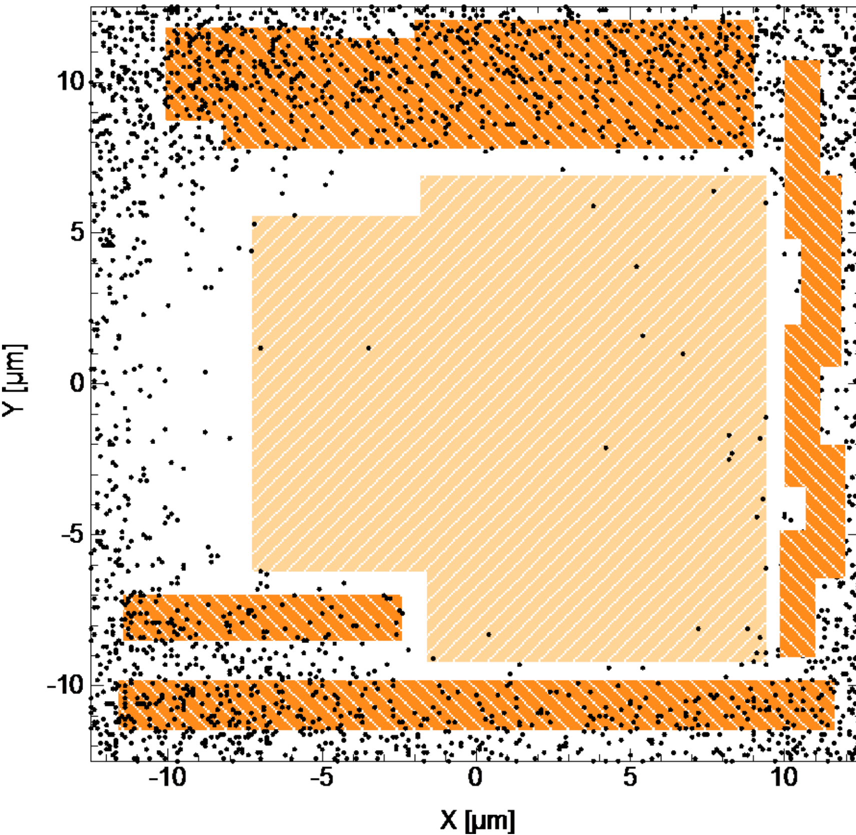
The number of elements may be increased without changing the pixel logic (just larger X- and Y- registers and serializer will be required)

Layout of the 2-tier 20 μm x 20 μm pixel cell

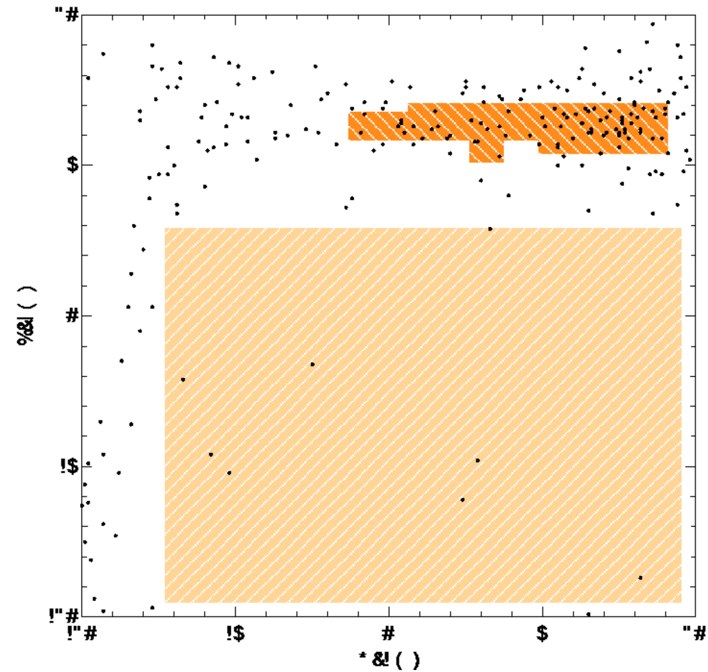


Detection efficiency in 2D and 3D DNW CMOS sensors (simulations)

2D 25x25μm² pixel



3D 20x20μm² pixel

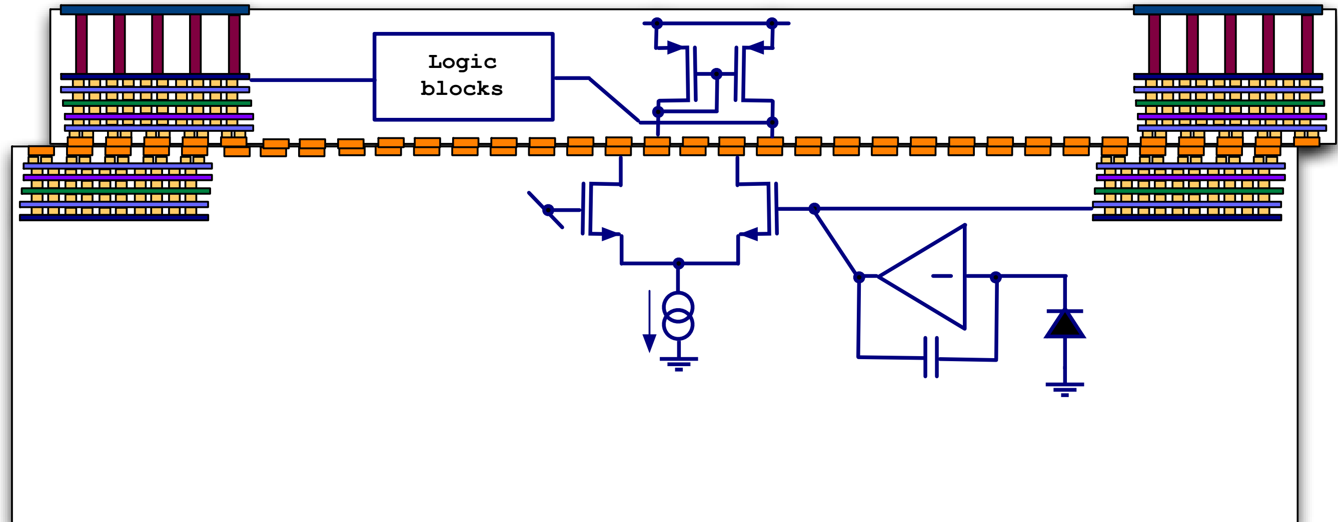


Moving most PMOS to the digital layer strongly reduces undetected hits (black dots in the pictures). In the 3D device, the fill factor is larger than 90 % (ratio between the DNW area and the total area of N-wells), which may lead to a detection efficiency close to 99% (see next)

The first 3D DNW CMOS sensors: experimental results

- The processing of 3D devices started about 3 years ago at Tezzaron/GlobalFoundries and, after many technical problems, only **recently (summer 2012) fully functional chips were delivered**. This is a signature that advanced 3D technologies have not yet reached a full maturity.

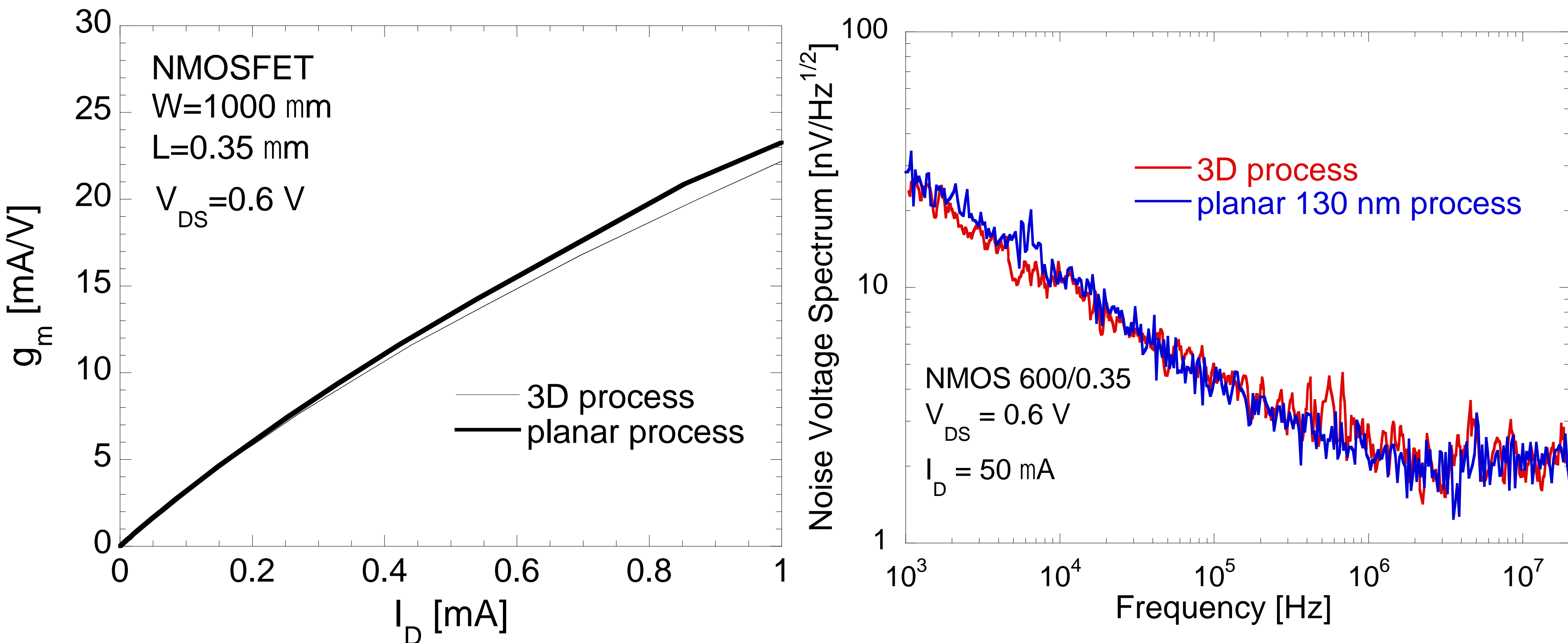
An example of what can go wrong: misalignment in inter-tier connection pads



- However, eventually **very good test results on fully working 3D chips provide a demonstration of the potential of 3D integration**, and stimulate further work.

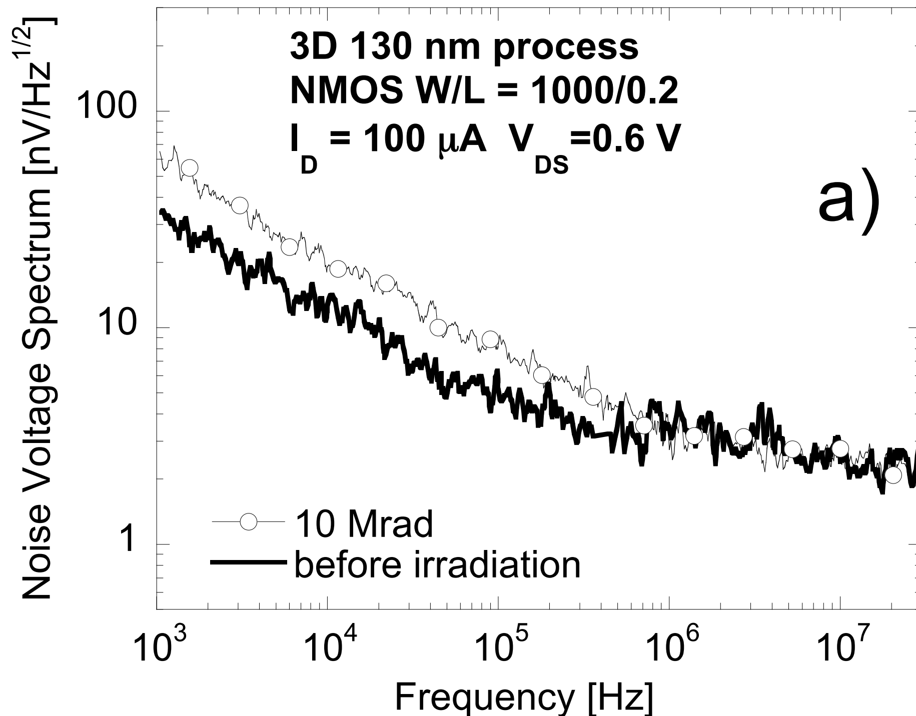
3D processing and MOSFET performance

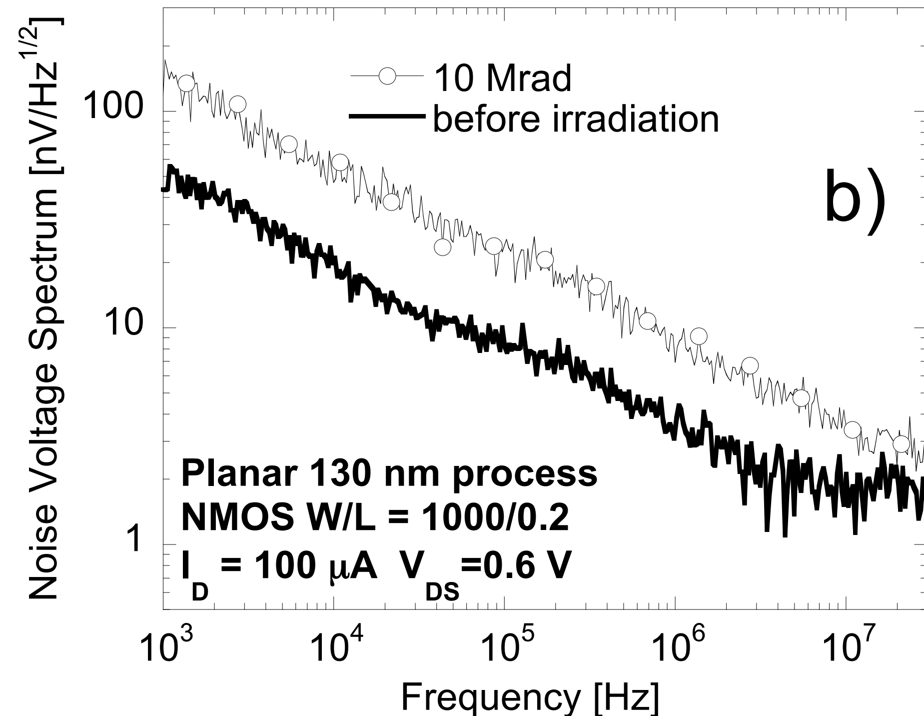
- **Processing steps associated to 3D integration** involve TSV etching and filling (with mechanical stress on surrounding regions of the silicon bulk), wafer bonding at relatively high temperatures, wafer thinning (12 μm), …
- These steps **do not degrade performance of transistors** in the thinned layer, with respect to standard CMOS devices in the same 130nm technology node



3D processing and MOSFET radiation hardness

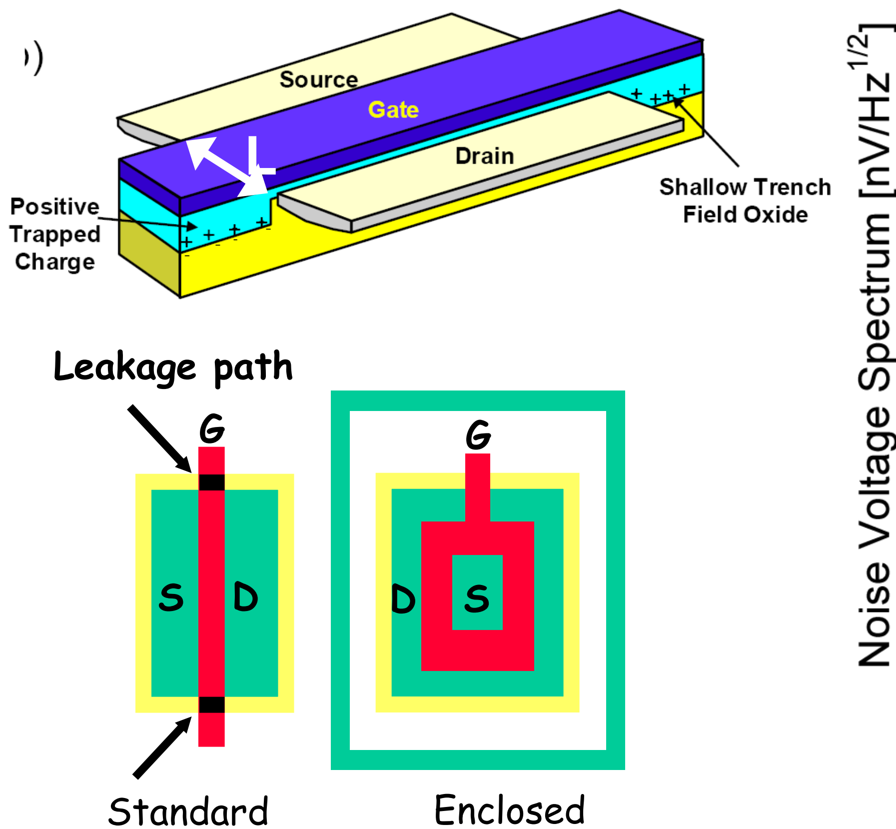
- **3D processing does not degrade MOSFET behavior after exposure to ionizing radiation.** At small drain currents, standard NMOSFETs show a **moderate radiation-induced increase of 1/f noise**, of a similar magnitude as in standard (2D) 130 nm CMOS. This effect is associated with noisy lateral parasitic transistors, which are turned on by radiation induced positive charge buildup in isolation oxides.

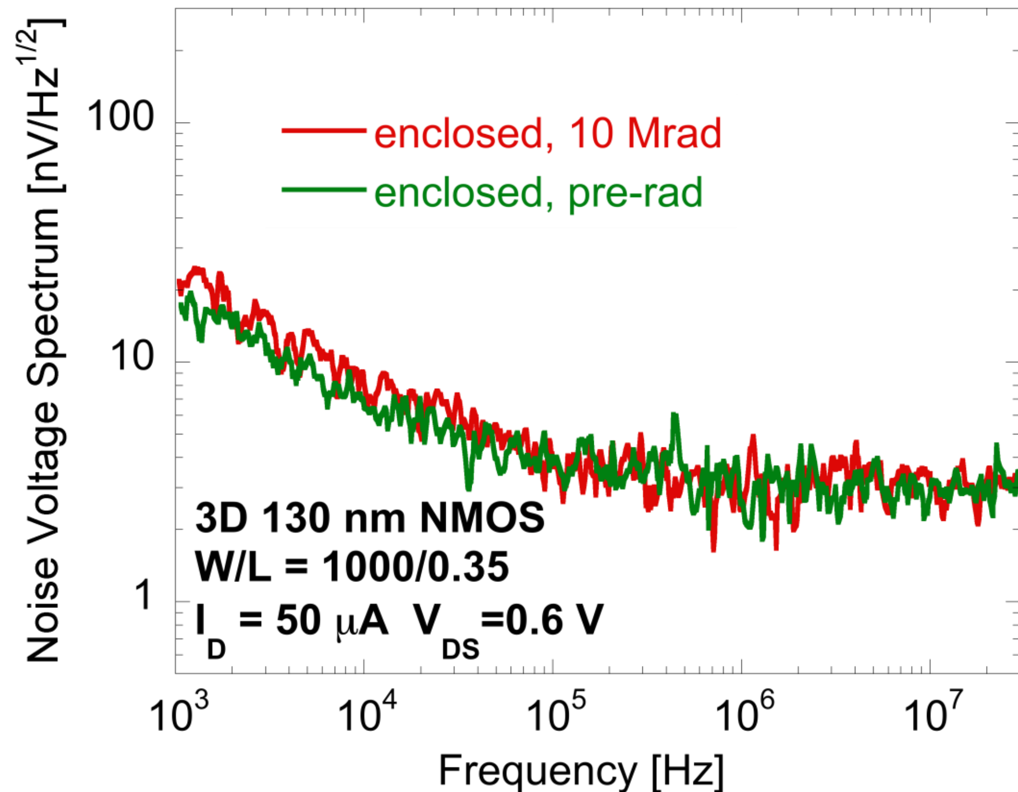




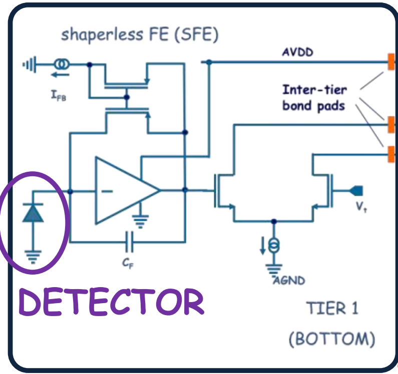
3D enclosed NMOSFETs

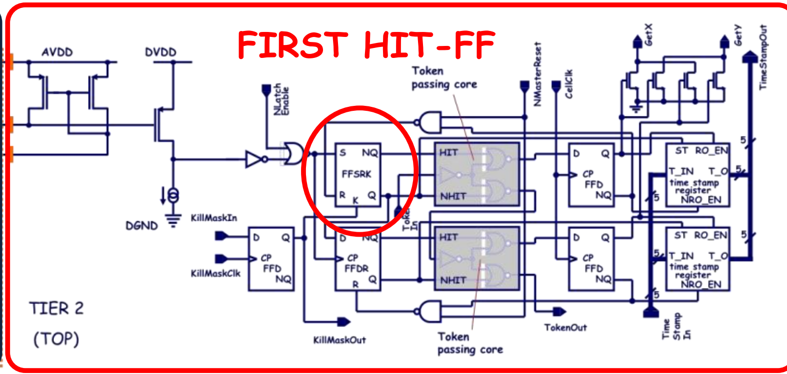
- The enclosed layout geometry has been successfully used since the 250 nm node to achieve a **large tolerance to very high total doses** of ionizing radiation, by **removing lateral leakage paths along lateral thick oxides**. As expected, this technique works also in 3D-IC 130 nm MOSFETs in the Tezzaron/GlobalFoundries process.



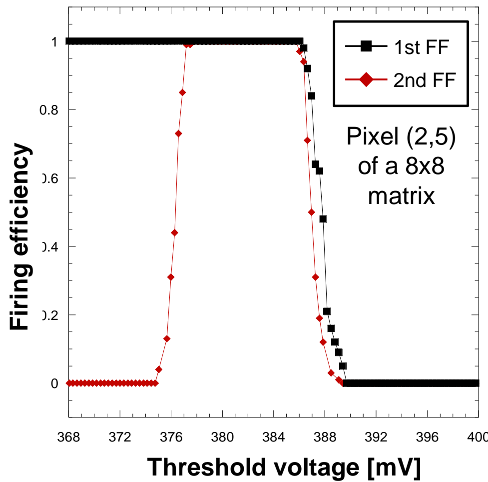


Tests on digital and analog section of 3D DNW sensors





- Tests on SDR1 digital circuits show the full functionality of vertically integrated chips



CELL ENABLE (when it is low, it enables the FIRST-HIT FF)

MASTER RESET
(when it is low, it reset the FF)

VTH

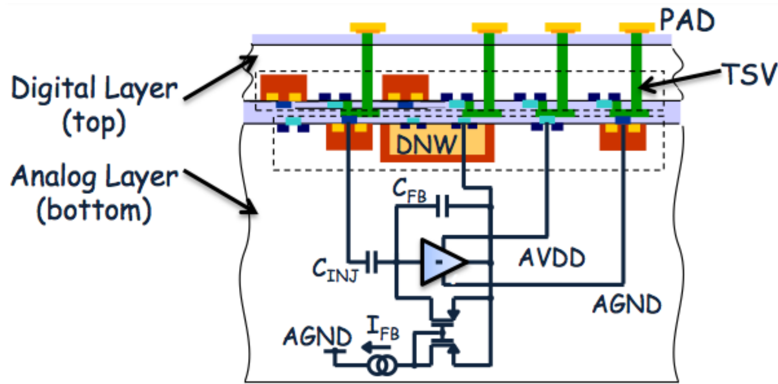
PA OUTPUT

Hit

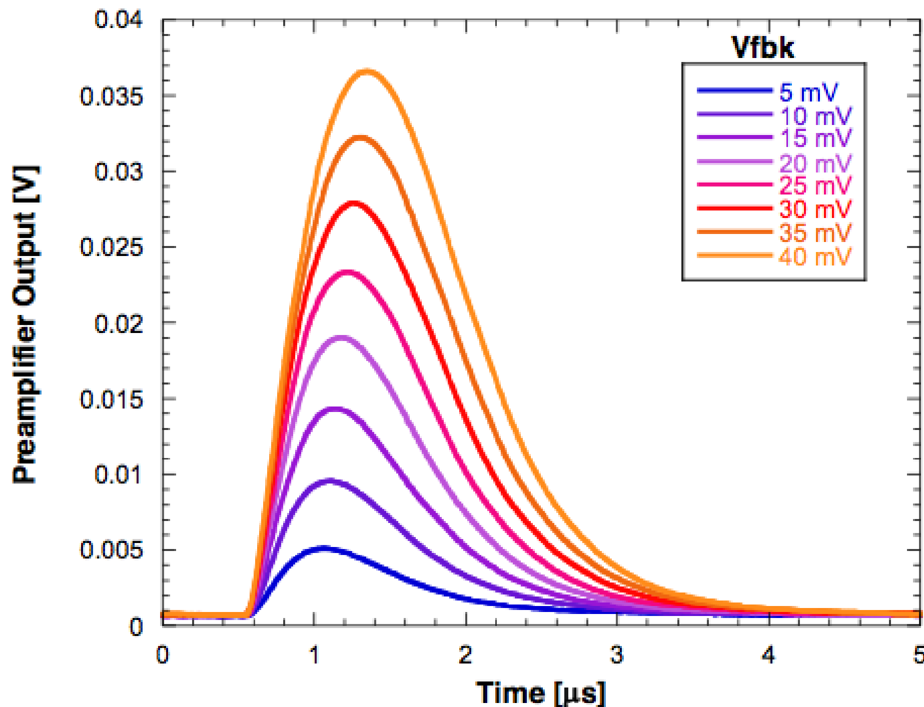
Reset

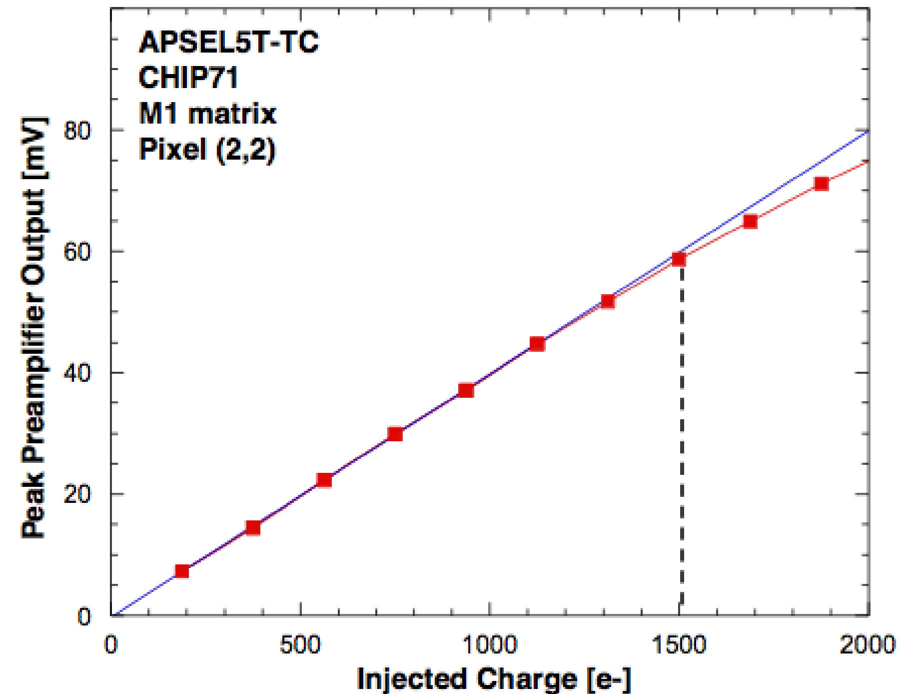
OUTPUT SIGNAL
of the FIRST-HIT FF

3D DNW MAPS: analog front-end characterization



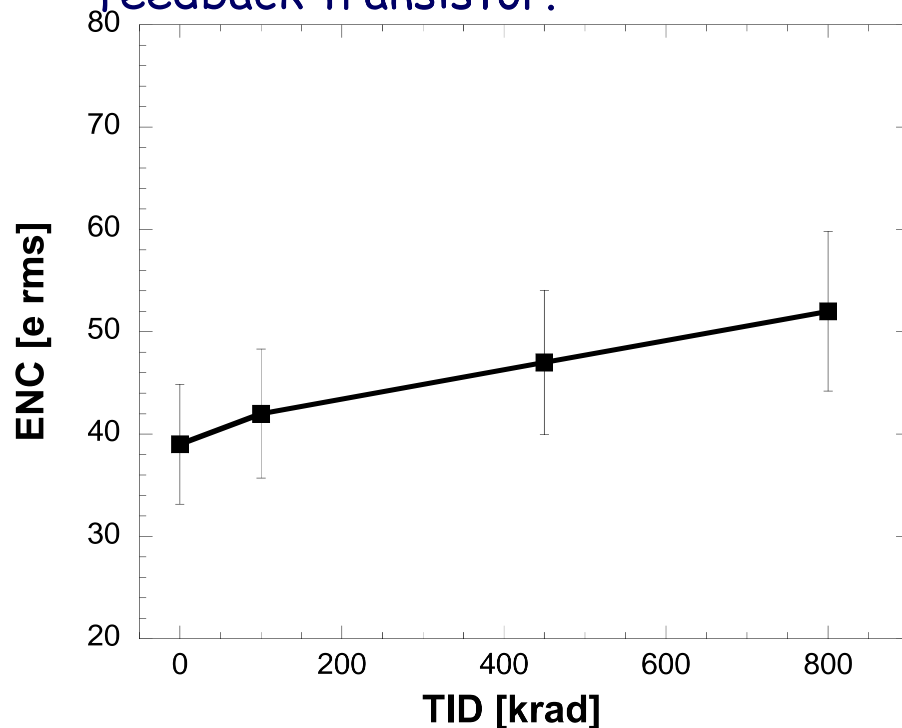
- Charge sensitivity: 550 mV/fC
- Input linear dynamic range: 1500 electrons
- ENC: 40 electrons rms
- Power dissipation: 5 μW/pixel (with power cycling capability)

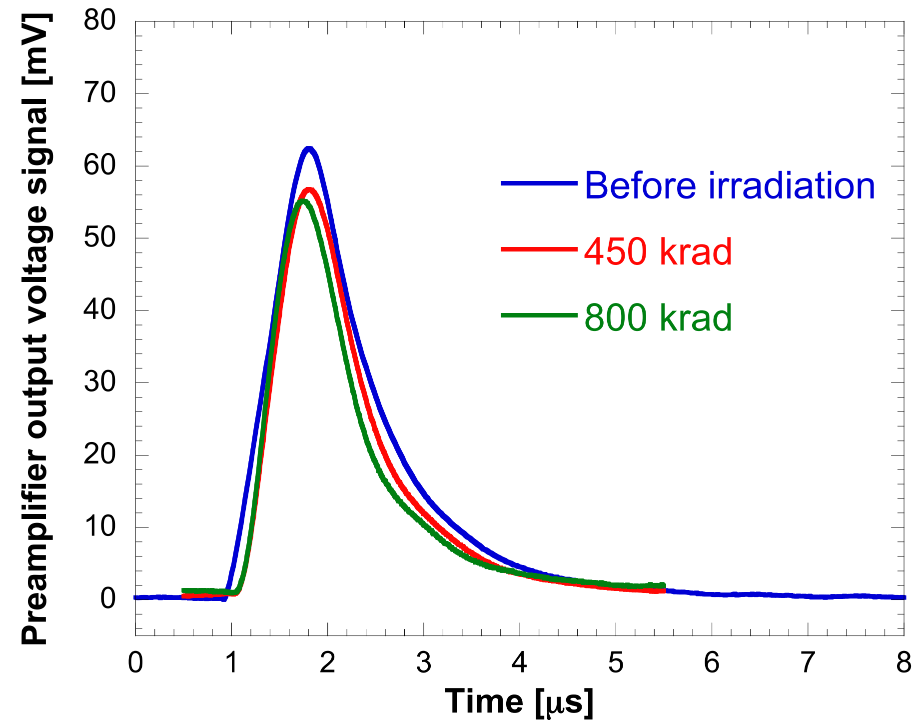




Ionizing radiation effects on 3D CMOS sensors

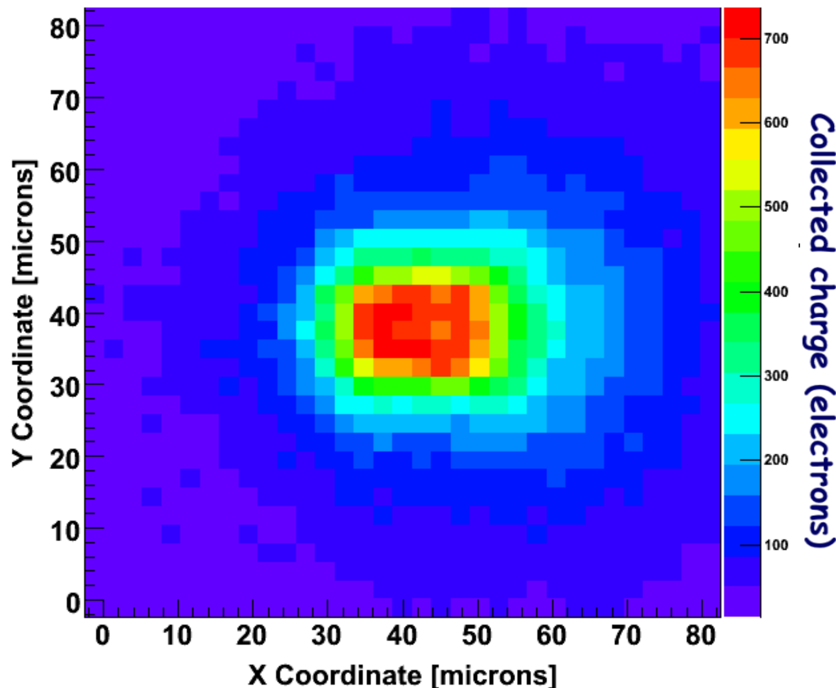
- Radiation-induced noise increase is due to the 1/f noise in the preamplifier input device, which is affected by ionizing radiation (see before). An enclosed layout may cure this problem.
- As in previous 2D versions of the sensor, the charge sensitivity of the analog section is reduced because of a faster signal return to the baseline after irradiation: this is due to the increased leakage current of the sensing electrode, which in turn increases the drain current of the preamplifier feedback transistor.

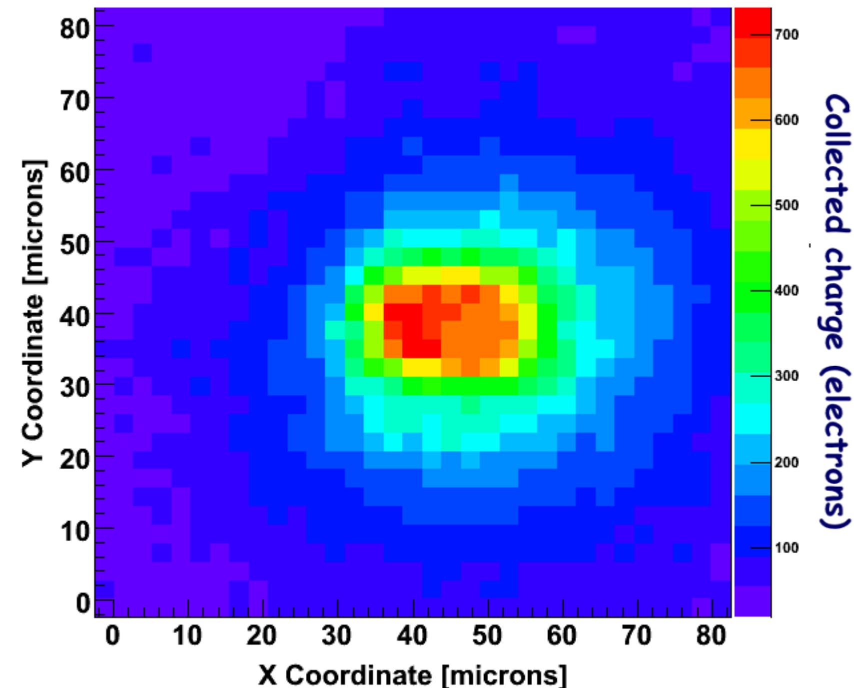




Ionizing radiation effects on 3D CMOS sensors

- Total ionizing dose damage in the silicon bulk of a CMOS sensor is expected to be negligible. So, the charge collection process (which mainly takes place by diffusion) is not impaired by the creation of bulk defects that may reduce the lifetime of minority carriers. After irradiation there is no sizable variation in the profile and amount of the collected charge in 3D CMOS pixel sensors exposed to an infrared laser source.

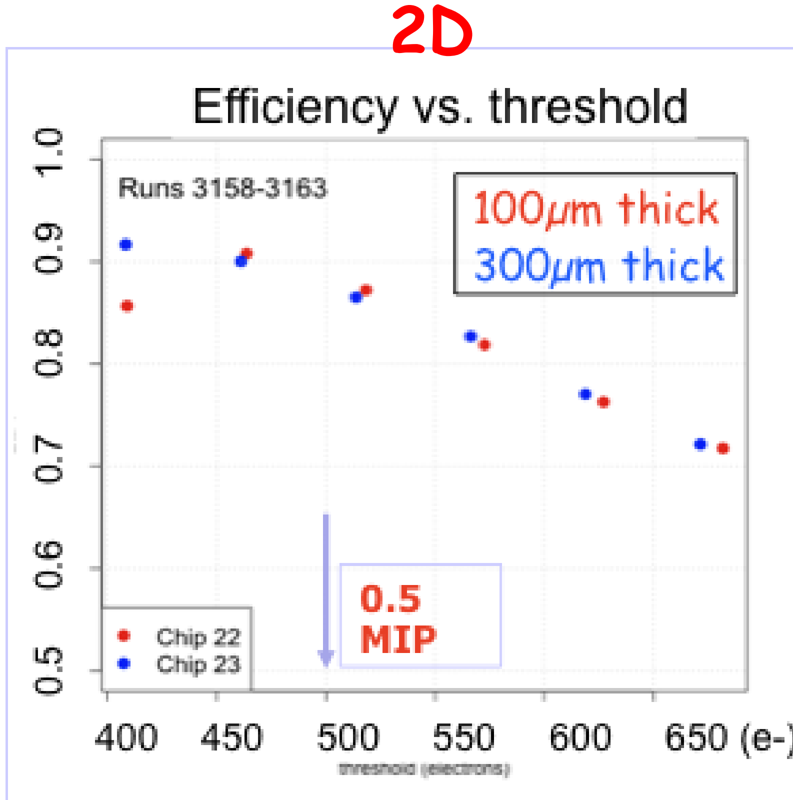


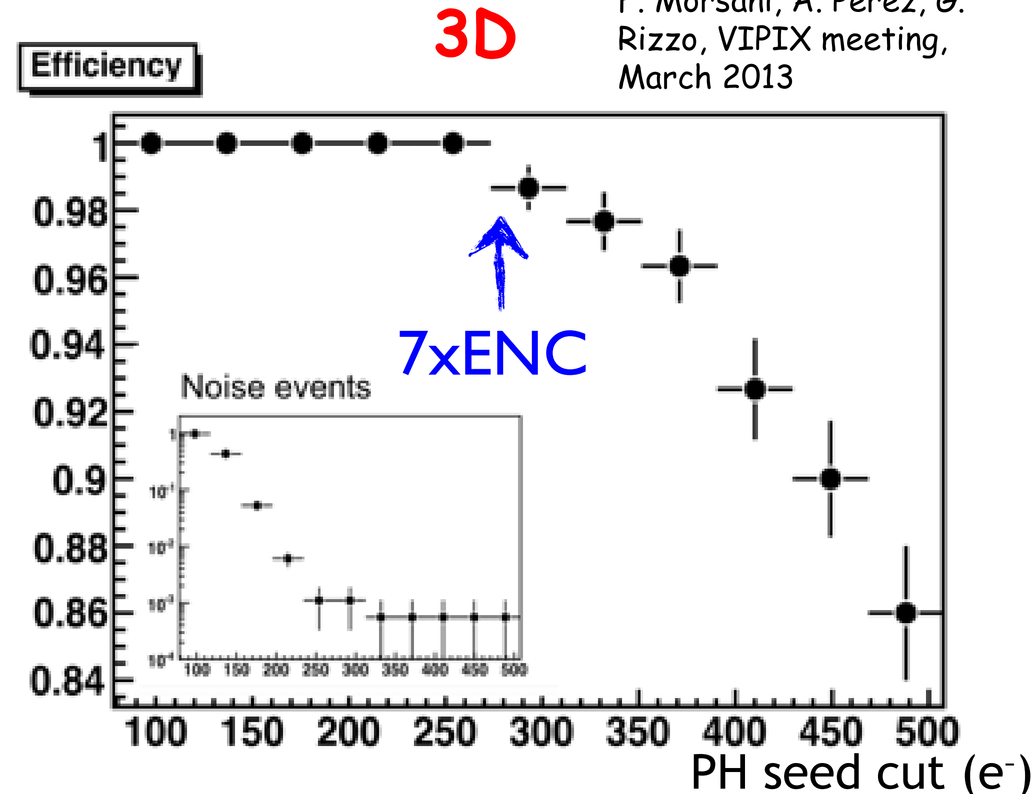


3D integration improves efficiency of DNW CMOS sensors

- In the first 3D-IC run, besides "ILC-like" devices, we had also DNW CMOS sensors with continuous sparsified readout (originally developed for SuperB, which was then cancelled), called APSEL.
- Beam test results on these 3D APSEL prototypes confirm the advantage in charge collection efficiency with respect to previous 2D versions, because of the reduction of the area of competitive PMOS N-wells.

S. Bettarini, G. Casarosa, F. Morsani, A. Perez, G. Rizzo, VIPIX meeting, March 2013

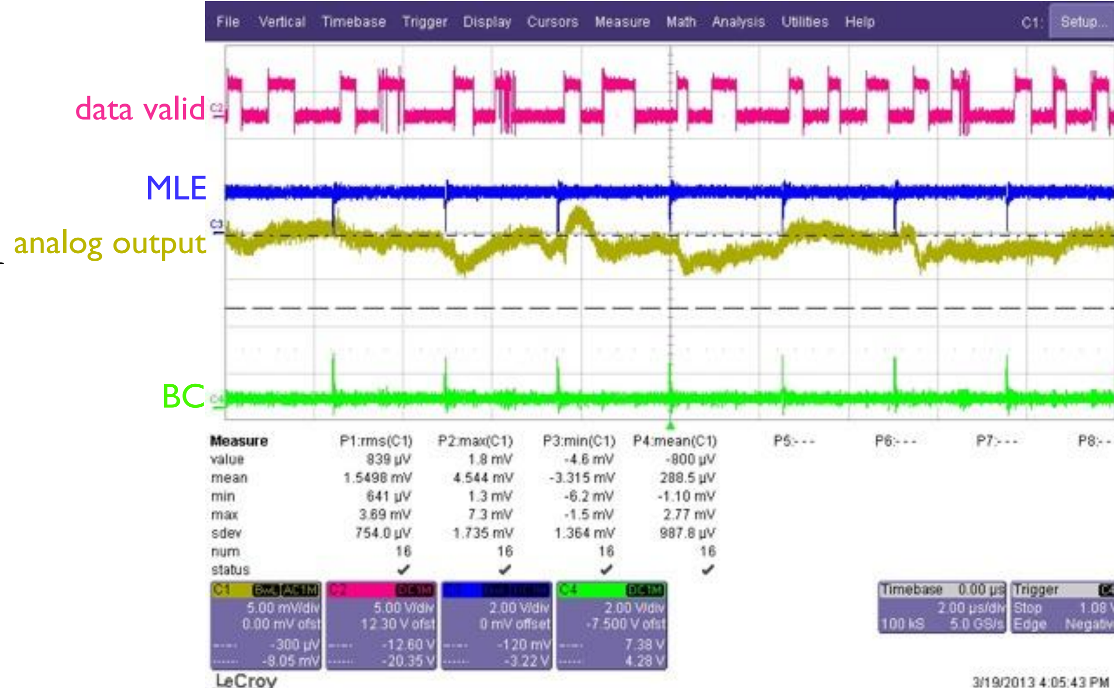




3D integration reduces digital-to-analog interferences

- In the APSEL chips, the digital readout is always up and running (50 MHz clock), sending out data from hit pixels. In 2D versions, coupling of digital signals to the analog front-end was not negligible.
- In the 3D version, thanks to the **separation of the analog and digital substrates**, digital-to-analog interferences are drowned in the electronic noise and do not give spurious hits.

readout running:



S. Bettarini, G. Casarosa, F. Morsani, A. Perez, G. Rizzo, VIPIX meeting, March 2013

A new generation of 3D chips

- The yield, reliability and turnaround time of the aggressive 3D process we used so far still seem to be an issue.
- Since an experimental proof of 3D-related performance advantages was provided by the first 3D-IC run, there are plans for submitting two new 3D chips, whenever a viable access is provided to the technology.

Main analog features	3D APSEL	SUPERPIX1
Charge sensitivity [mV/fC] @ DAC out	700	50
peaking time [ns]	300	250
ENC [e rms]	40 @ C_D=300 fF	180 @ C_D=150 fF
Threshold dispersion before/after correction [e rms]	106/15	560/65
Pitch [μm]	50	50
Matrix size	128x100	128x32
Power/pixel [μW]	36	13.5

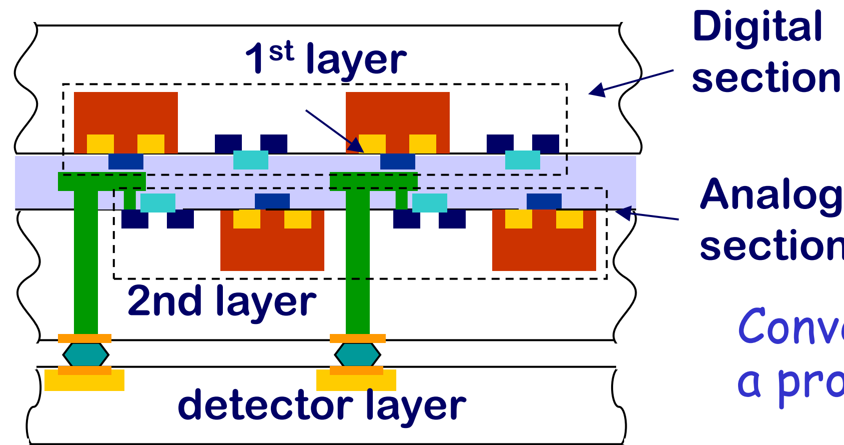
1) Large-scale 3D deep N-well MAPS (3D APSEL)

1) 3D readout chip for high resistivity pixel sensors (SUPERPIX1)

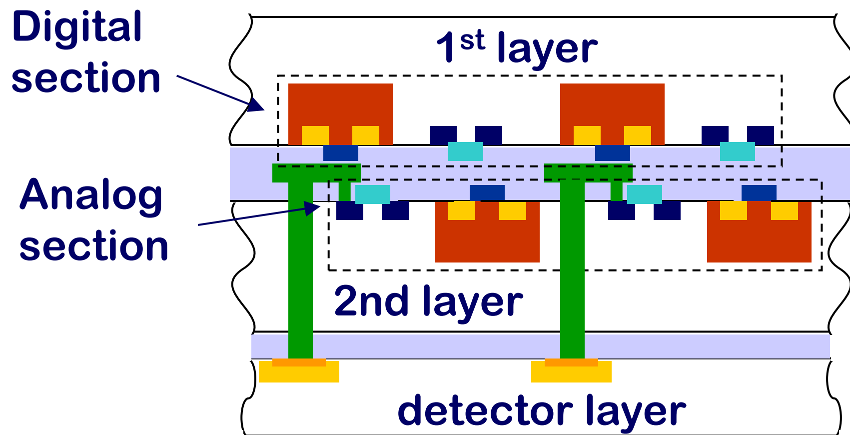
Both chips share a new flexible readout architecture: data push & triggered version

3D readout integrated circuits interconnected to high resistivity sensors:

standard bump bonding vs vertical integration



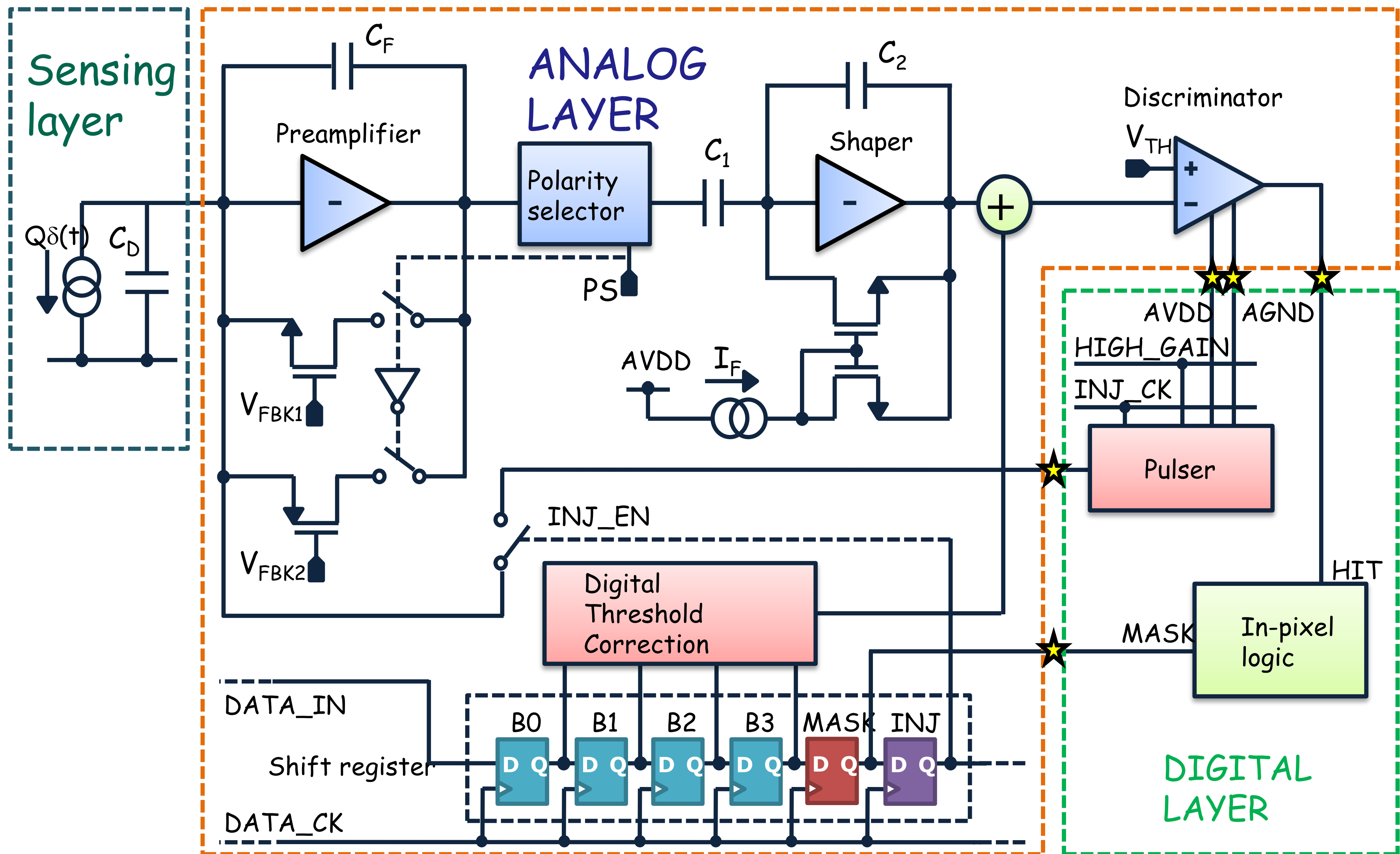
Conventional solder bumps may still pose a problem for low mass assemblies



Low-mass bonding of sensors to readout circuits is possible with advanced high-density interconnection technologies

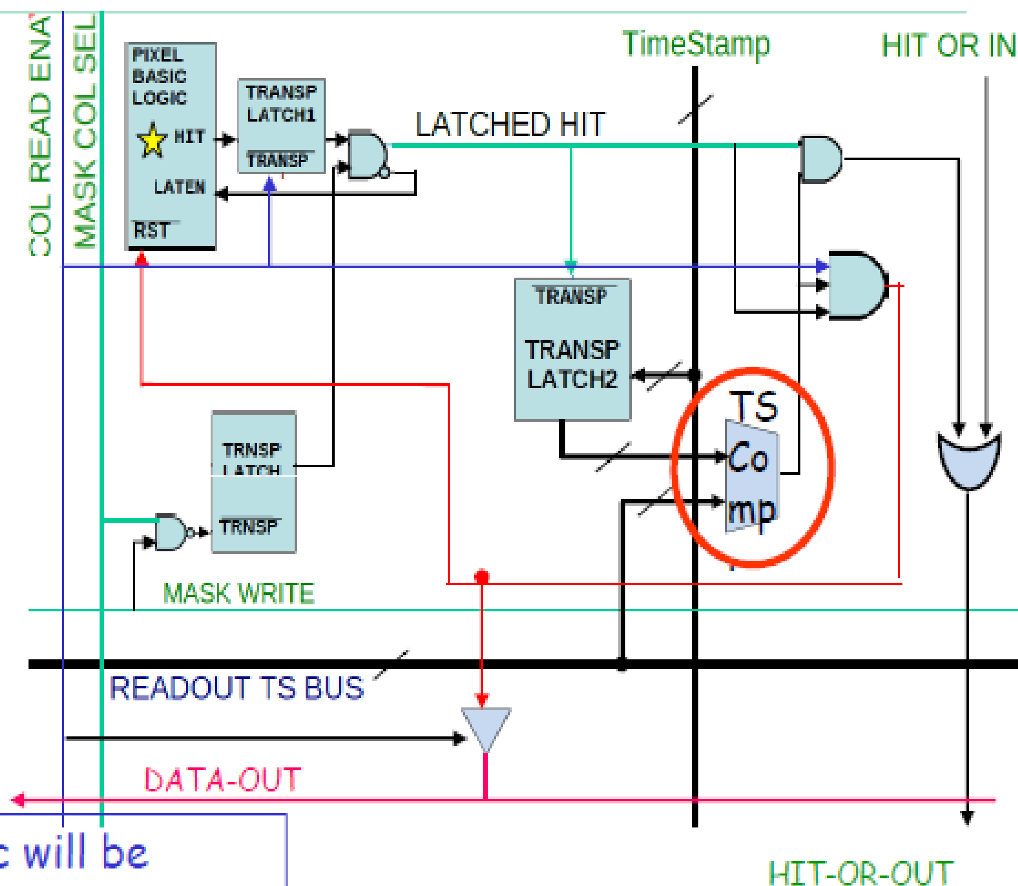
Wafer bonding

Exploiting 3D integration: the analog section of a 3D readout chip for high resistivity pixels (50 μm pitch)



Exploiting 3D integration: pixel-level logic with time-stamp latch and comparator for a time-ordered readout

- No Macropixel
- Timestamp (TS) is broadcast to pixels & pixel latches the current TS when is fired.
- Matrix readout is timestamp ordered
  - A readout TS enters the pixel, and a HIT-OR-OUT is generated for columns with hits associated to that TS.
  - A column is read only if HIT-OR-OUT=1
  - DATA-OUT (1 bit) is generated for pixels in the active column with hits associated to that TS



- This more complex in pixel logic will be implemented with 3D integration without reducing the pixel collection efficiency even improving the readout performance
  (readout could be data push or triggered)

VHDL simulation of the data push chip ($100 MHz/cm^2$ input hit rate)

- Readout Effi > 99 % @ 50 MHz clock with timestamp of 200 ns.

Layout and electronic functions in a 2-tier pixel readout cell (50 x 50 μm^2)

Analog tier

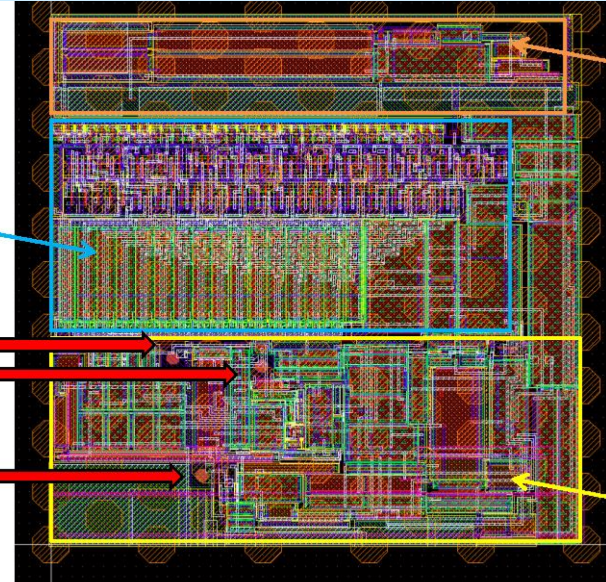
DRC

LVS

Routing

DAC, decoder and shift register

3 connections PA input – bump bond pad (Supercontact)



Discriminator

Preamplifier, polarity selector and shaper blocks

Digital tier

(includes a pulser for an accurate calibration of the pixel cell)

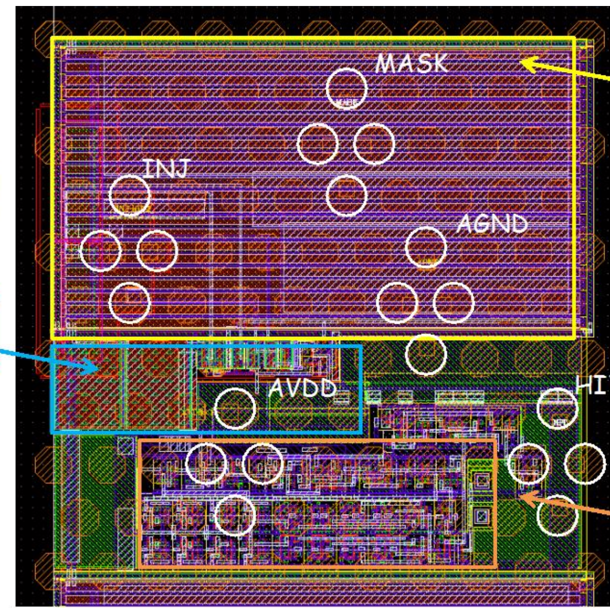
DRC

LVS

Routing

Integration with digital front-end (Fabio)

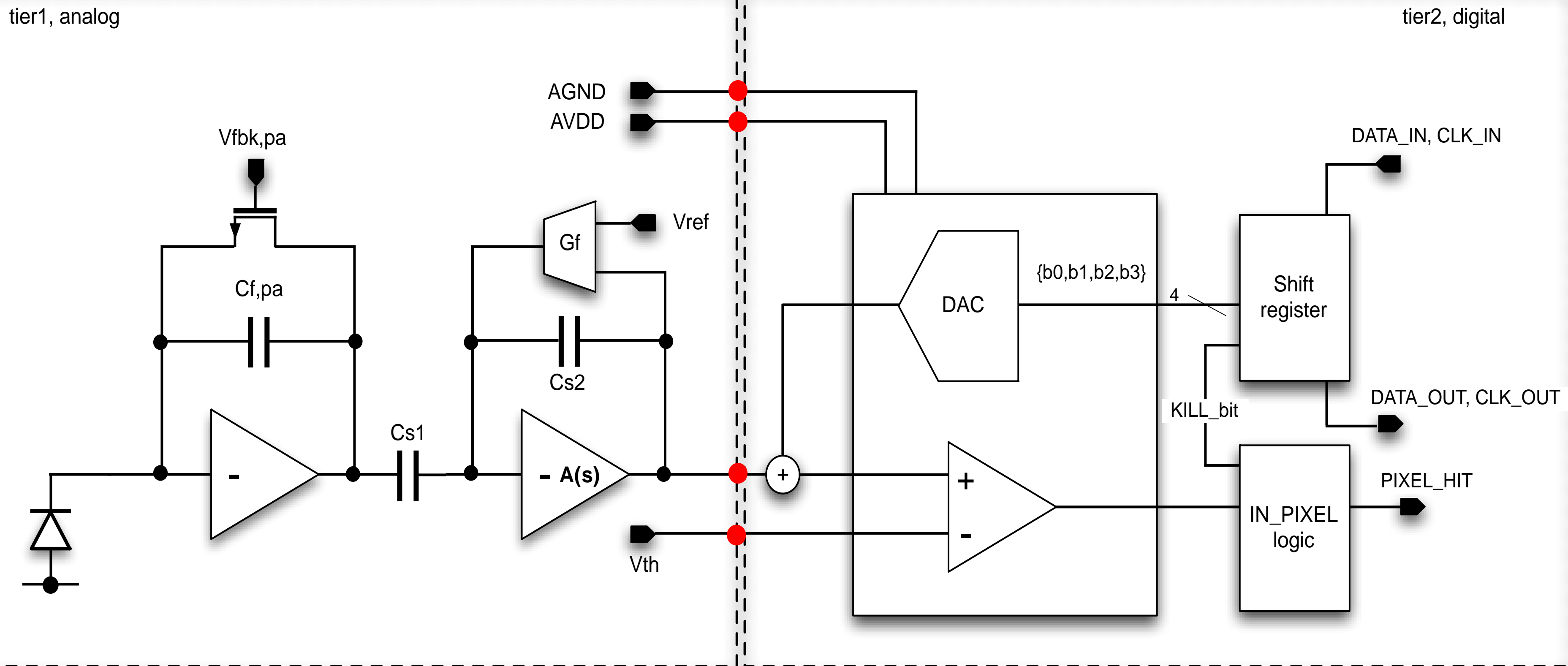
Pulser circuit



poly resistors

In-pixel logic

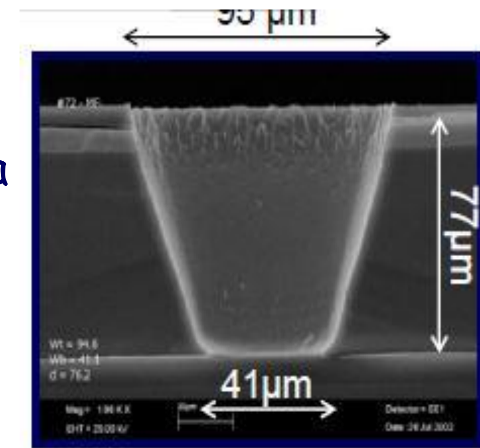
ApselVI front-end architecture



Thanks to 3D integration, the addition of a shaping stage in the analog tier makes it possible to independently optimize noise and threshold dispersion (also with a DAC for local threshold adjustment), achieving a high charge sensitivity in a reliable way

Perspectives and support to 3D integration in the semiconductor detector community

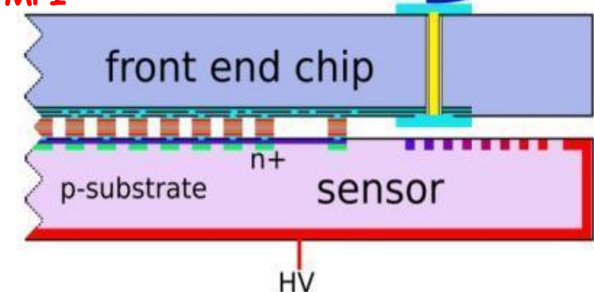
- 3D integrated circuits based on homogeneous layers (same CMOS technology) and high density TSVs and interconnections are a very promising approach to advanced pixel detector readout and other applications.
- The **AIDA WP3** project is supporting the less aggressive **"via last"** variant of 3D integration, where **low-density TSVs are etched in fully processed CMOS wafers**. It is a mature technology, presently available at various vendors.



- This technique makes it possible to **use heterogeneous layers** (different technologies) for sensors and front-end electronics and to fabricate four-side buttable devices with minimal dead area.
- A high-resistivity, fully depleted sensor can be combined in a low-mass assembly with a readout chip designed in an aggressively scaled CMOS generation (usually not available in the typical MAPS "Opto"processes), both with excellent radiation hardness (among other properties).

See next talk by A. Macchiolo, MPI

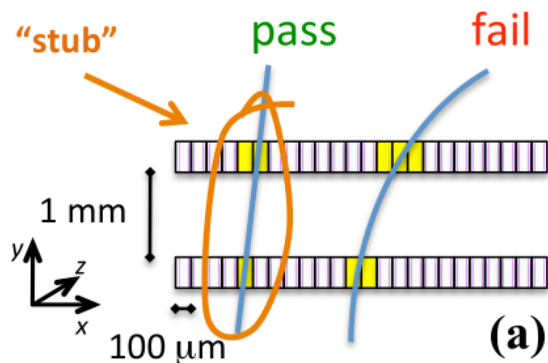
- Low-density peripheral TSVs can be used to reach backside bonding pads for external connection. The interconnection technology can be chosen according to the pixel pitch.



The diversity of 3D integration approaches: "via first" vs "via last"

- Different approaches to 3D integration differ in terms of the minimum allowed pitch of bonding pads between different layers and of vertical Through-Silicon Vias (TSVs) across the silicon substrate.
- Even with not so aggressive 3D technologies (the so-called "via last" ones, where TSVs are fabricated on fully processed CMOS wafers), a significant advantage can be gained by designing a 2-tier readout chip (for example, analog layer + digital layer)
- In most cases, only one or two connections are needed between the analog and digital blocks of a single pixel cell, and the digital layer can use low-density peripheral TSVs (pitch > 50 μm) to reach backside bonding pads for external connection.
- The "via last" approach was successfully tested by AIDA groups, both for HEP and imaging applications, and may open the way to new design ideas: a few of them will be discussed in the following slides.

3D techniques in a pixel-strip module for a prompt momentum discriminating tracker at HL-LHC



Provide information for Level-1 trigger processing, with local rejection of signals from low-momentum particles. correlating signals in two closely-spaced sensors.

Optimize pT cut by tuning sensor spacing and acceptance window.

TSV at the periphery of the pixel ASICs "bridging" two rows of chips in the middle, avoiding regions of stub finding inefficiency

D. Abbaneo, A. Marchioro, A hybrid module architecture for a prompt momentum discriminating tracker at HL-LHC, JINST 7 C09001

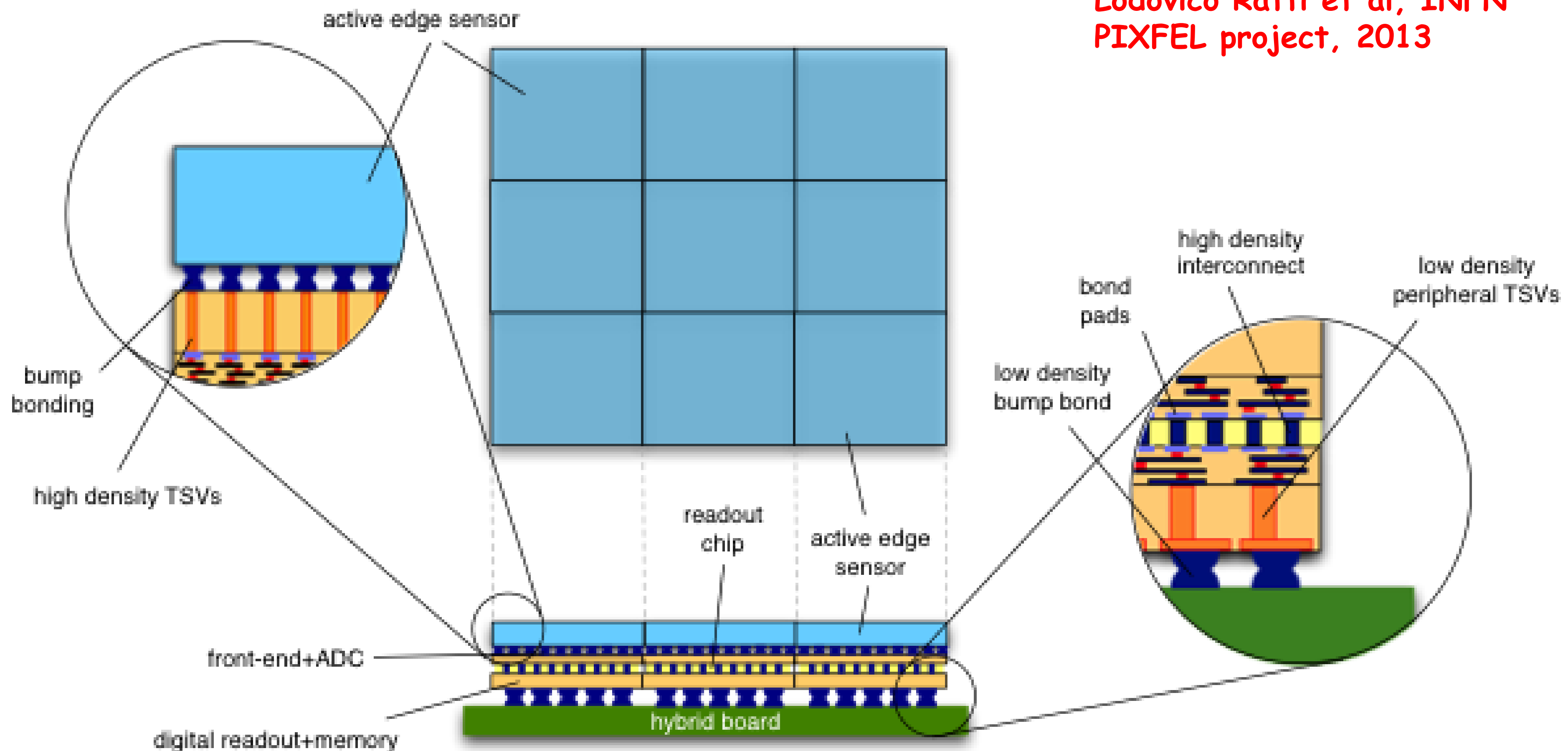
New ideas for 3D integration in photon science

Potential benefits to new detector systems for X-ray imaging at free electron laser facilities:

- Reduction of pixel size to about 50 μm x 50 μm (presently limited by the need of complex electronic functions in the pixel cell)
- Larger memory capacity to store more images
- Advanced pixel-level processing (1 – 10000 photons dynamic range, 10-bit ADC)
- 4-side buttable tiles for a large area detector with minimum or no dead area

Enabling technologies for high-performance 4-side buttable X-ray imaging module: active edge pixel sensors, through-silicon vias, 65 nm CMOS,…

Lodovico Ratti et al, INFN PIXFEL project, 2013



A 3D integrated circuit (AGIPD) for the readout of edgeless pixel sensors for X-ray imaging at XFEL

> mid term: "logic – on - memory"

1) bump-bond to the detector

2) amplification & double sampling

3) ADConversion

4) store the digitalized signal in a digital memory cell

5) digital signal readout

tech #1 (CMOS Low Pow)

tech #2 (CMOS High Perf)

tech #3 (DRAM)

Heinz Graafsma, 532.WE-Heraeus Seminar, May 2013

532. Heraeus-Seminar I May 2013 | Page 33

Conclusions

- The first 3D-IC run provided demonstrators of 3D CMOS chips, and confirmed potential advantages of 3D integration. The problems associated with this run do not have to prevent us to continue pursuing 3D as a way of devising advanced pixel detectors.
- 3D integration is progressing in the microelectronic industry, and we have to be ready to exploit it. Ultimately, it may allow designers to avoid using sub-50 nm processes for analog and digital circuits in very small pixel readout cells.
- R&D activities in these technologies have to be supported by our community, since they enable new concepts for detector systems. AIDA WP3 is doing this job of testing diverse approaches to 3D.
- New detector ideas exploiting 3D integration are being proposed, for particle tracking and vertexing and for X-ray imaging at FELs.

The INFN VIPIX collaboration

VIPIX - Vertically Integrated PIXels

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M. Caccia[6], F. Risigo[6]

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L. Bissi[8], P. Ciampolini[8], A. Marras[8], G. Matrella[8], P. Placidi[8], E. Pilicer[8], D. Passeri[8], L. Servoli[8], P. Tucceri[8]

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[7]Università degli Studi di Trento and INFN Padova

[8]INFN Perugia

[9]INFN Roma III

Backup slides

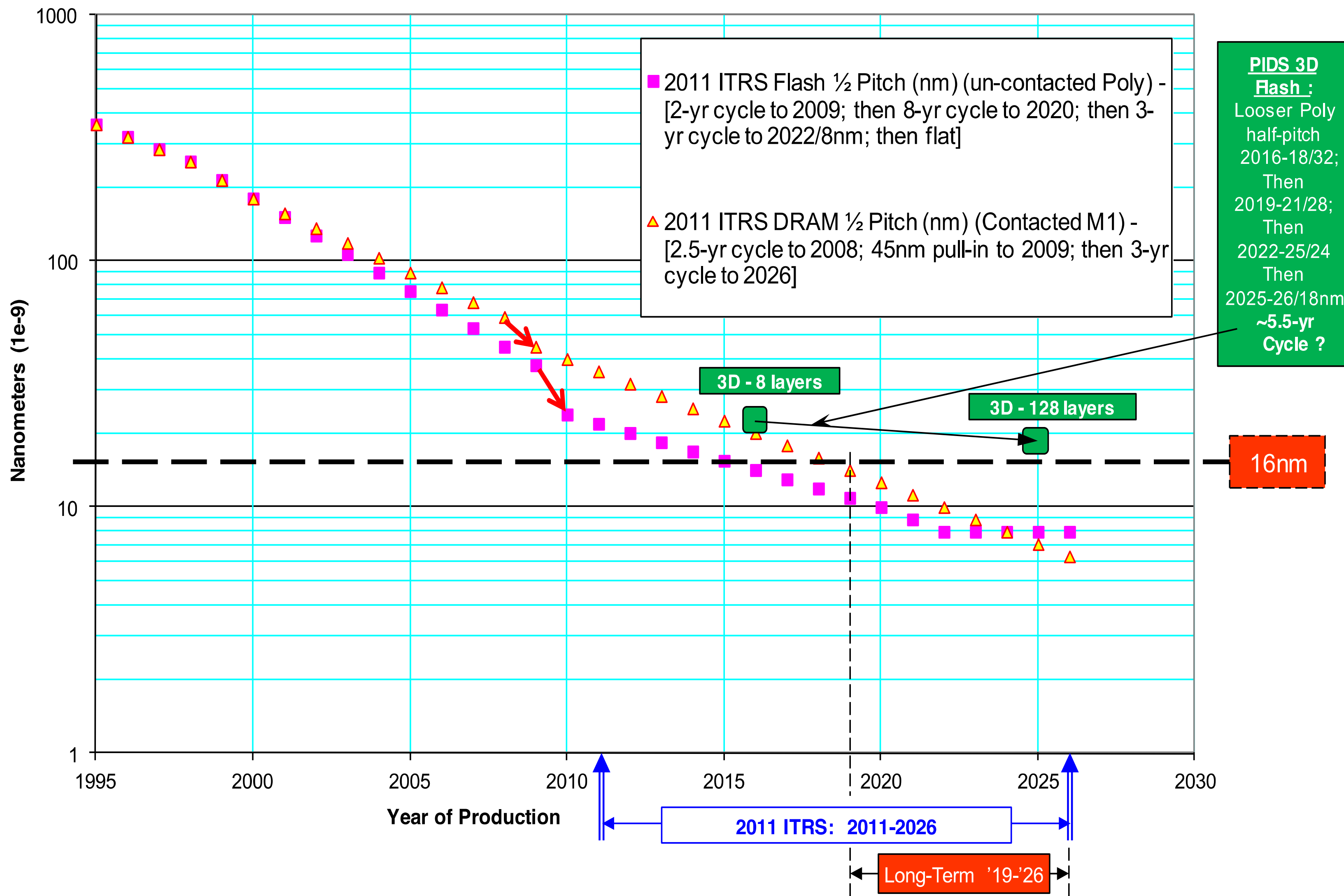
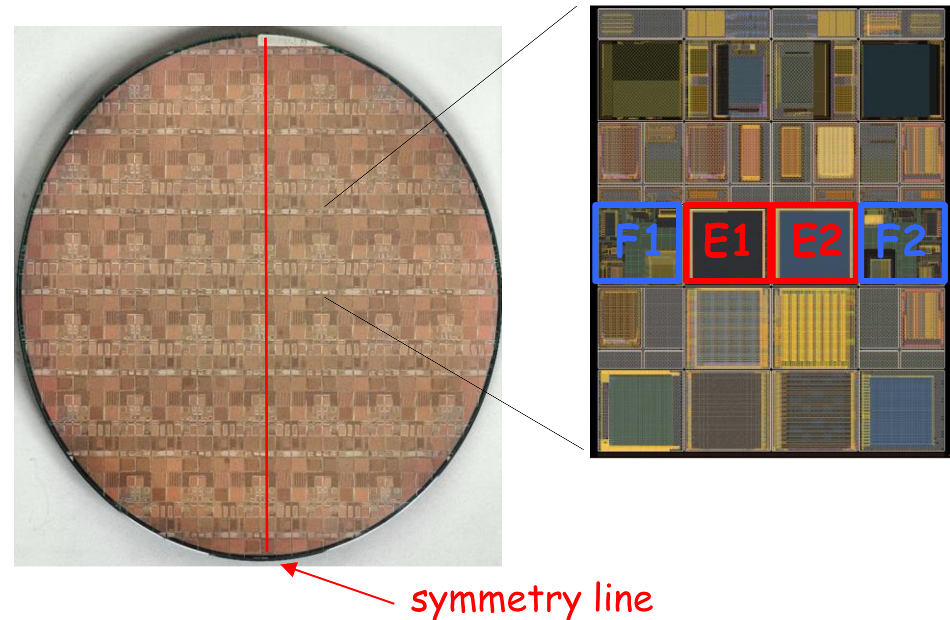


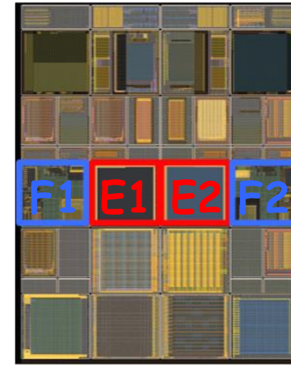
Figure ORTC3 *2011 ITRS—DRAM and Flash Memory Half Pitch Trends*

First MPW run of the 3D-IC consortium

- ✓ Several groups from US and Europe have been involved in the first 3D MPW for HEP (pixel and strip readout chips for ATLAS, CMS, B-factory, ILC) and photon science applications (X-ray imaging)
- ✓ Single set of masks used for both tiers to save money
  - ✓ identical wafers produced by Chartered (now GlobalFoundries) and face-to-face bonded by Tezzaron
  - ✓ backside metallization by Tezzaron



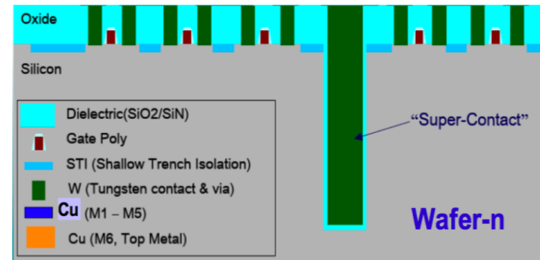
Top layer flipped over



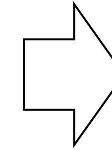
Bottom layer

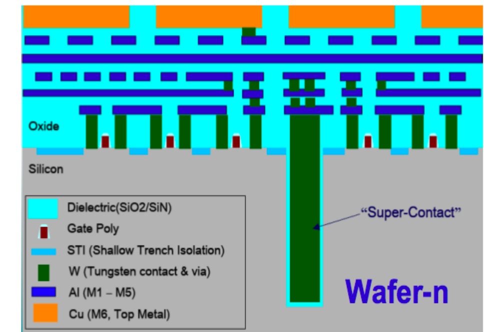
Tezzaron vertical integration (3D) process

Tezzaron uses a "via middle" approach for the fabrication of 3D chip

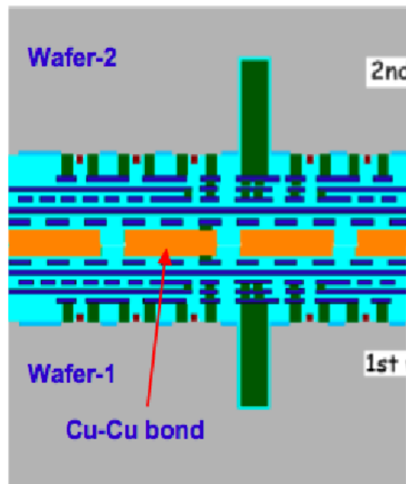


Step 1: On all wafer to be stacked complete transistor fabrication, form TSV, passivation and fill TSV at same time connections are made to transistors

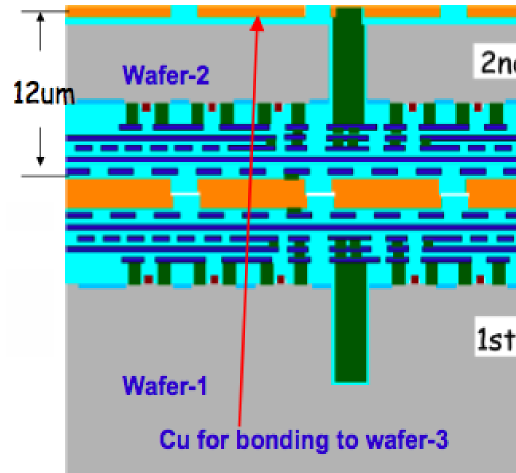




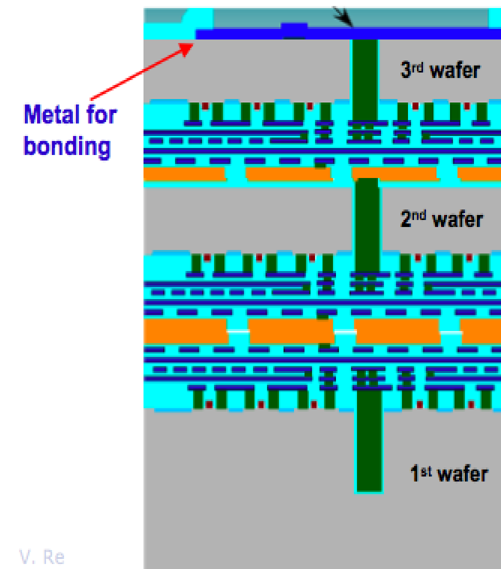
Step 2: Complete back end of line (BEOL) process by adding Al metal layers and top Cu metal (0.7um)



Step 3: bond wafer 2 to wafer 1 (Cu-Cu thermo-compression bond)



Step 4: thin the wafer 2 to about 12um to expose TSV. Add Cu to back of wafer 2 to bond wafer 2 to wafer 3 OR add metallization on back of wafer 2 for bump bonding or wire bonding



V. Re

Step 5: stack wafer 3, thin wafer 3 to expose TSV, add final passivation and metal for bond pads.