Development of pixel sensors with 25x500μm² pitch for the ATLAS HL-LHC upgrade

Presenter: Helen Hayward

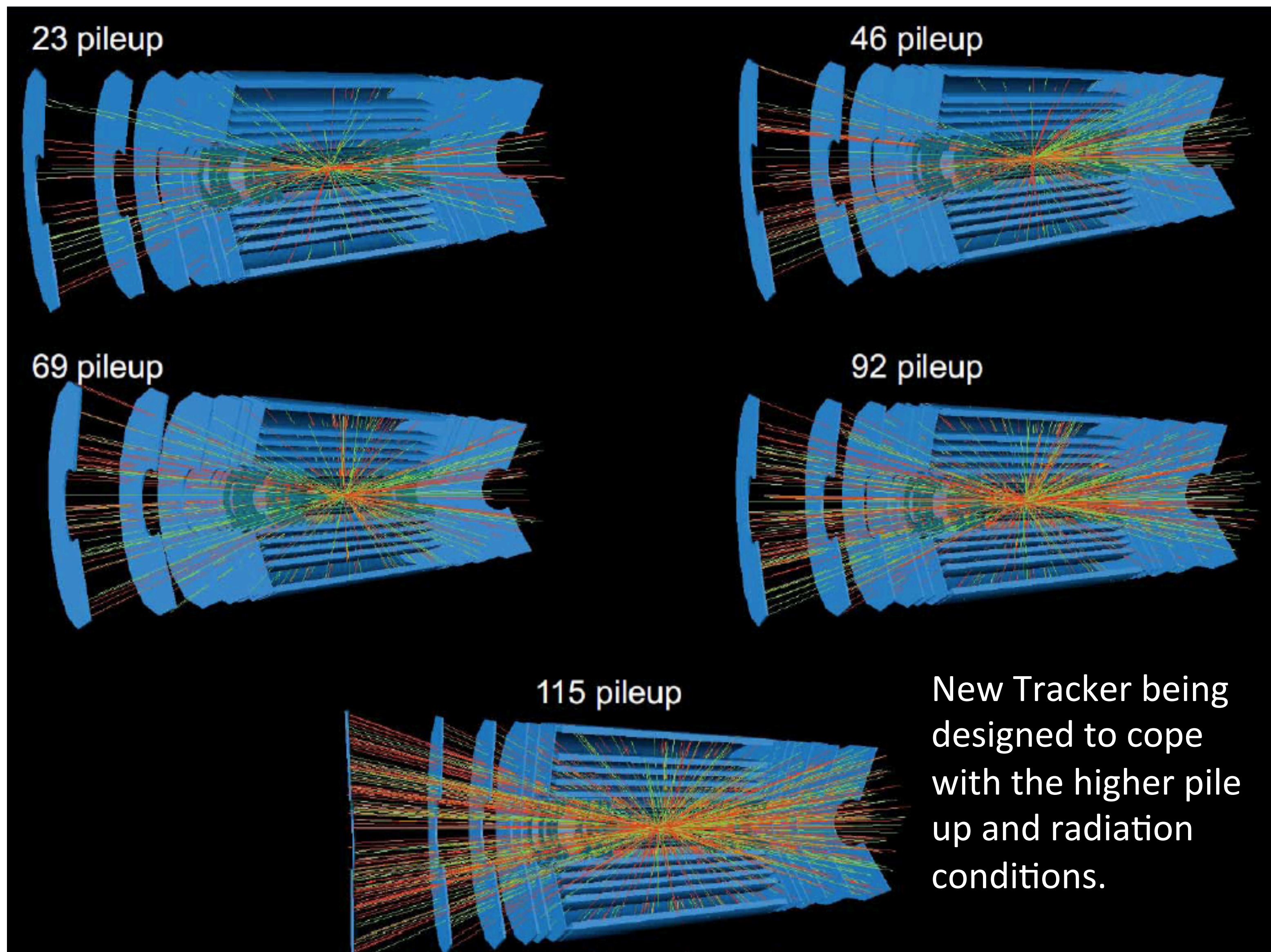
Secondary Authors:
Dean Forshaw
Sergey Burdin, Gianluigi Casse

9th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors, Hiroshima, Japan

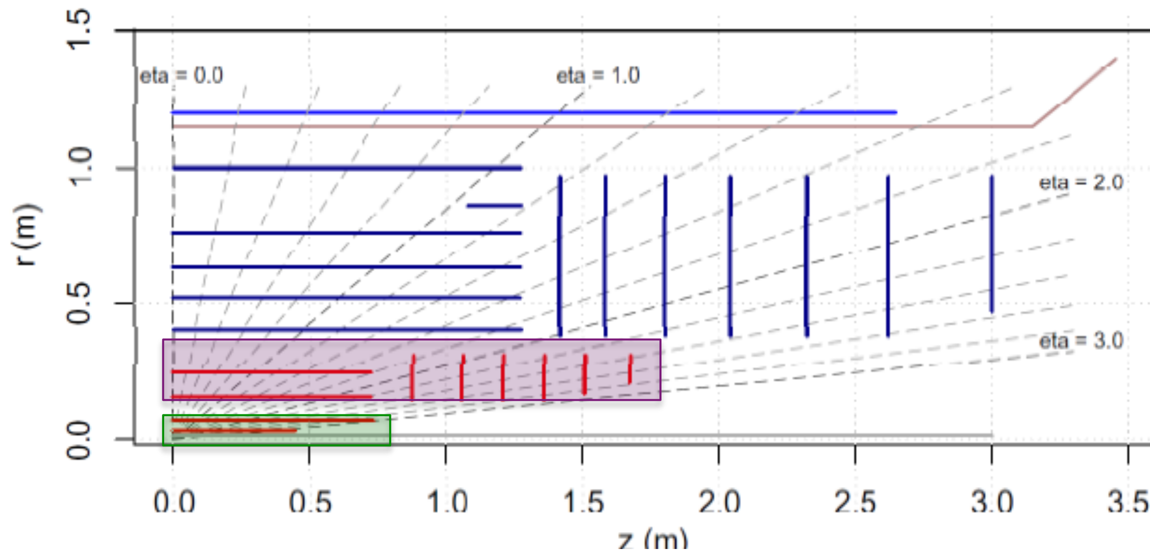
Contents

- **Motivation:**
  - Upgrade of ATLAS tracker detector for the HL-LHC
- **Devices**
  - CERN Pixel V – alternative geometries
- **Performance**
  - Sensor performance
- **Conclusion**

HL-LHC Pileup



ATLAS Itk – LOI design



- 4 pixel barrel layers
  - Radius from 39 mm to 250 mm
  - Z: ±449 mm to ±694 mm (outer 2 layers)
- 6 Pixel disks
  - R_{inner} = 150 mm
  - R_{outer} = 315 mm
  - Z: 820 mm to 1890 mm

2 outer Barrel layers / Disks

- Sensor
  planar n-in-p
  150 µm
- Pixel size **50 µm x 250 µm**
- ROIC thickness 150 µm
- ToT = 4 bits
- 2x2 (Quad) and 2x3 (Hex) chip modules
- Data rates of 640 Mbit/s per module

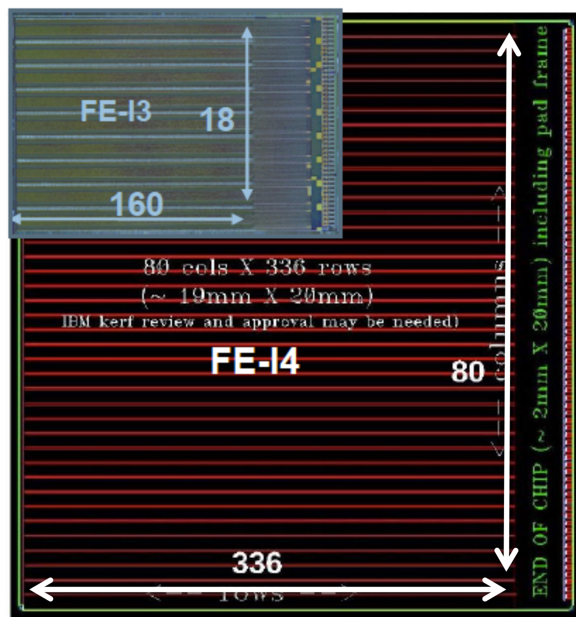
2 Inner Barrel layers

- Sensors
  All sensor materials possible
  150 µm silicon or thinner
- Pixel size **25 µm x 150 µm**
- ROIC thickness 150 µm
- ToT = 0-8 bits
- 2x1 and 2x2 chip modules
- 2x2 sensor = 33.9 mm x 40.6 mm
- Data rate as high as 2 Gbit/s per module

Goal

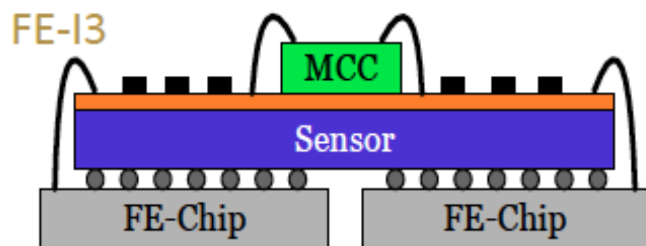
- The goal is to obtain the optimal pitch and thickness of pixel modules for different locations for the ITK.
- How do the pixels performance depend on the angle, irradiation and particle type ?
- The first step is to study the basic quantities for 0° and non-radiated sensors.
- Once we demonstrate we have the tools in place, we can proceed with high eta and radiated modules.
  - For different pitch and thickness sensors

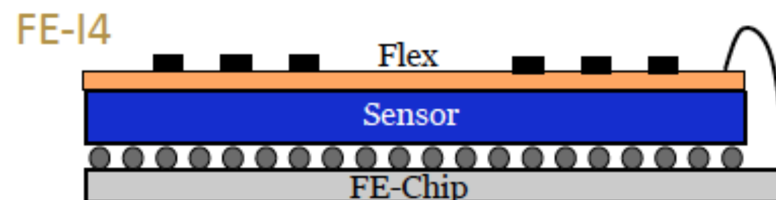
ATLAS FE-I4 chip



FEI4 vs FEI3 specs

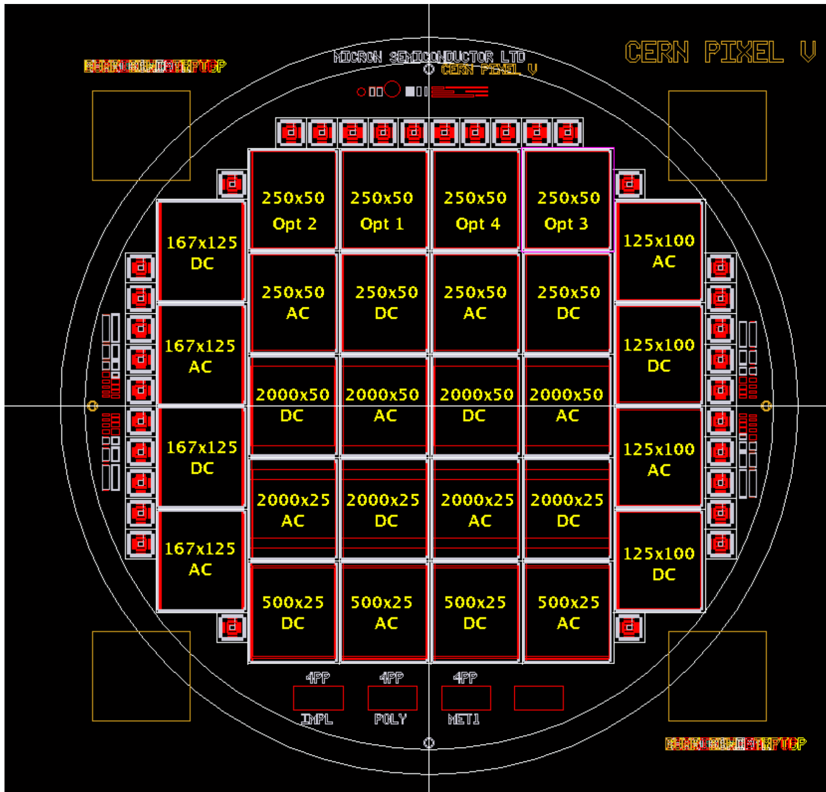
	FEI4	FEI3
Year	2011	2003
Technology	130nm	250nm
Chip Size	$20x19mm^2$	$7.6x10.8mm^2$
Active Area	89%	74%
Array	80x336 =26,880	18x160=2,880
Pixel Size	$50x250\mu m^2$	$50x400\mu m^2$
N Transistors	87M	3.5M
Data Rate	320 Mb/s	40Mb/s
Wafer Yield	60%	80%





UNIVERSITY OF LIVERPOOL

Liverpool CERN PIXEL V design



In production at Micron:

Segmentation:

- 125x100 µm (square)
- 167x125 µm (square)
- 250x50 µm (Standard)
- 500x25 µm (elongated)
- 2000x25 µm (strixel)
- 2000x50 µm (strixel)

Features both AC and DC power, polysilicon/ PTB

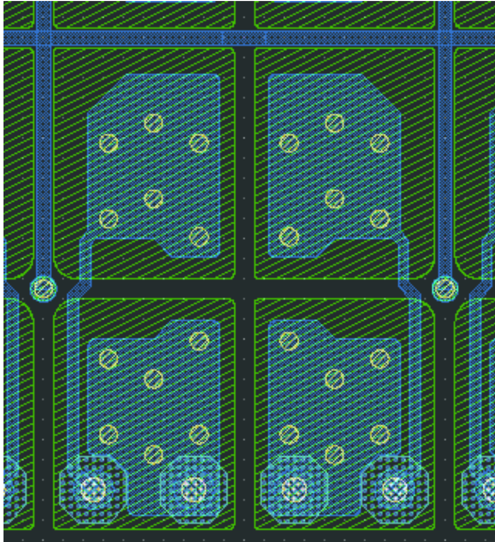
Production will be on 300, 200, 150, 100µm

DC only wafers already produced and made into working modules.

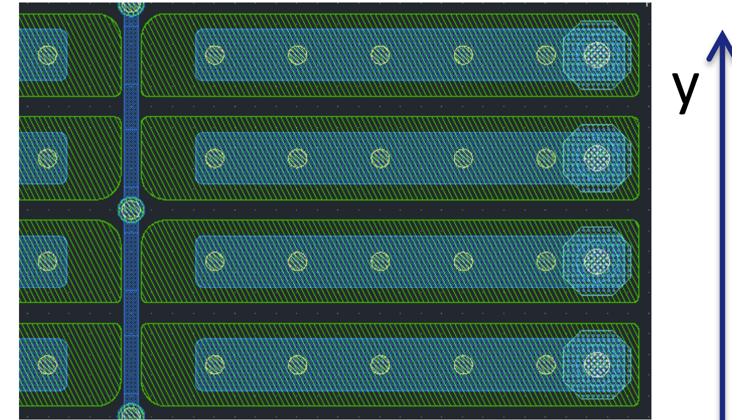
Fully finished AC/DC wafers across 4,10 and 13kΩ resistivity wafers expected mid to end of September, assembly production in weeks following

CERN PIXEL V – alternative geometries

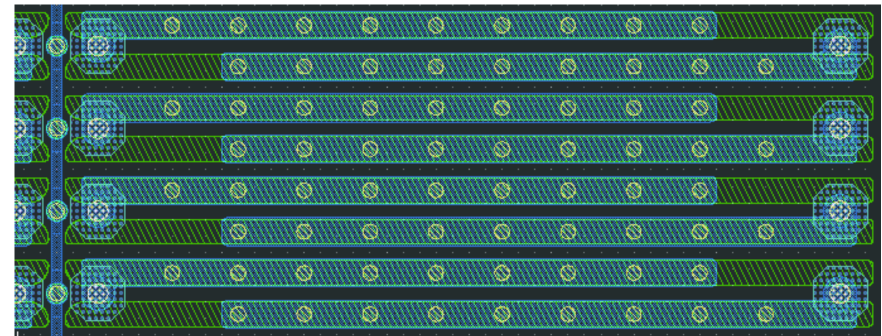
125x100 (square)



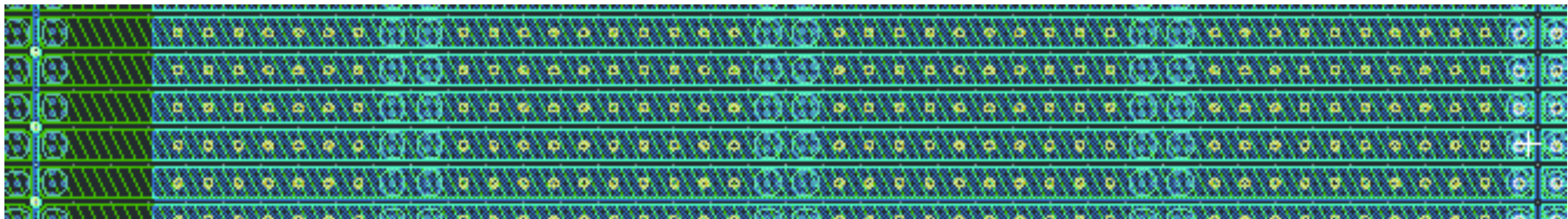
250x50 (VTT5)



500x25 (VTT10)



2000x50 (strixel)



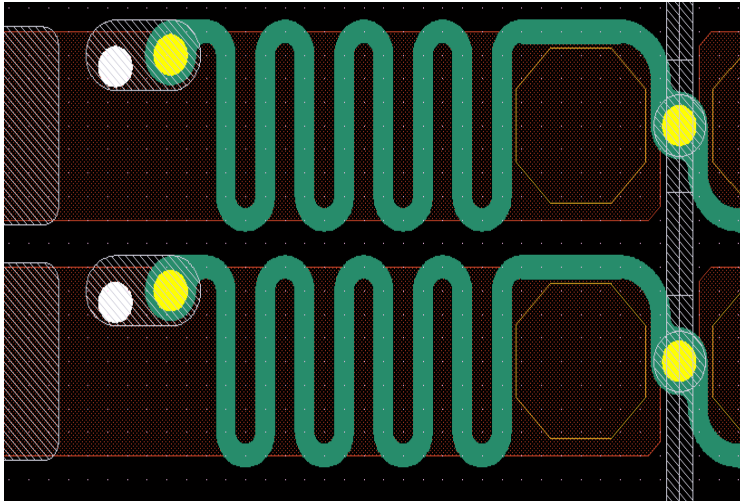
y

x

CERN PIXEL V – sensor powering

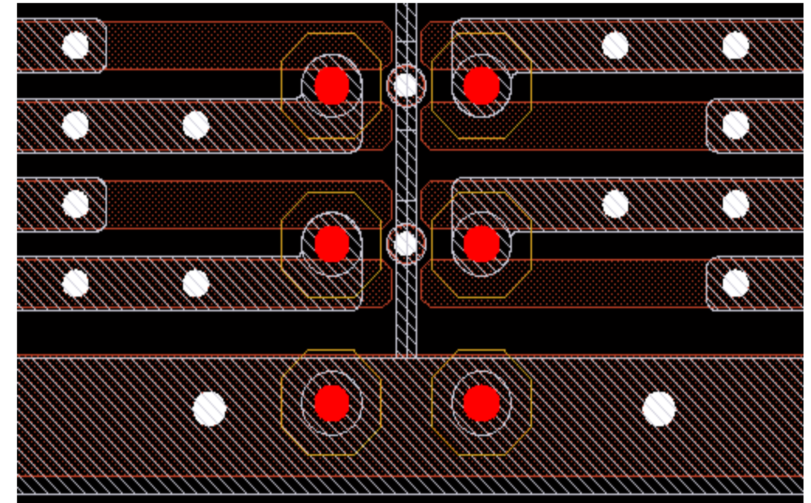
AC-coupling

All polysilicon bias resistors are ~100 squares long -> 300 kOhm



DC-coupling

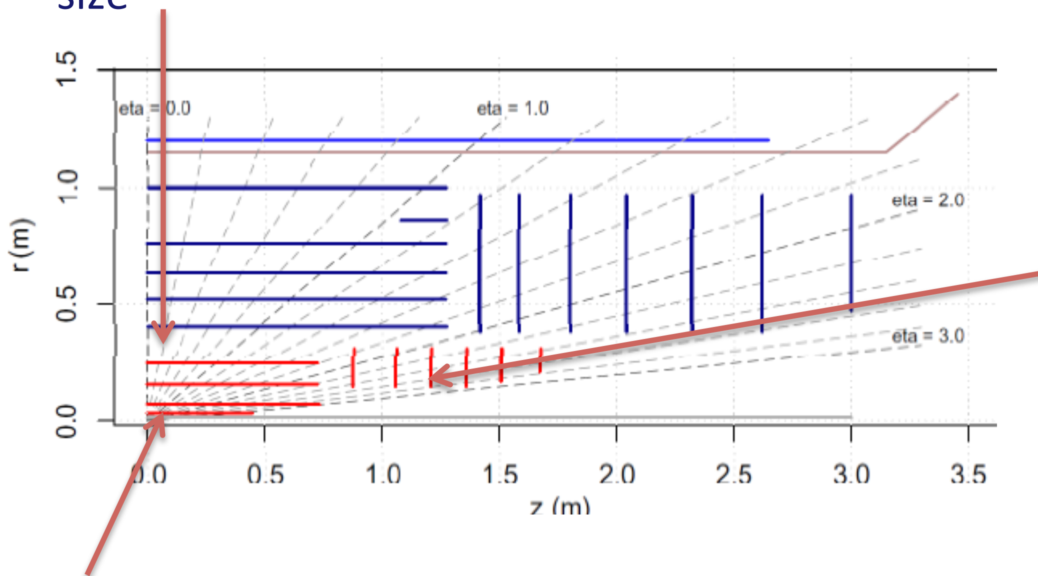
Each group of 4 pixels share one punch-through biasing dot



AC and DC coupled sensors are shuffled for the homogeneous etching of polysilicon ("minimum area coverage" DRC requirement)

Why study different pixel sizes?

Outer Barrel layers:
250x50 current baseline for outer barrel layers
Investigate using 500x25 device for outer barrel layers at high eta to reduce the cluster size



Pixel Endcap:
Investigate square modules for endcap (125x100 and 167x125)

Using the 167x125 would require turning off some channels

- less power/cooling

Inner barrel layer:
Plan to use FEI5 chip: 125x25. In order to study the pitch in x and y, we can study **125**x100 and 500x**25**

Why the different pixel sizes?

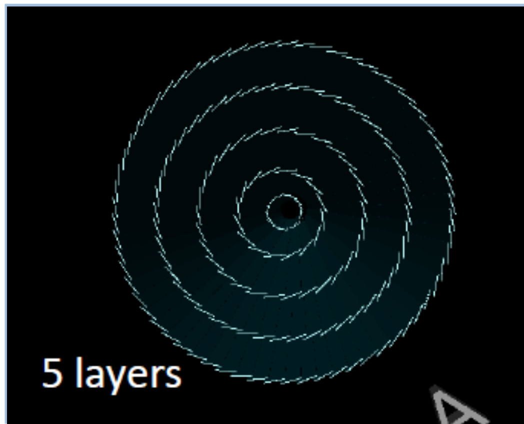
Alternative Tracker Geometries

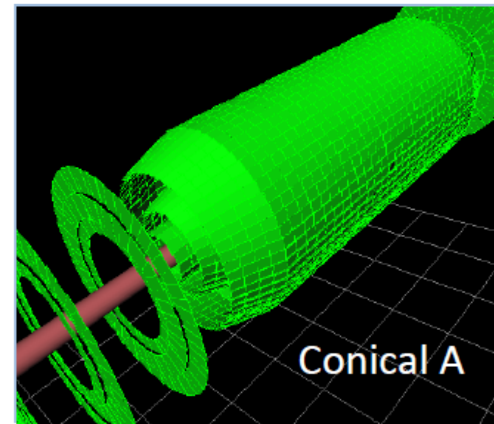
The layout for the ITK is still being optimised, alternative layouts are being discussed (e.g. 5 pixel layers, conical layouts.

5th Pixel Layer

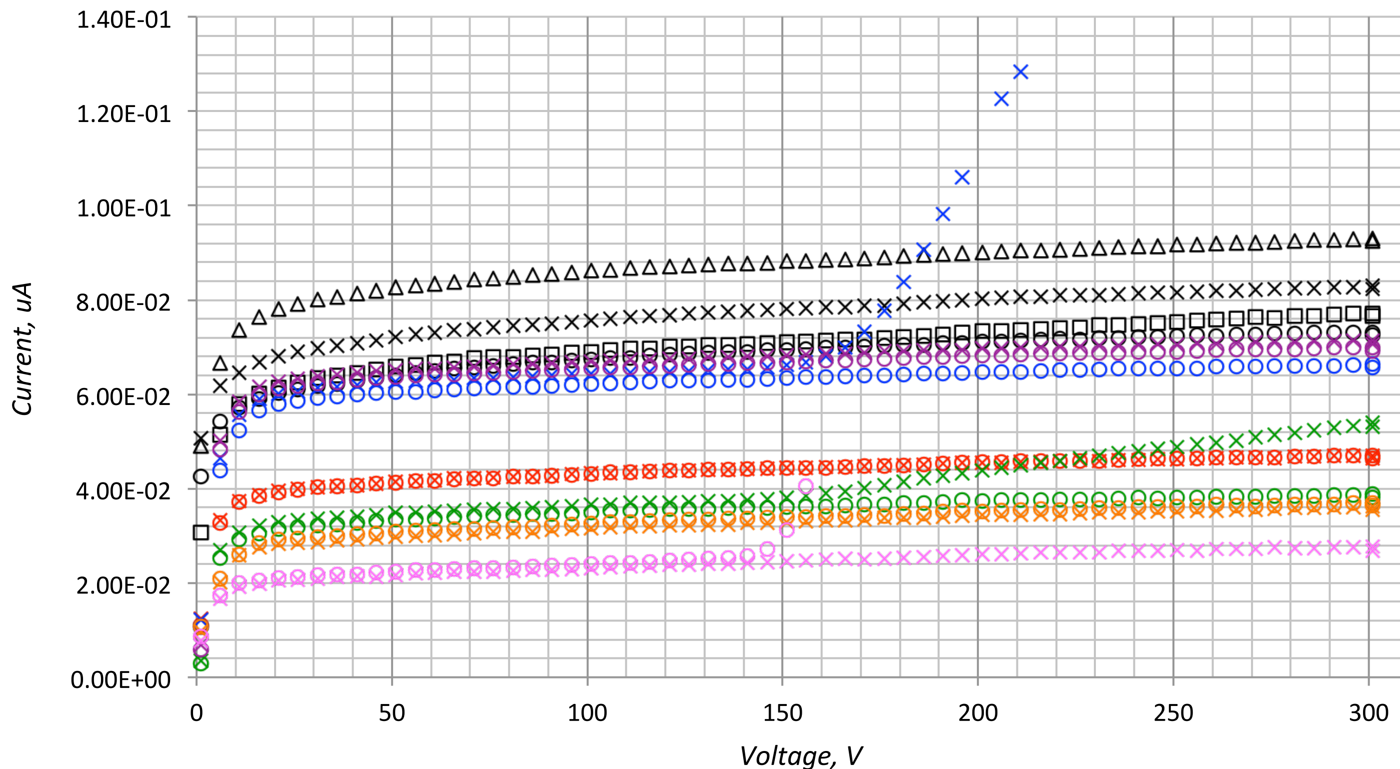
Investigate strixels (2000x25 and 2000x50): These should have better resolution than silicon strips.

These will again be dependent on switching off readout channels -> reduced power.





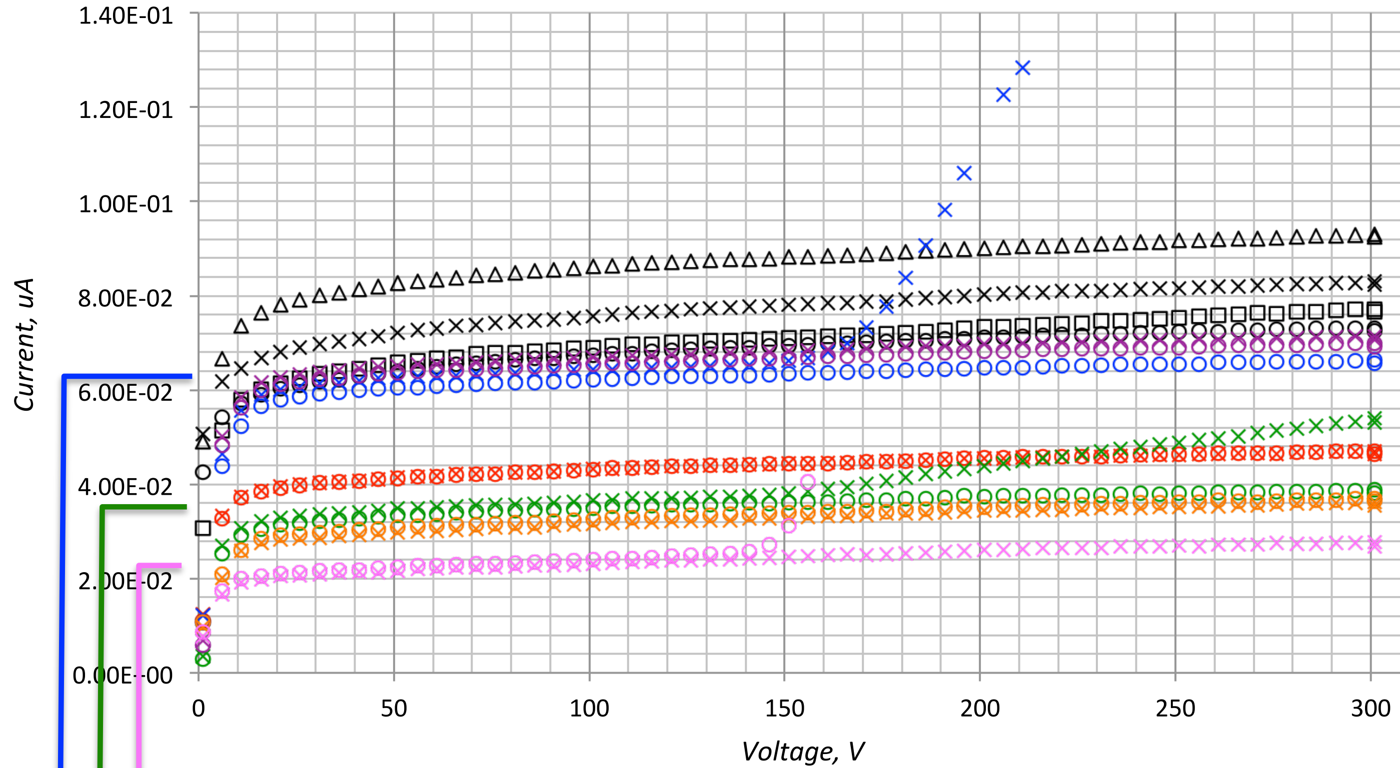
Alternate Geometry IV Characteristics



Standard operating voltage is 150V

Devices bias up to 500V before Breakdown typically occurs (Not shown here)

Alternate Geometry IV Characteristics



UNIVERSITY OF LIVERPOOL

- CP5-3072-3-300UM-OPT1
- CP5-3072-3-300UM-OPT2
- CP5-3072-3-300UM-OPT3
- CP5-3072-3-300UM-OPT4
- CP5-3072-3-300UM-250x50DC1
- CP5-3072-3-300UM-250x50DC2
- CP5-3072-3-300UM-500x25DC1
- CP5-3072-3-300UM-500x25DC2
- CP5-3072-3-300UM-2000x50DC1
- CP5-3072-3-300UM-2000x50DC2
- CP5-3072-3-300UM-2000x25DC1
- CP5-3072-3-300UM-2000x25DC2
- CP5-3072-3-300UM-125x100DC1
- CP5-3072-3-300UM-125x100DC2
- CP5-3072-3-300UM-167x125DC1
- CP5-3072-3-300UM-167x125DC2

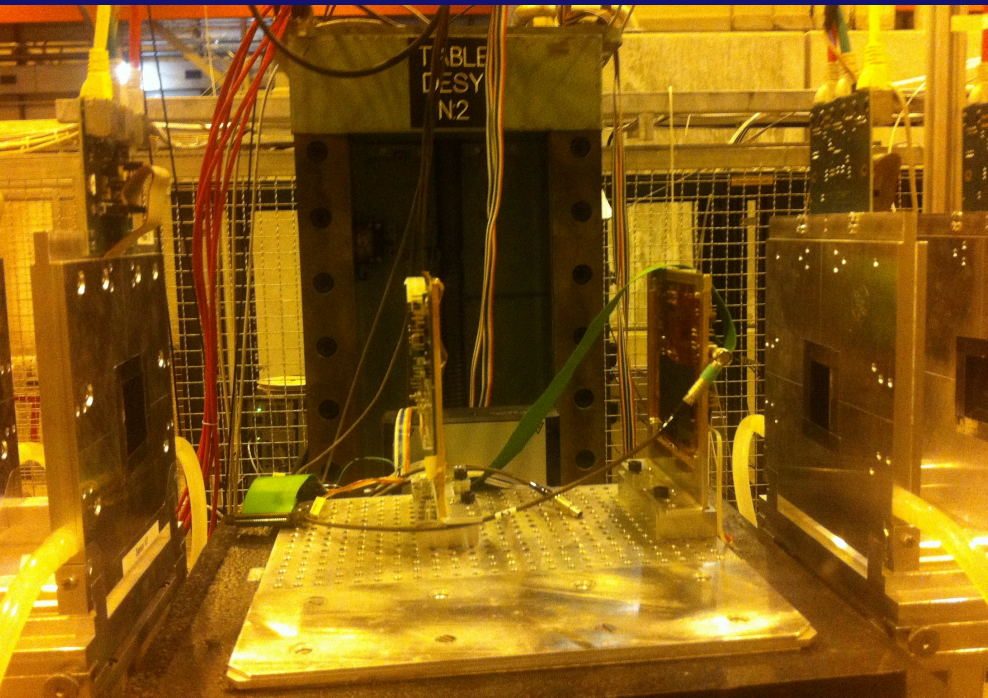
Square devices

Devices with 50µm pitch in Y

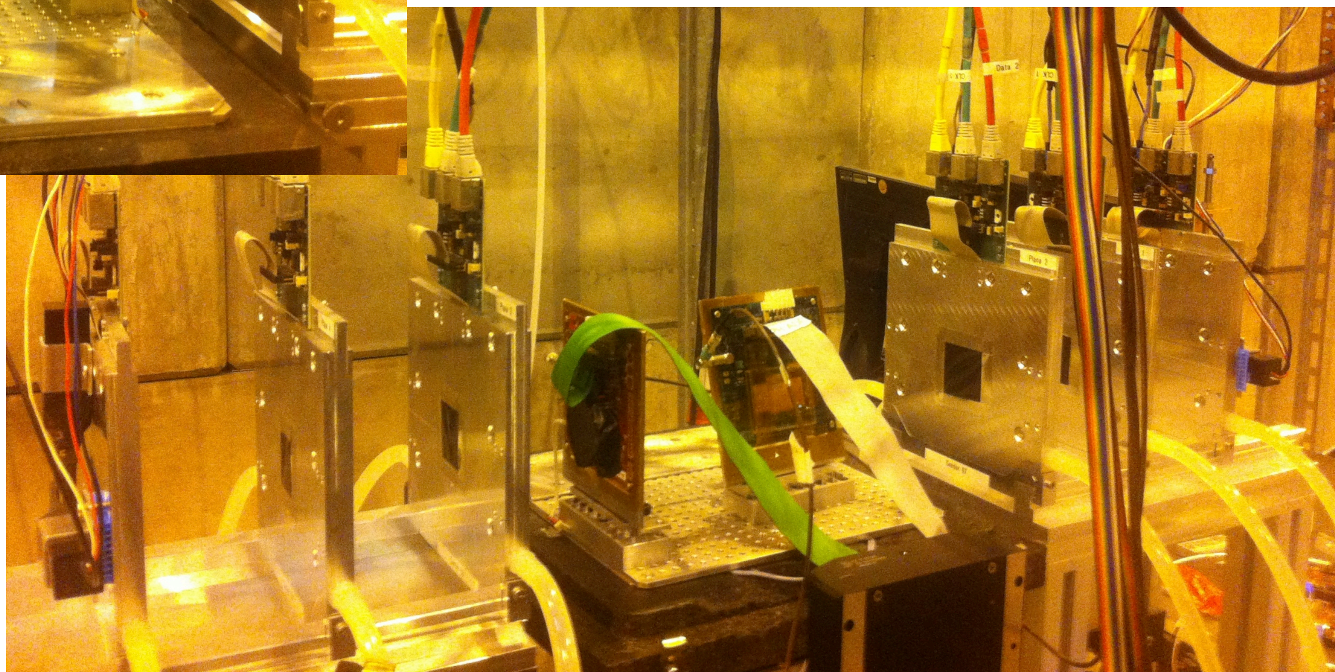
Devices with 25µm pitch in Y

Local Density of PTB dominates base leakage current, not the total number of PTB's

ACONITE telescope @ CERN SPS

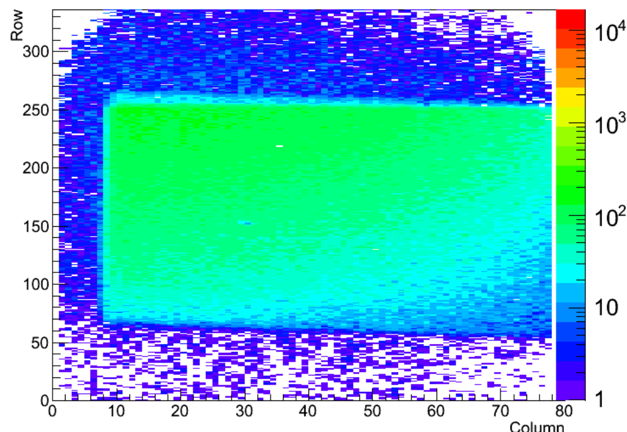


Pixels tested using 120GeV pions
6 MAPS sensors
2 Device Under Test (DUT)

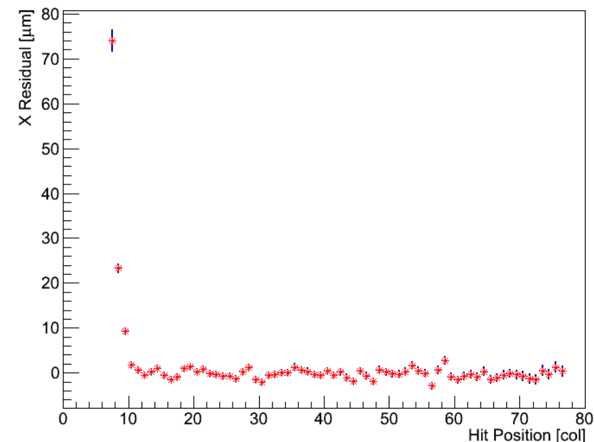


250x50 (VTT5) – 3200e – basic plots

VTT5 Hitmap – all



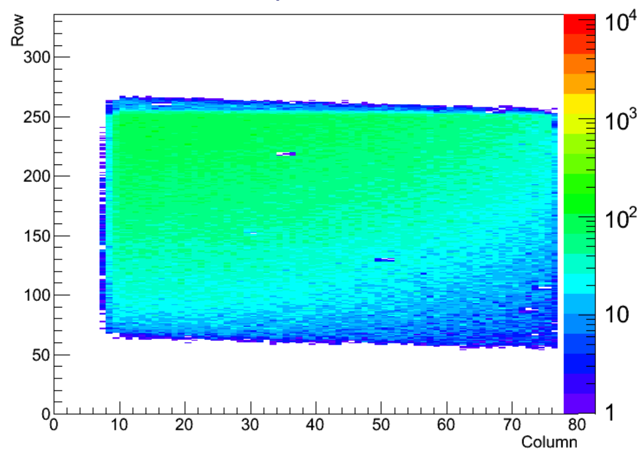
Hit position X vs Residual X



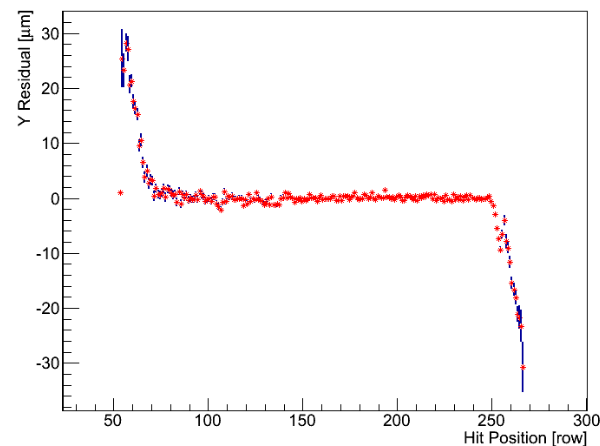
Residual vs Hit position are bad at outer region of matched track hitmap – due to limited scintillator size

-> Use only central region for performance studies

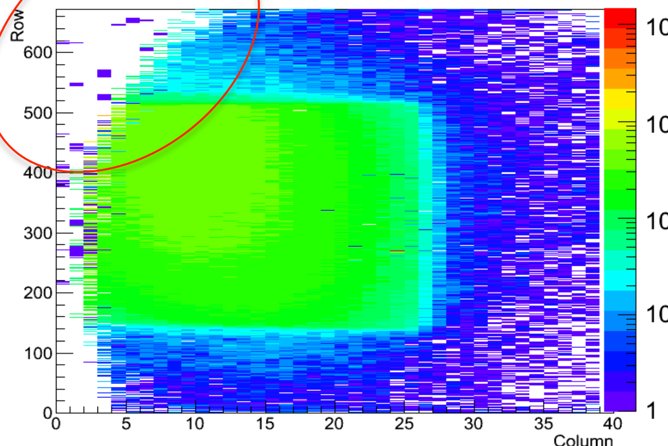
VTT5 Hitmap – matched tracks



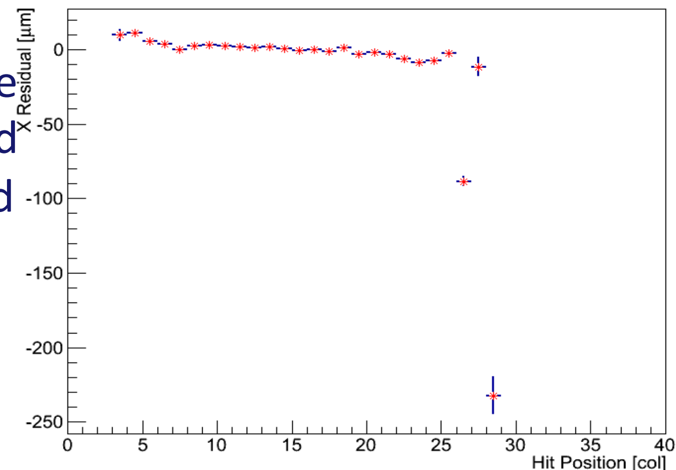
Hit position Y vs Residual Y

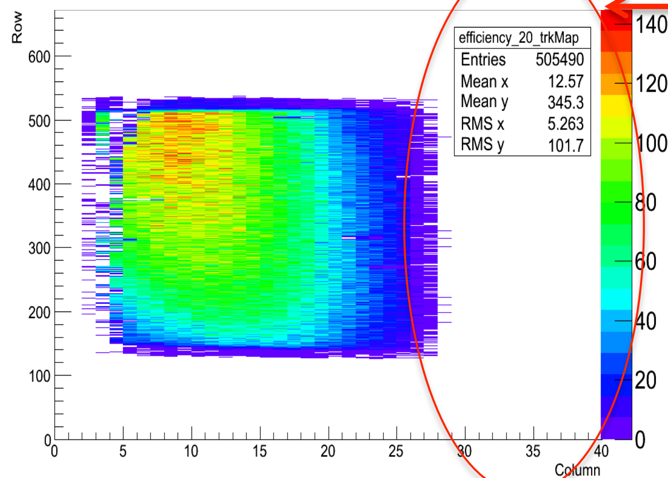


500x25(VTT10) – 3200e – basic plots

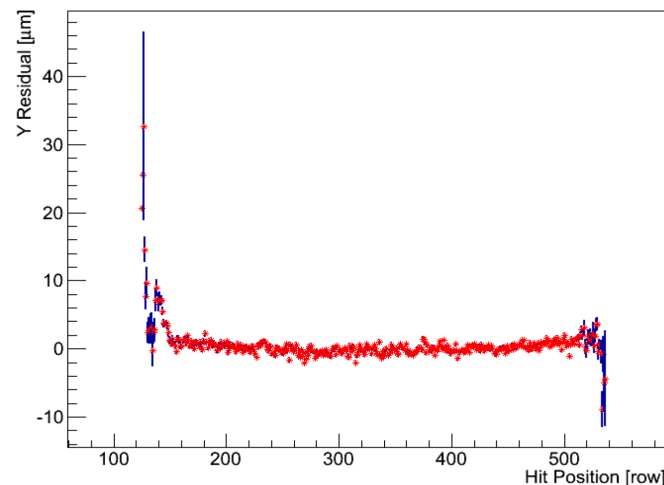


In this area, the readout chip is disconnected from the sensor pixels. Thinned readout chip was used during bump bonding to sensor - heat used (~300deg) caused the read out chip to bow.



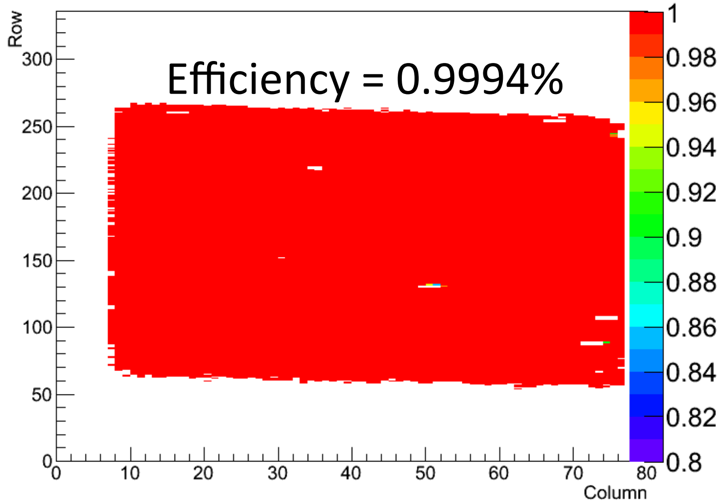


Alignment issues meant the device was not fully in the beam

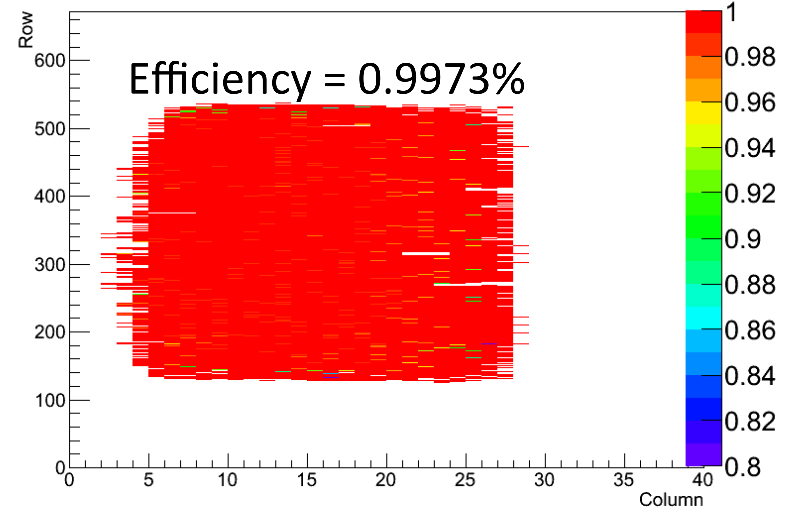


Sensor Efficiency - 250x50 (VTT5) vs 500x25(VTT10)

VTT5 3200e



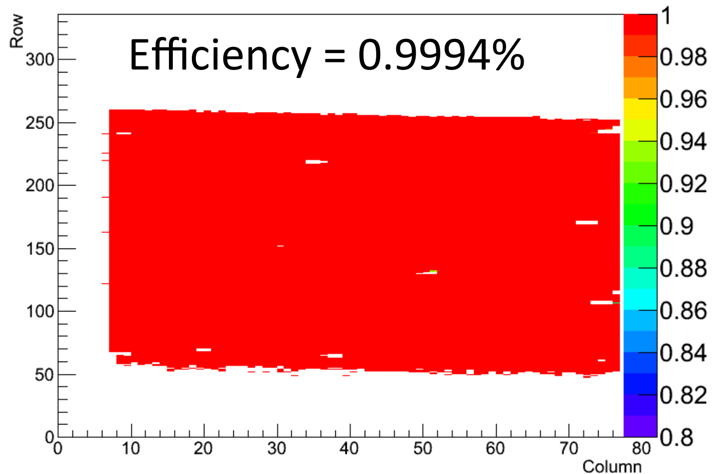
VTT10 3200e



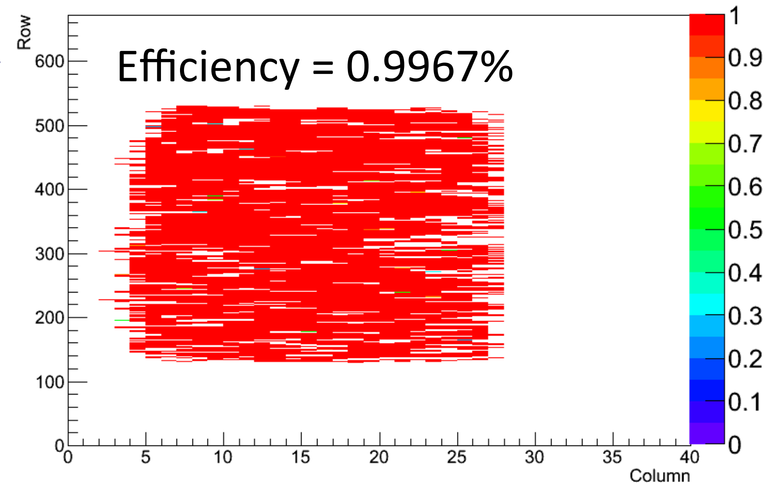
VTT10 show same high efficiency performance as VTT5

(small degradation due to quality of tuning).

VTT5 1600e



VTT10 1600e

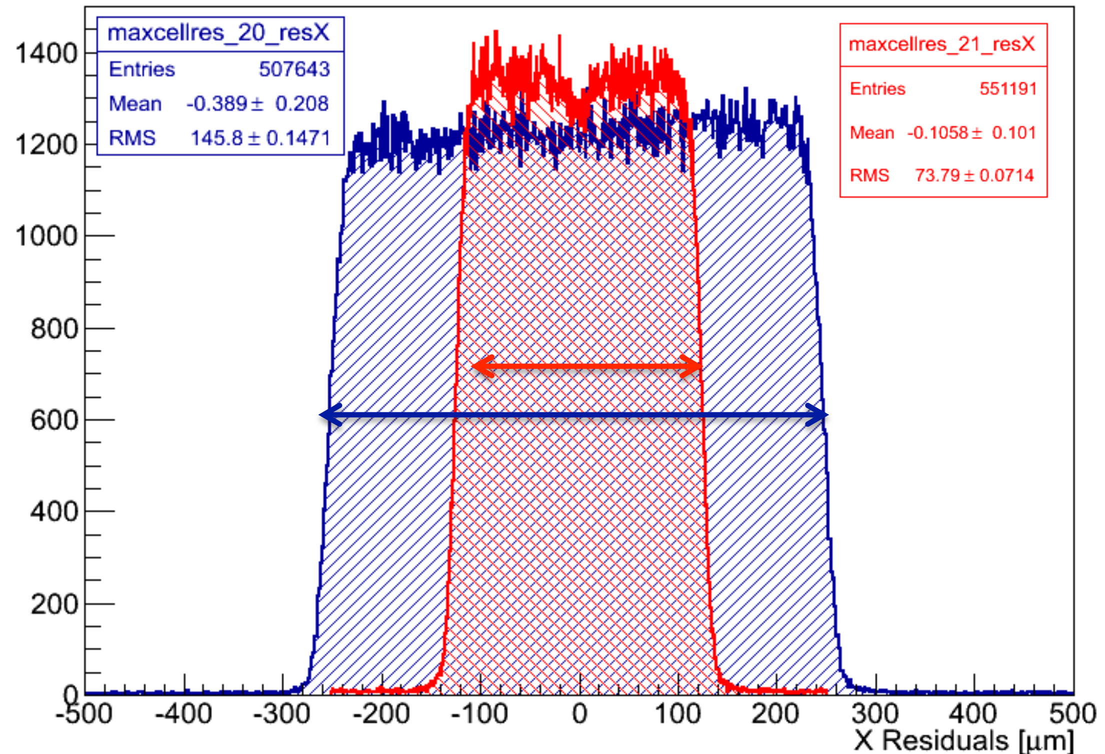


Residual X and resolution – 250x50 vs 500x25

RMS values are approximately what is expected for pitch/root(12):

500x25 : $500/\sqrt{12} = 144.3\mu m$
250x50 : $250/\sqrt{12} = 72.17\mu m$

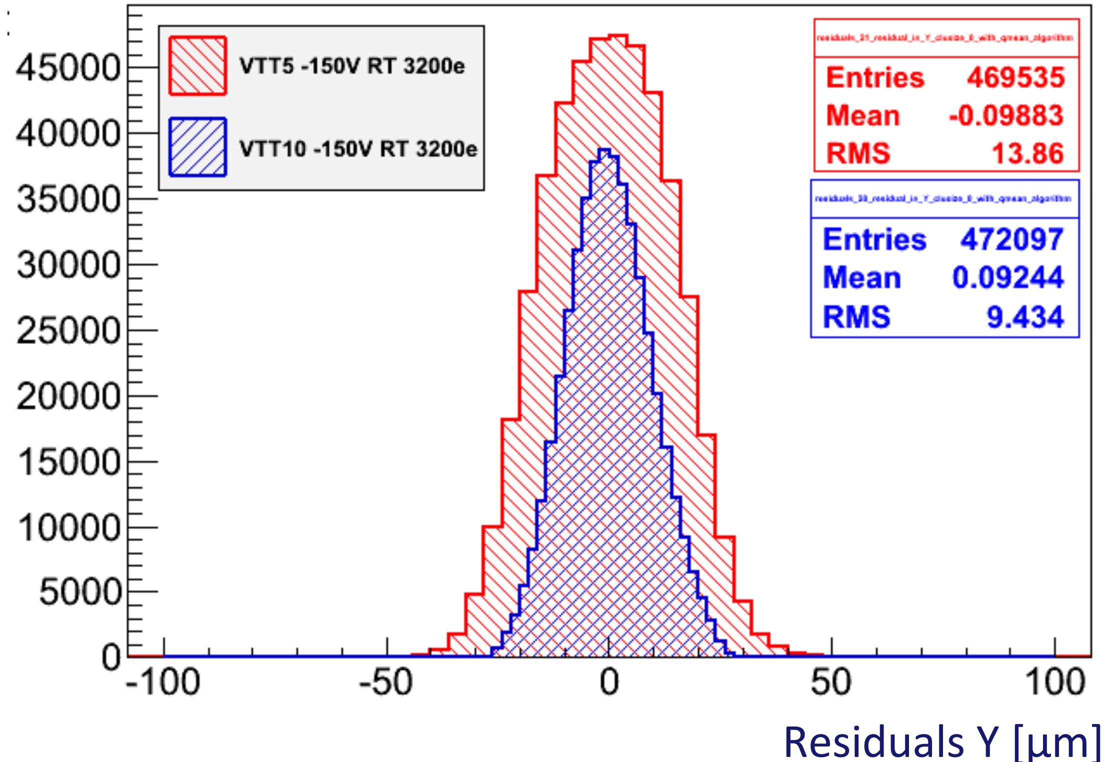
Width of distribution (half way up) should be 500 for 500x25 and about 250 for 250x50



Residual Y and resolution – 250x50 vs 500x25

RMS values are approximately what is expected for pitch/root(12)

500x25 : $25/\sqrt{12} = 7.217\mu m$
250x50 : $50/\sqrt{12} = 14.43\mu m$

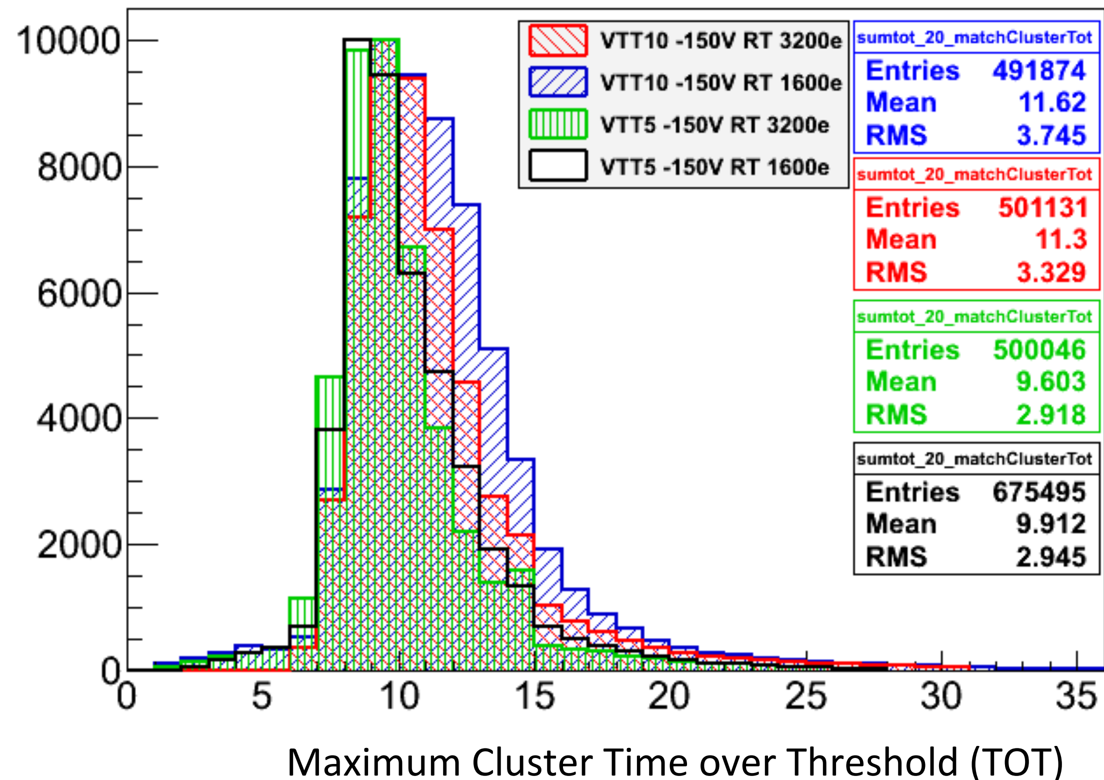


Device total Matched Cluster ToT

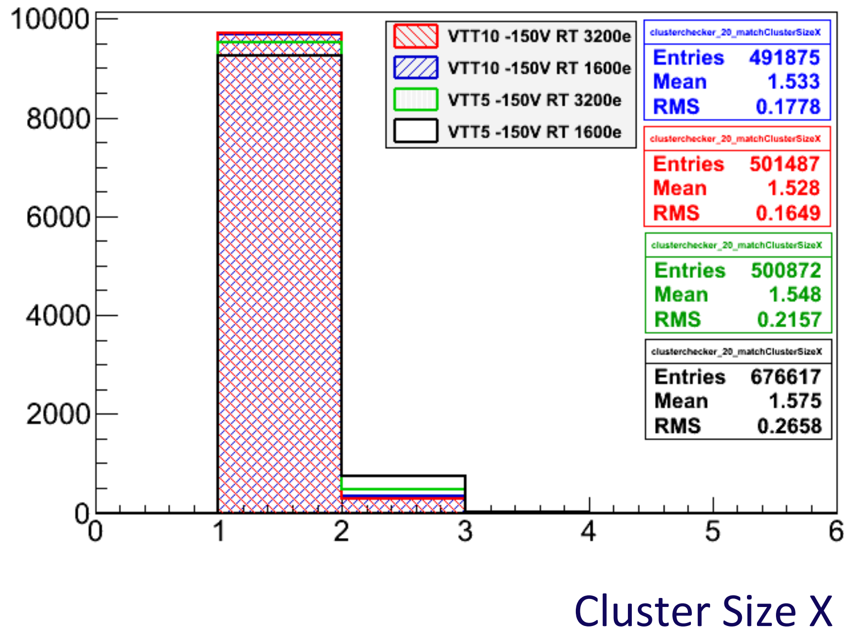
All device tunings are set for 10 ToT = 20ke

No real difference seen between different thresholds of the same device (500x25 and 250x50)

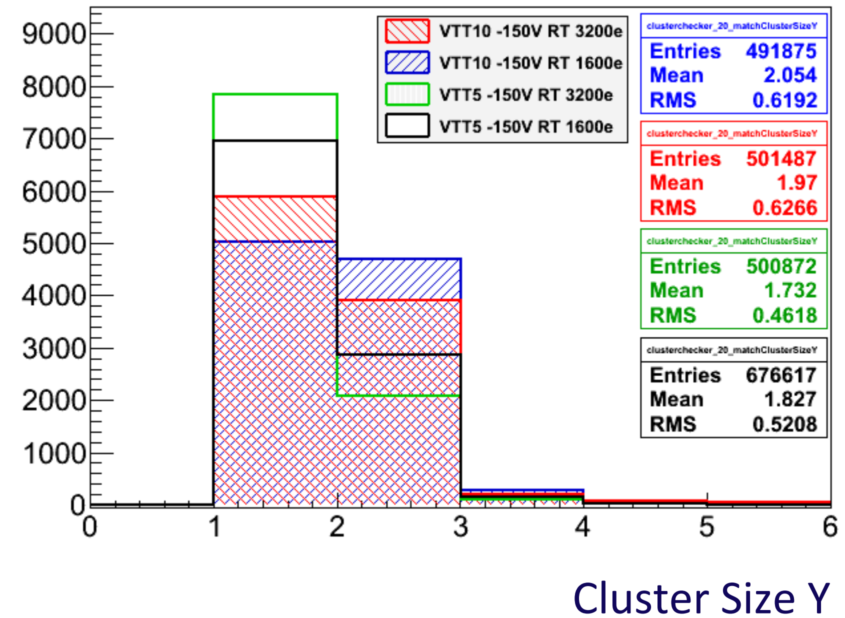
There is a slight difference between the tunings of the 500x25 and 50x250 devices



Device total Matched Cluster Sizes



Cluster Size X



Cluster Size Y

As expected :

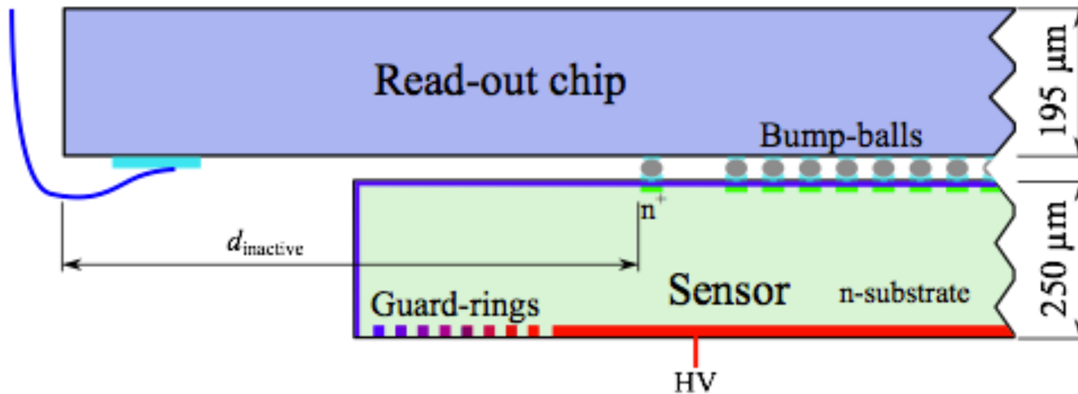
- greater number of 2 hit clusters along Y in 500x25(VTT10)
  - Increased charge sharing
- Minimal change in cluster size in x-direction
  - (500x25 cluster size is slightly more skewed to 1 than 250x50(VTT5))

Summary

- We are studying different pixel geometries that could be part of the ATLAS ITK
- We are starting with basic measurements at 0degrees, for unradiated 25x500μm^2 modules
  - The CERN pixel V has improved electrical characteristics
  - Basic characteristics such as efficiency and residuals are looking sensible
  - Cluster Size
    - Minimal difference in x
    - Increased charge sharing in y
- We can now progress to studying :
  - Radiated pixel studies
  - High Eta studies
    - Data available, but not yet reconstructed
  - 125x500
    - Data available, but not yet reconstructed
  - AC coupling

UNIVERSITY OF LIVERPOOL

BACKUP

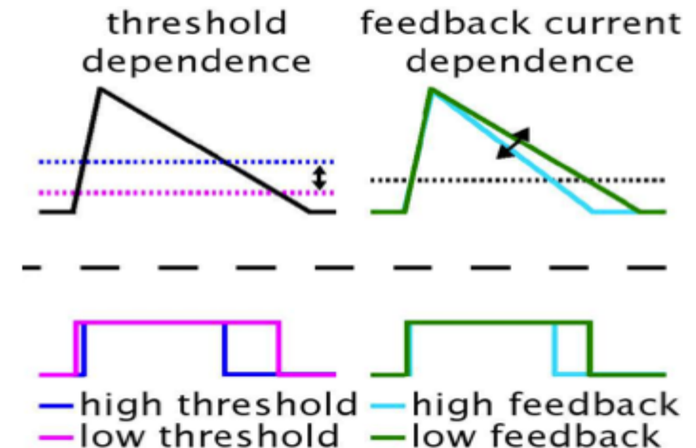


Sensor design

- DOFZ Si n-substrate, 250µm thick
- Read-out chip planar n+-in-n pixels, 400x50µm2
- 16 guard rings on p side to shape HV step
- 1.1 mm inactive edge incl. safety margin

Read-out and interconnection

- FE-I3: 2880 channels
- DC coupled and bump bonding
- Shaper + Amplifier + Discriminator
- ToT ∝ Charge



Choosing a device thickness

Thinner devices retain, a greater fraction of Collected Charge (CC) than thicker devices after irradiation

Graphs show the CC vs received fluence for strip devices at 600V and 1000V

Low threshold operation of FE-I4 enables thin devices to be used.