



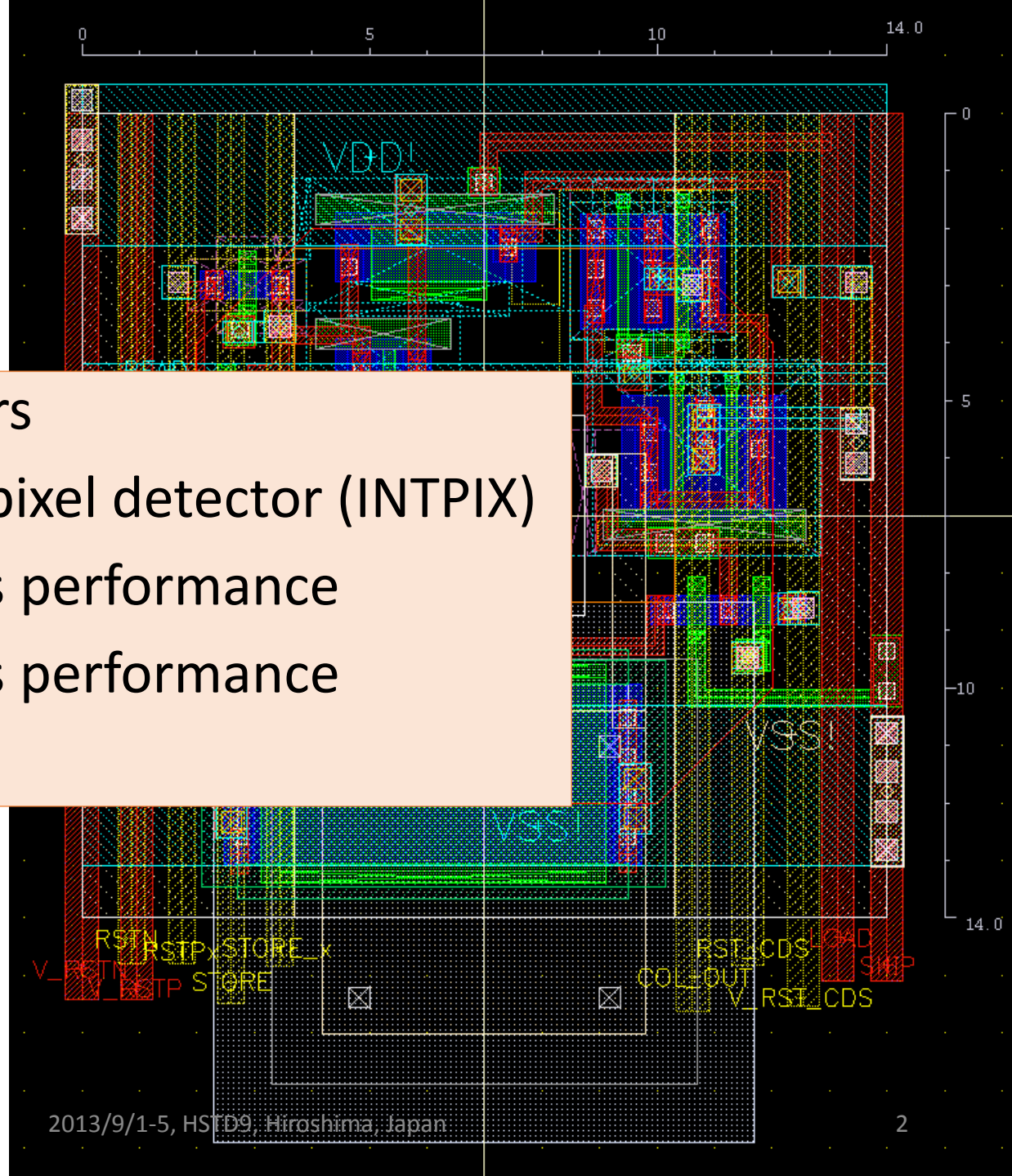
# Development of Silicon-On-Insulator Monolithic Pixel Detectors -FZ SOI sensor-

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**<http://rd.kek.jp/project/soi/>**

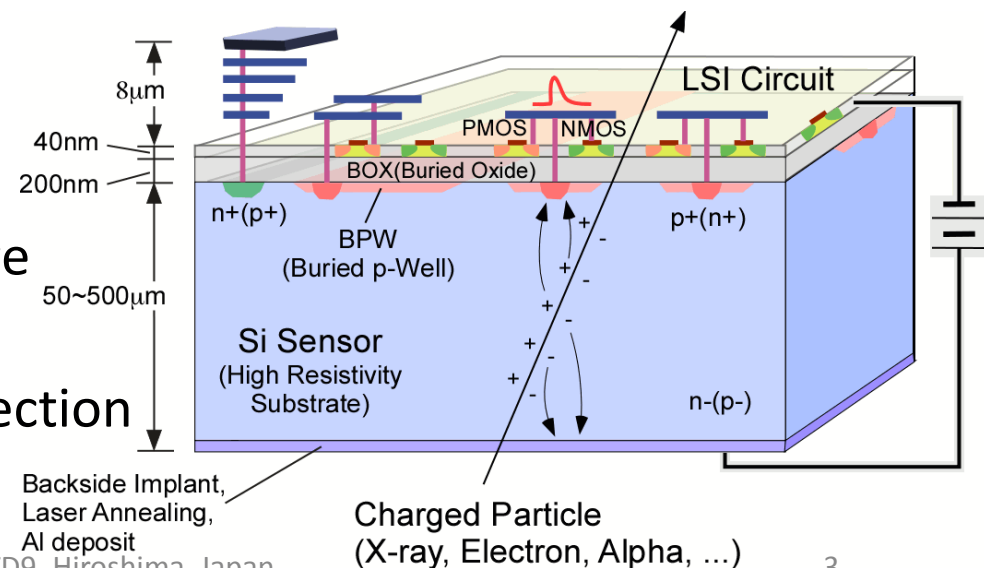
# Outline



- SOI pixel detectors
- Integration type pixel detector (INTPIX)
- Cz INTPIX sensors performance
- FZ INTPIX sensors performance
- summary

# Features of the SOI pixel detectors

- Bonded wafers : Thick High Resistivity Sensor + CMOS
- Monolithic Detector (-> **High circuit density, Low material** )
- Standard CMOS (-> **Complex functions in a pixel** )
- No mechanical bump bonding (-> **High yield, Low cost** )
- Full depleted sensor with small capacitance of the sense node  
( **~10fF, High conversion gain, Low noise** )
- Based on Industrial standard technology  
(-> **Cost benefit and Scalability** )
- No Latch Up, Low SEE  $\sigma$
- Low Power
- Operate in wide temperature range  
( 4 K-570 K ( 300 deg.C ) )
- BPW for the back-gate effect protection



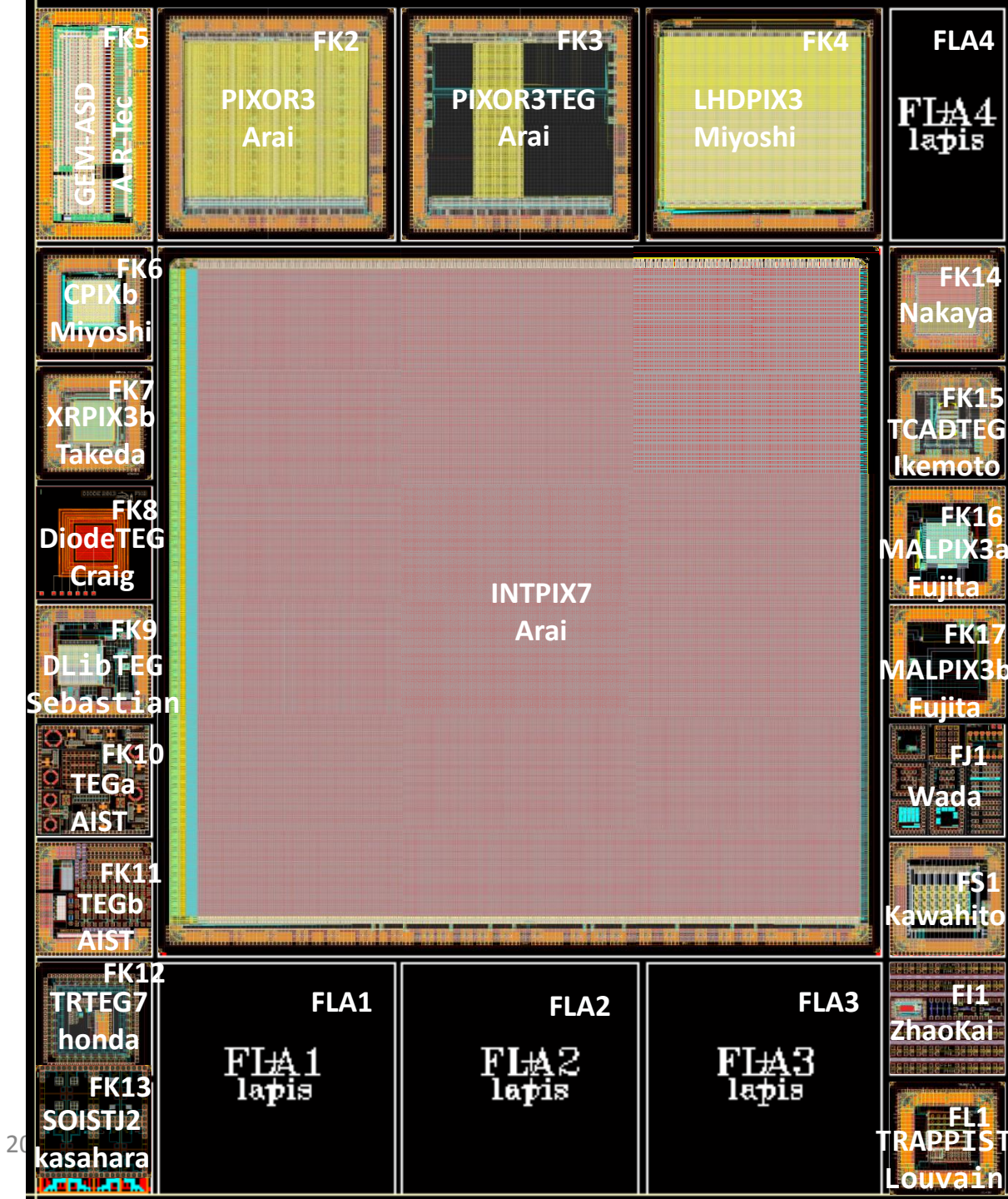
# Lapis Semiconductor\* 0.2 $\mu\text{m}$ FD-SOI Pixel Process

Process	0.2 $\mu\text{m}$ Low-Leakage Fully-Depleted (FD) SOI CMOS 1 Poly, 5 Metal layers (MIM Capacitor and DMOS option) Core (I/O) voltage : 1.8 (3.3) V
SOI wafer (200 mm $\phi$ =8 inch)	Top Si : Cz, $\sim 18 \Omega\text{-cm}$ , p-type, $\sim 40 \text{ nm}$ thick Buried Oxide: 200 nm thick Handle wafer thickness: 725 $\mu\text{m}$ $\rightarrow$ thinned up to $\sim 300\mu\text{m}$ (Lapis) or commercial process $\rightarrow$ $\sim 50 \mu\text{m}$ (then, backside process...) Handle wafer: Cz (N) $\sim 700 \Omega\text{-cm}$ , FZ (N) $> 3\text{k} \Omega\text{-cm}$
Backside process	Mechanical Grind $\rightarrow$ Chemical Etching $\rightarrow$ Back side Implant $\rightarrow$ Laser Annealing $\rightarrow$ Al plating

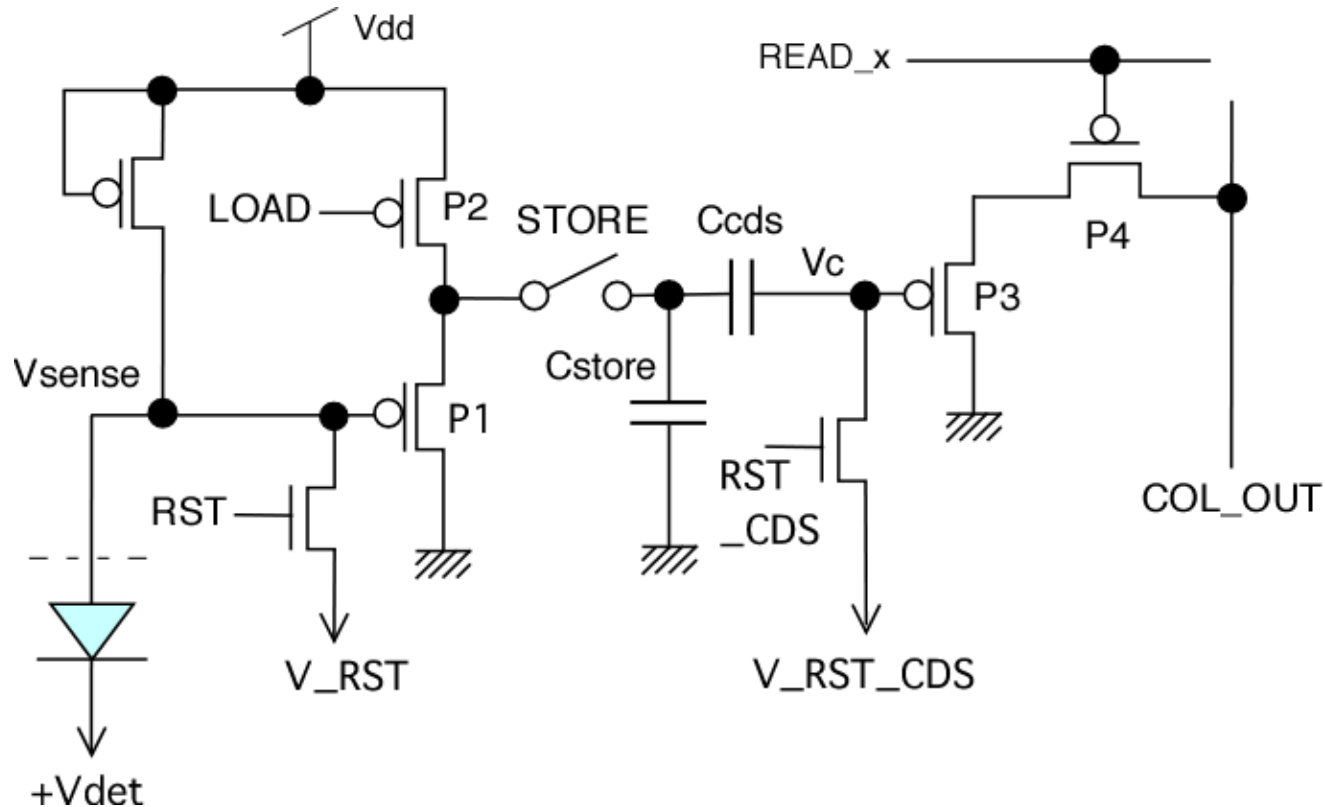
\*former OKI semiconductor

# MPW (Multi Project Wafer)

- mask size:  
 $24.6 \times 30.8 \text{ mm}^2$
- KEK organizes MPW runs  
 ~twice a year.
- Mask is shared to reduce  
 cost of a production.



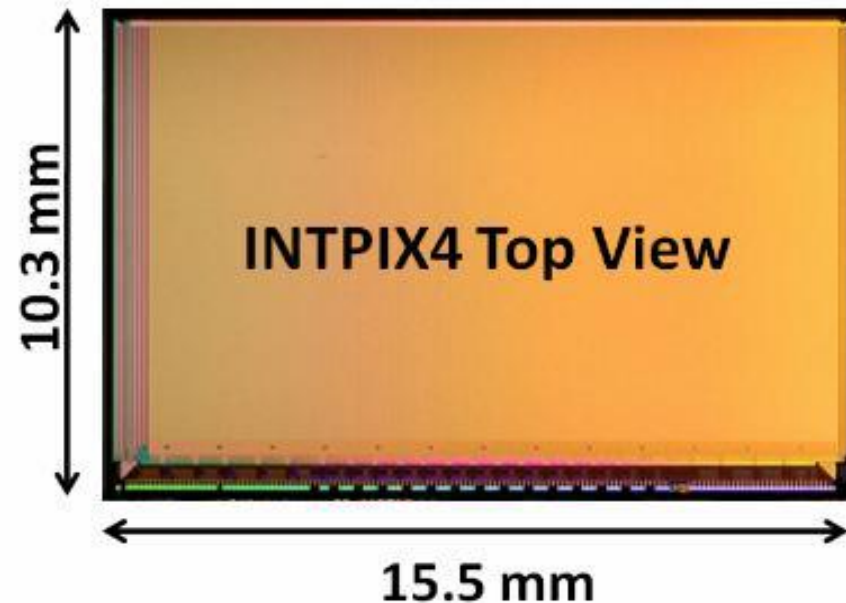
# Integration Type Pixel (INTPIX)



The pixel circuit has CDS function.  
2 Capacitors ( $C_{store}$  and  $C_{cnds}$ )

# INTPIX4

- Integration type SOI pixel detector (mainly for X-ray imaging)
- Chip size : 10.3 x 15.5 mm<sup>2</sup> (Effective area : 8.7 x 14.1 mm<sup>2</sup>)
- Number of pixels : 512 x 832 ( ~426k pixels)
- Pixel size : 17 μm<sup>2</sup>
- Correlated Double Sampling (CDS) Circuit in each pixel
- 13 analog out
- Wafer (n type)
  - Cz: 700 Ω-cm (260 μm thick)
  - FZ: 7k Ω-cm (500 μm thick)
- Front / Back-side illumination

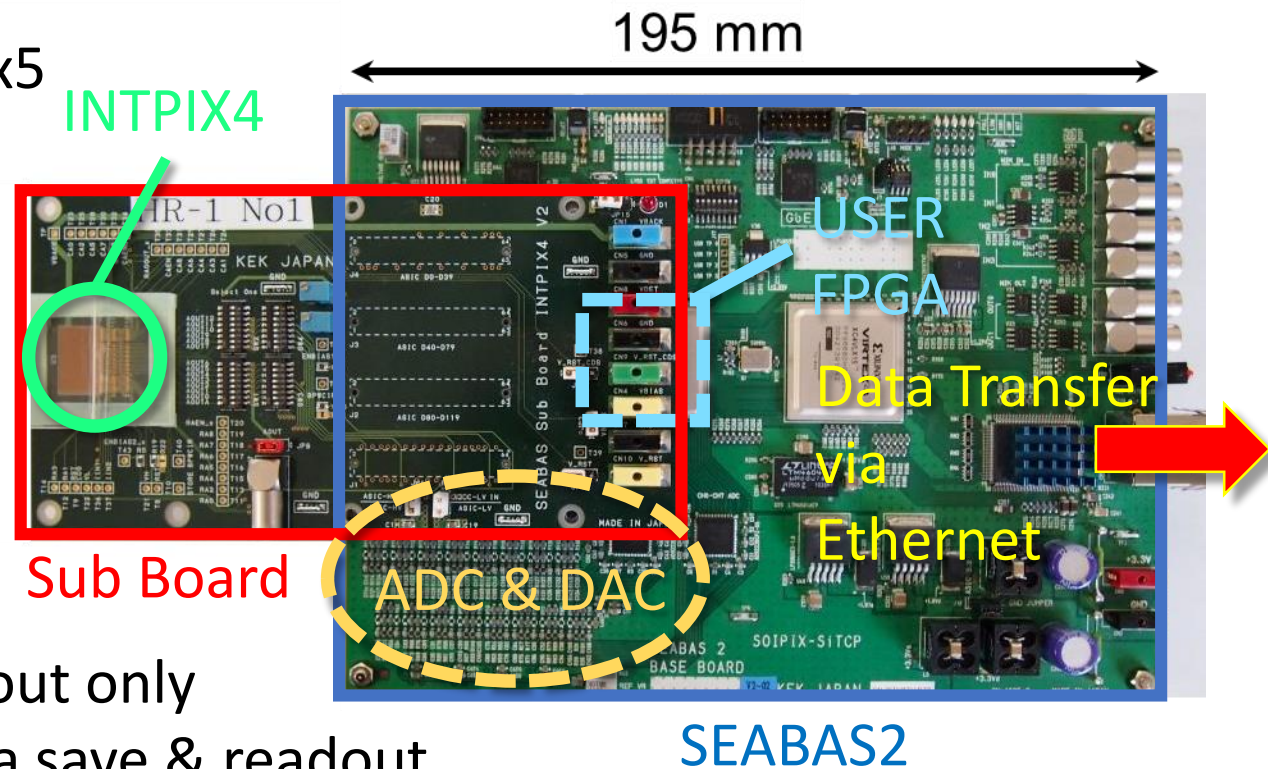


# Evaluation board

- SoI EvAluation BoArd with Sitcp 2 (SEABAS2)
- Gbit Ethernet
- User FPGA Virtex5
- Clock 50 MHz
- +/- 3.3 V
- ADC 16 ch
- DAC 4ch
- NIM I/O

Readout rate

- ~60 fps for readout only
- ~20 fps with data save & readout

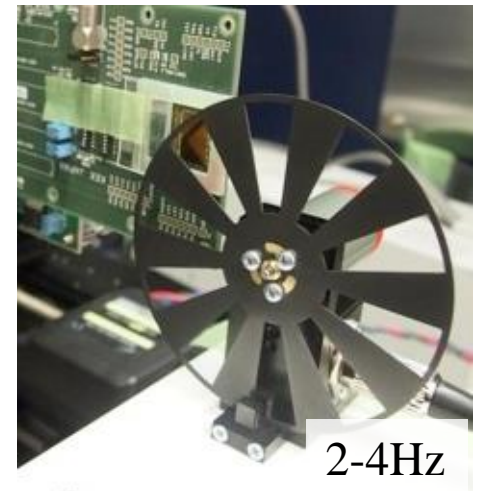
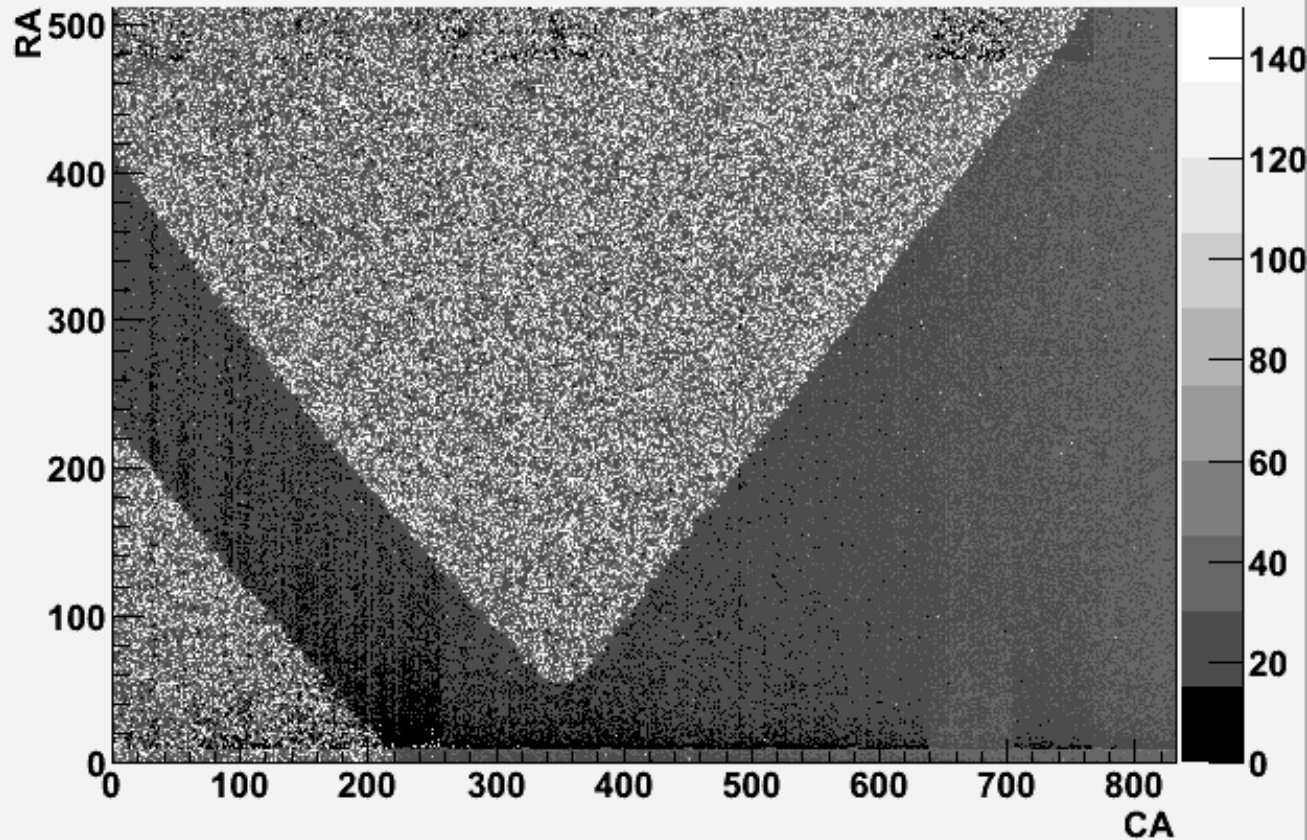




# X-ray movie (Cz)

Optical chopper

INTPIX4 Movie



X-ray tube Mo target  
30kV-40mA

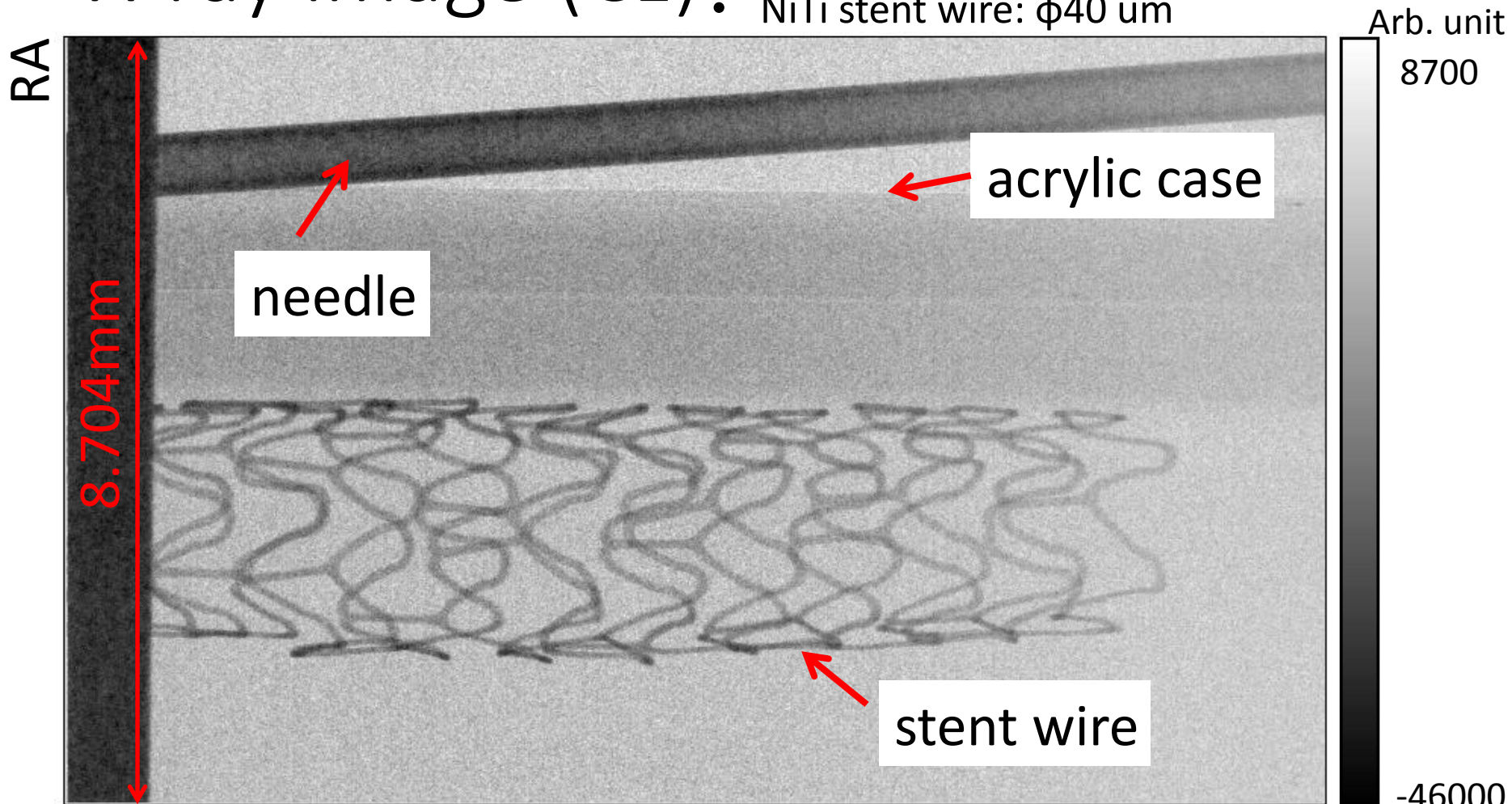
**Frame rate: ~20 fps**

Int. time: 200  $\mu$ s/frame

Back bias: 150 V

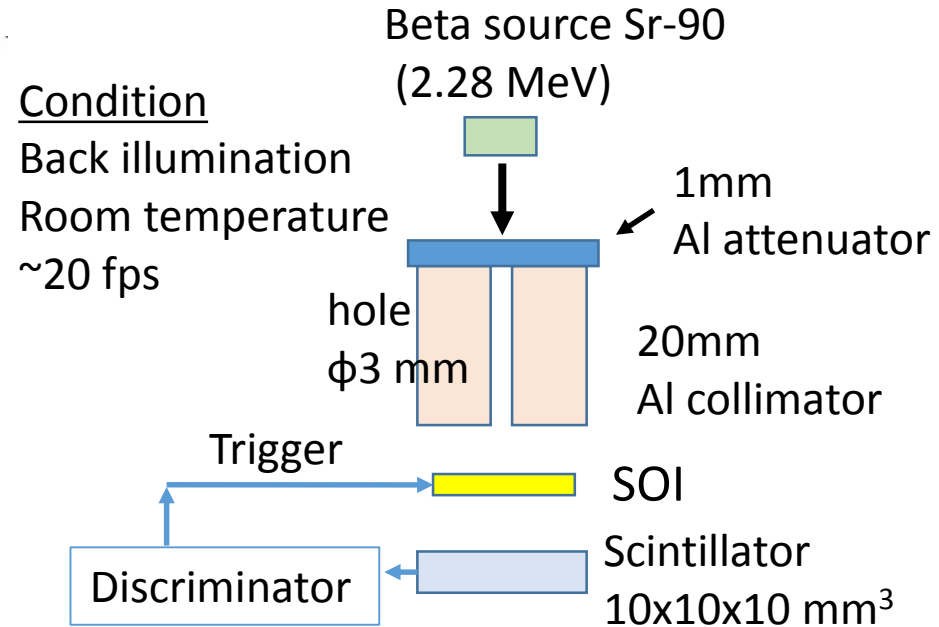
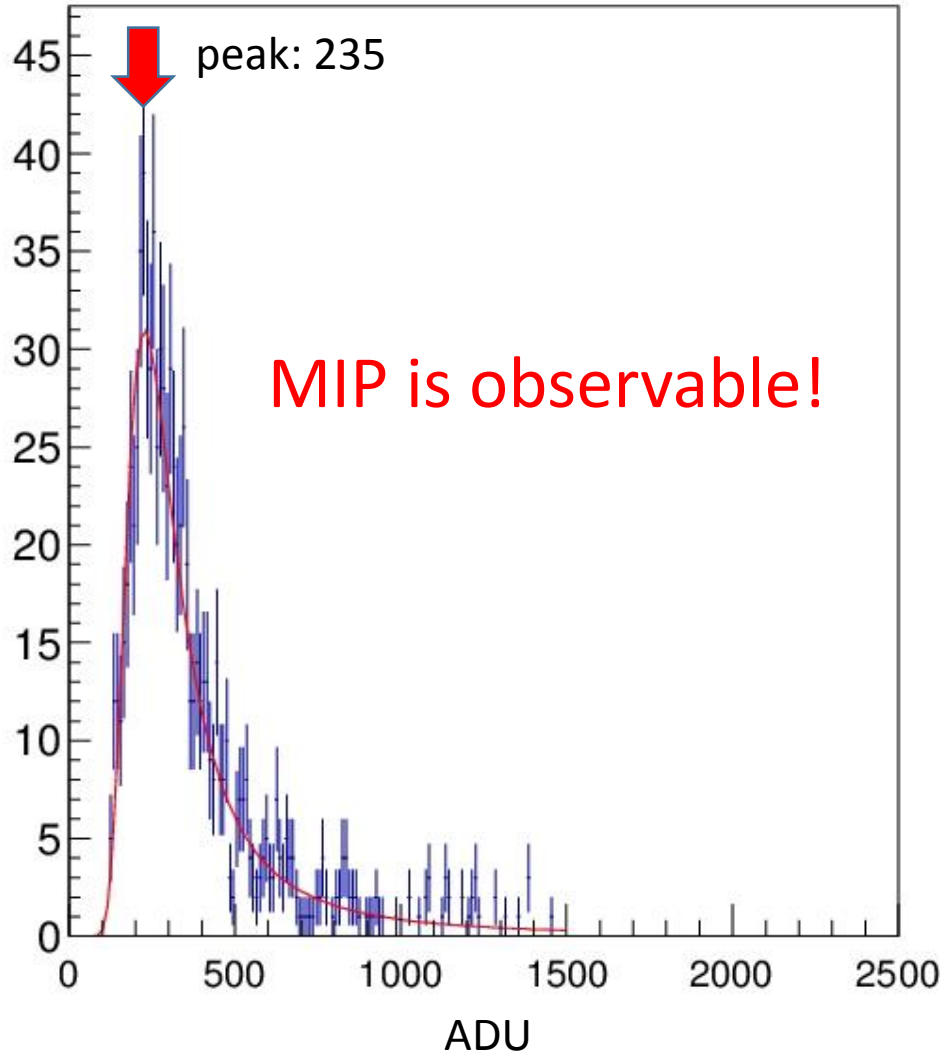
# X-ray image (Cz)

- PF-AR NE7A 33.3keV monochromatic X-ray
- int. time: 200  $\mu$ s x 250 frames
- Total int. time: 50 ms
- NiTi stent wire:  $\phi$ 40  $\mu$ m



difference between [sample image] – [no sample image]

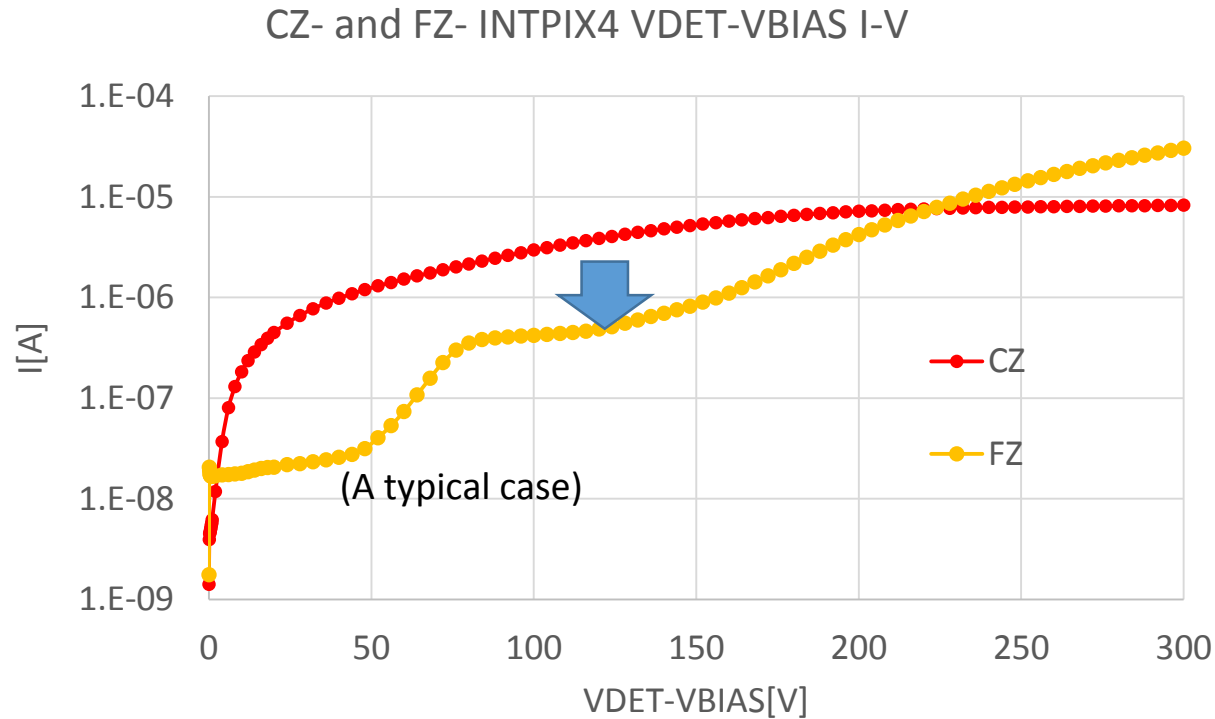
# $^{90}\text{Sr}$ beta source test (Cz)



Sensor thickness: 260  $\mu\text{m}$   
Bias voltage: 100 V  
Depletion width:  $\sim 150$   $\mu\text{m}$   
Int. time: 400  $\mu\text{s}$

Pedestal sigma:  $\sim 13$   
S/N  $\sim 235/13 \sim 18$

# Wafer improvement (Cz->FZ)



Leakage current is lower in FZ SOI sensors.

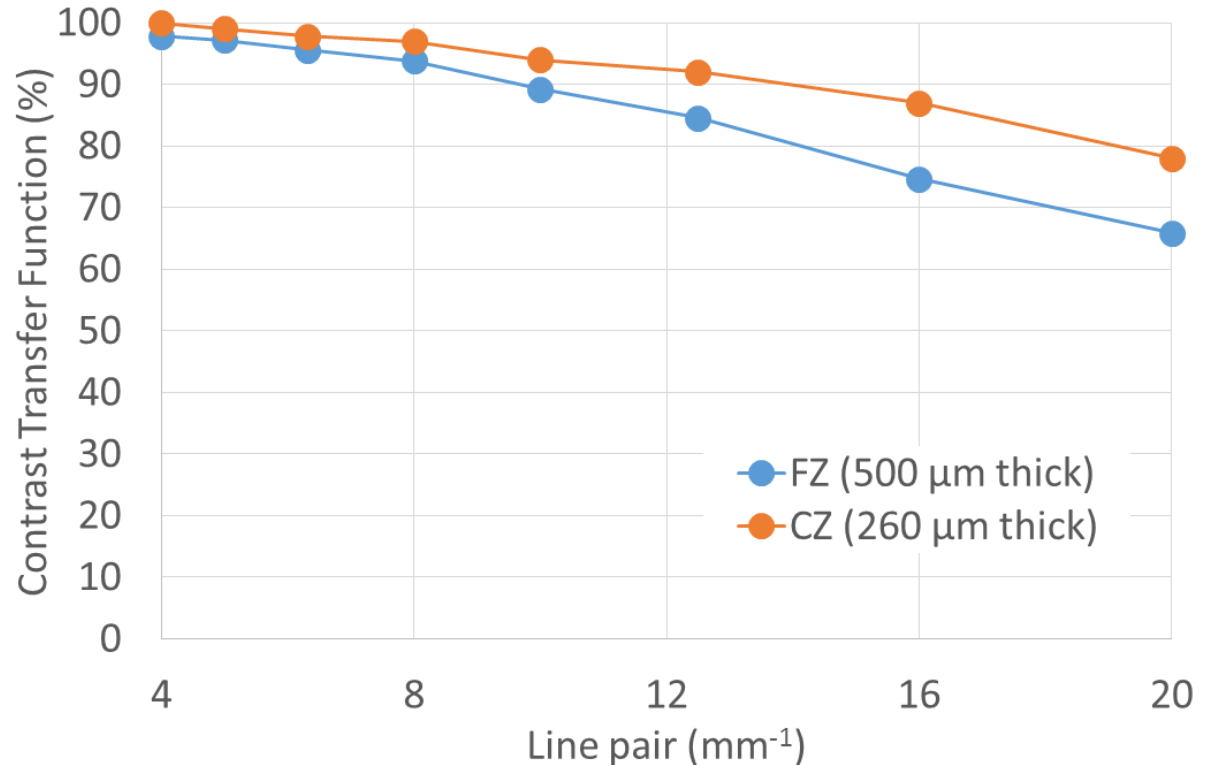
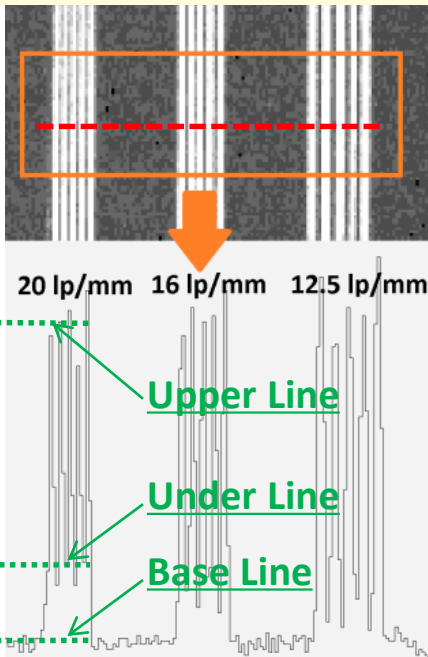
HSTD8 (2011) Cz-INTPIX4 performance study was shown.

**HSTD9 (this conference) FZ-INTPIX4 performance study**

# Spatial resolution (FZ)

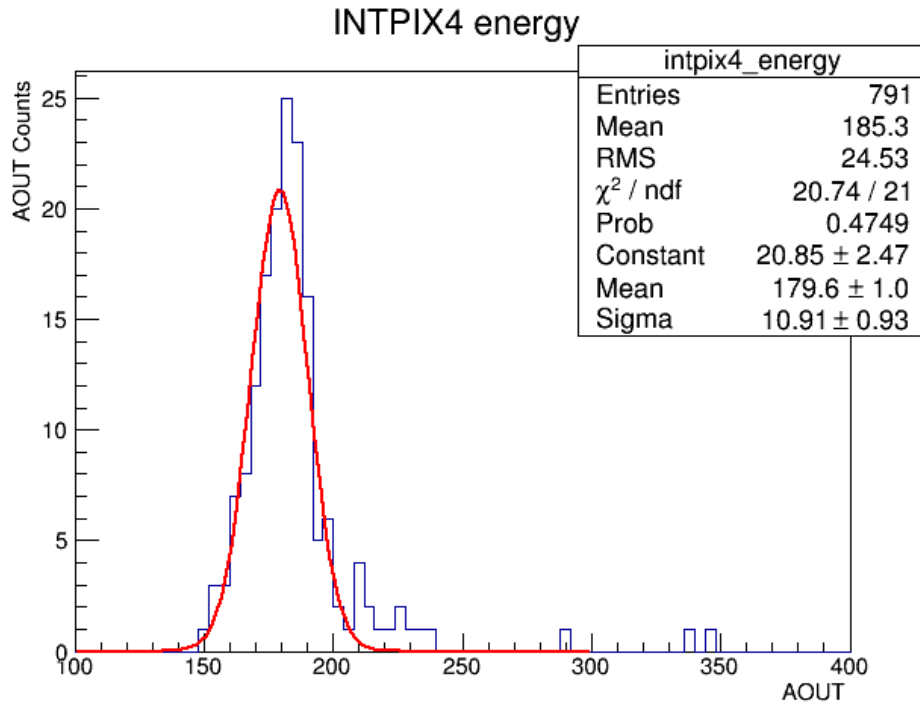
- Evaluation of the spatial resolution by direct radiography in back-side illumination.
- CTF (Contrast Transfer Function) of the FZ N type (500um thick) sensor is a little bit worse than the Cz N type(260um thick) sensor due to it's thicker.
- Both FZ & Cz sensors are showing good CTF!

$$\text{CTF (\%)} = B / A$$



# Energy spectrum (FZ)

$^{109}\text{Cd}$ -Ka (22.2 keV) X-ray spectrum



- Bias voltage = 200 V
- Integration Time = 250  $\mu\text{s}$
- Back-side illumination
- temperature: 0 deg.C
- Single pixel hits are only selected

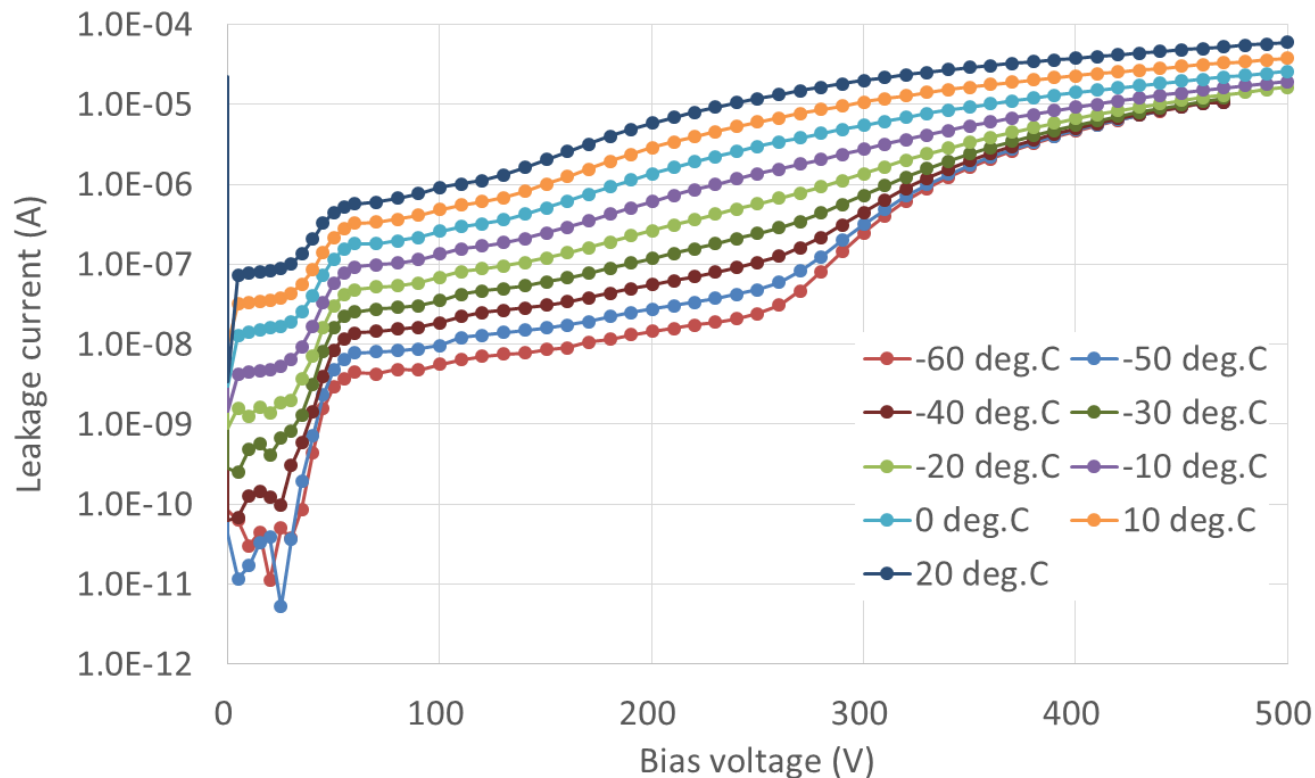
Gain = 17.08  $\mu\text{V}/e^-$

(circuit gain =  $\sim 0.8$ )

FWHM: 14.3 % (882  $e^-$ ) @22.2 keV

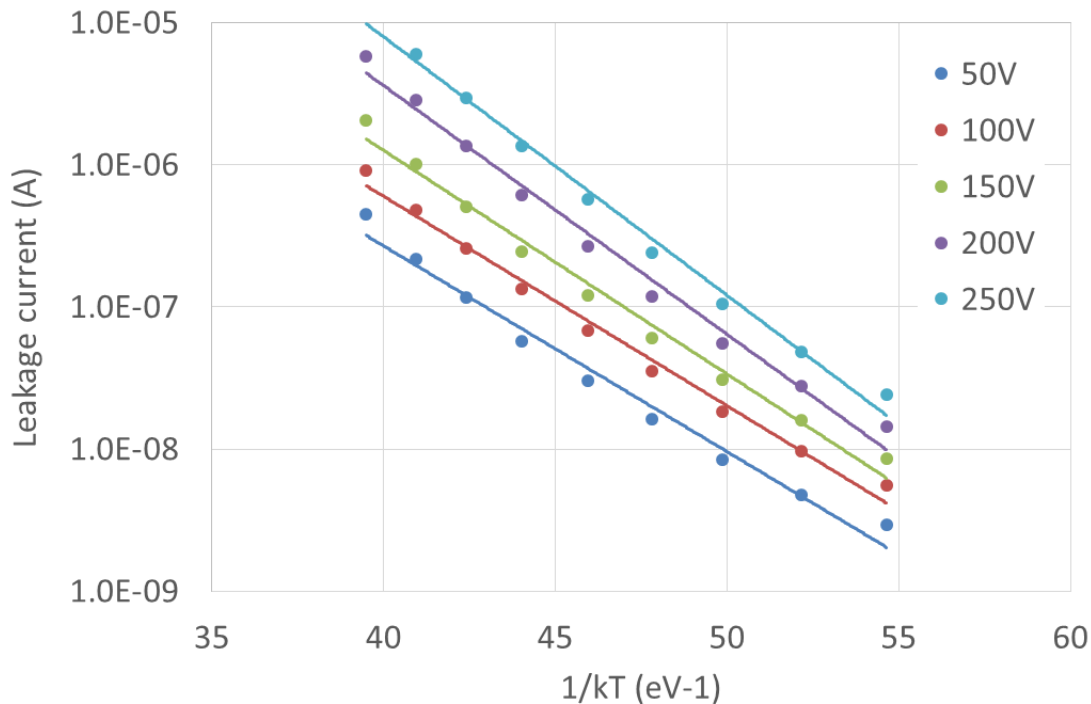
First X-ray spectrum taken with SOI-FZ sensor.

# IV characteristics (FZ)



- Temperature: -60 deg.C ~ +20 deg.C (10 deg.C step)
- At each temperature, there is no significant breakdown.
- Current increase around 280V is probably caused by reaching the depletion region to side or back surface. The cause of the increase around 50V is under investigation.

# Arrhenius plot (FZ)



$$I = A e^{\frac{-E_a}{kT}}$$

I: Leakage current

A: Constant

$E_a$ : Activation energy

k: Boltzmann constant

T: Absolute temperature

$$E_a = 0.41 \text{ eV @250 V}$$

$$(Cz = 0.56 \text{ eV (=} E_g/2))$$

Activation energy of the FZ sensor is less than that of the Cz sensor.  
Thus other source but generation current is expected.



# summary

We are developing monolithic pixel detectors using an SOI technology for X-ray and charged particle applications.

- INTPIX4 works successfully.
  - High resolution, high contrast, high rate X-ray images
- FZ sensors show good performance as well as Cz.
  - Spatial resolution: CTF 66 % @ 20 lp/mm
  - Energy resolution: FWHM 14.3 % @22.2 keV
  - ~10 times higher resistivity enables thicker sensing depth at moderate bias voltages.