

Development of Silicon-On-Insulator Monolithic Pixel Detectors

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We are developing monolithic pixel detectors using a Silicon-on-Insulator (SOI) technology for X-ray and charged particle applications. It is based on a 0.2 μm CMOS fully-depleted (FD-)SOI process of Lapis Semiconductor Co. Ltd. The SOI wafer consists of a thick, high-resistivity substrate for the sensing part and a thin Si layer for CMOS circuits.

To overcome back-gate effect affected by higher back bias voltages, we have successfully introduced buried-well structures. Furthermore, to reduce crosstalk between the sensing node and the pixel circuit, we have developed a double-SOI wafer process. Newly introduced middle Si layer also works as a compensation electrode to the electric field generated by oxide trapped holes created by radiations.

Here we present recent progress and test results of the SOI monolithic pixel detectors.

Author: MITSUI, Shingo (High Energy Accelerator Research Organization (JP))

Co-authors: ISHIKAWA, Akimasa (Tohoku University (JP)); TAKEDA, Ayaki (The Graduate University for Advanced Studies (JP)); HARA, Kazuhiko (University of Tsukuba (JP)); TAUCHI, Kazuya (High Energy Accelerator Research Organization (JP)); SHINODA, Naoyuki (Tohoku University (JP)); HONDA, Shunshuke (University of Tsukuba (JP)); TSUBOYAMA, Toru (High Energy Accelerator Research Organization (JP)); MIYOSHI, Toshinobu (High Energy Accelerator Research Organization (JP)); ARAI, Yasuo (High Energy Accelerator Research Organization (JP)); Ikegami, Yoichi (High Energy Accelerator Research Organization (JP)); ONO, Yoshimasa (Tohoku University (JP)); UNNO, Yoshinobu (High Energy Accelerator Research Organization (JP)); FUJITA, Yowichi (High Energy Accelerator Research Organization (JP)); IKEMOTO, Yukiko (High Energy Accelerator Research Organization (JP))

Presenter: MITSUI, Shingo (High Energy Accelerator Research Organization (JP))

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