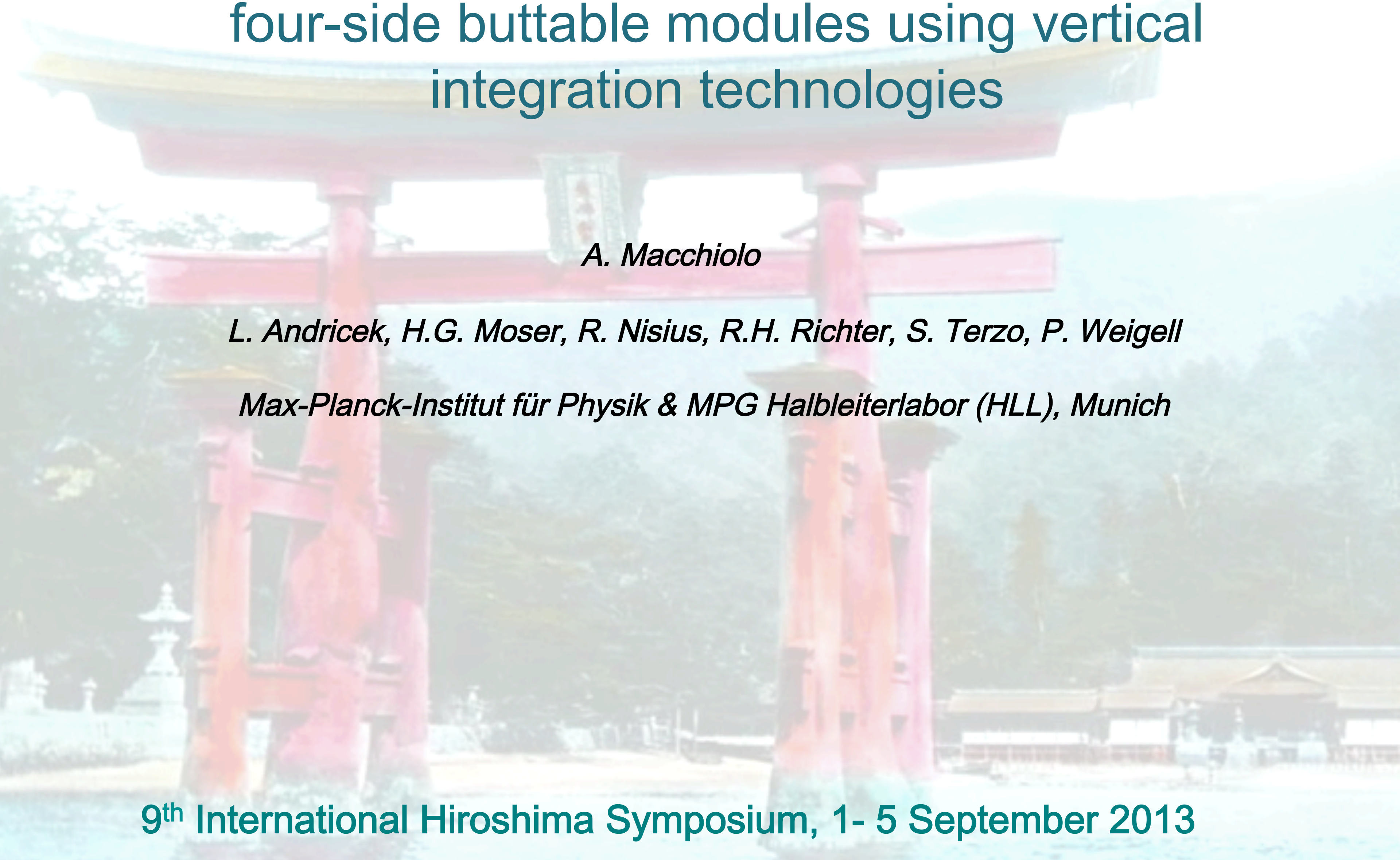


Active edge pixel sensors and development of four-side buttable modules using vertical integration technologies

A. Macchiolo

L. Andricek, H.G. Moser, R. Nisius, R.H. Richter, S. Terzo, P. Weigell

Max-Planck-Institut für Physik & MPG Halbleiterlabor (HLL), Munich

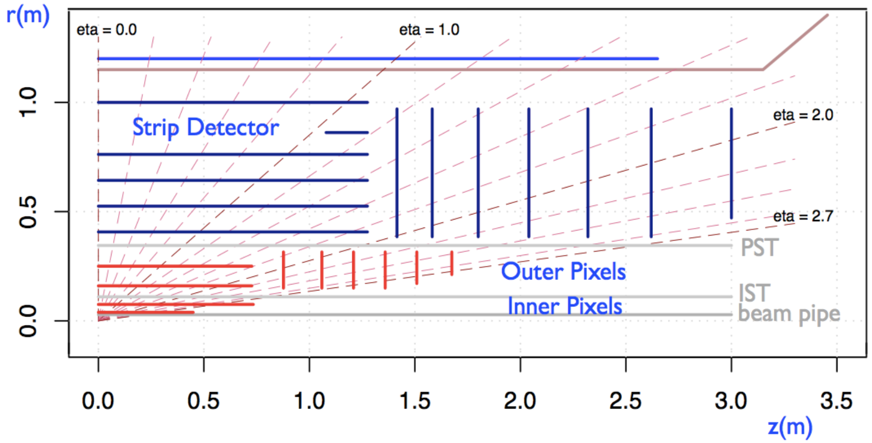
9th International Hiroshima Symposium, 1- 5 September 2013

Requirements for the ATLAS Pixel System upgrade

- ❑ Baseline design for the upgrade of the ATLAS pixel detector for the higher luminosity phase of the LHC (> 2022)

The layout proposed in the LoI provides 14 points/track to |n| < 2.7

Pixel: 4 layers + 6 disks, 25 x 150 (in) / 50 x 150 (out) μm^2



❑ Requirement for the pixel inner layers:

- **Radiation hardness** requirements of 2×10^{16} n_{eq}/cm^2 in the inner pixel layer
- **Thinner silicon** sensors to reduce multiple scattering
- **Low fraction of inactive area** to reduce geometrical inefficiencies, especially in the inner tracking layer where it will not be possible to overlay the modules along the beam direction → active edge sensors + vertical integration technologies

Requirements for the ATLAS Pixel System upgrade

- ☐ Baseline design for the upgrade of the ATLAS pixel detector for the higher luminosity phase of the LHC (> 2022)

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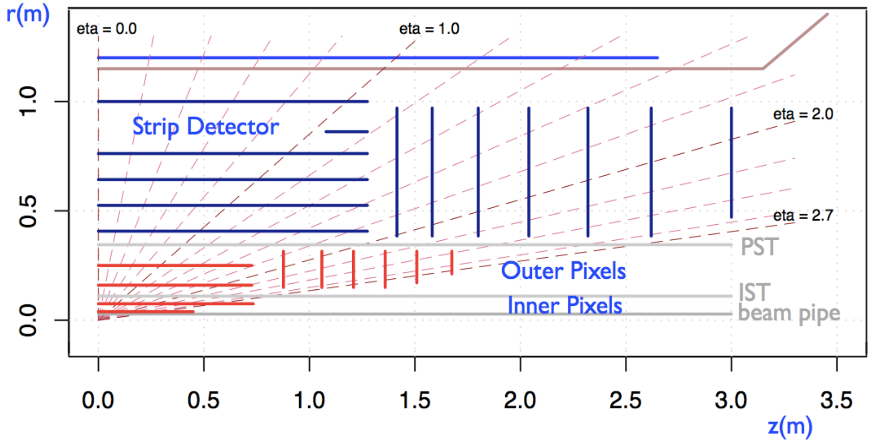
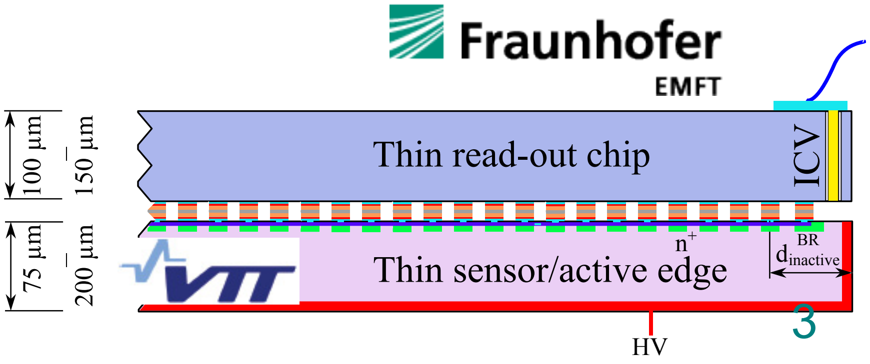
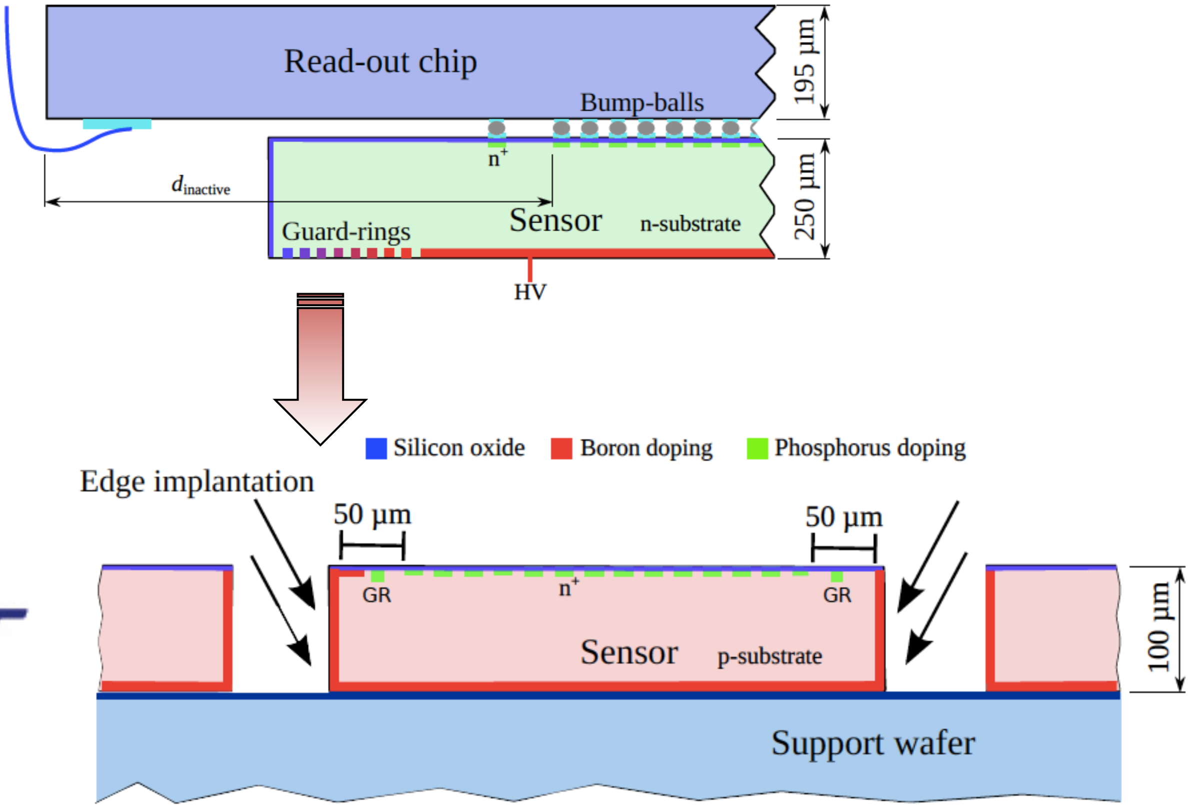


- ☐ MPP 3D integrated demonstrator module to achieve a fully four-side buttable module, in collaboration with EMFT and VTT



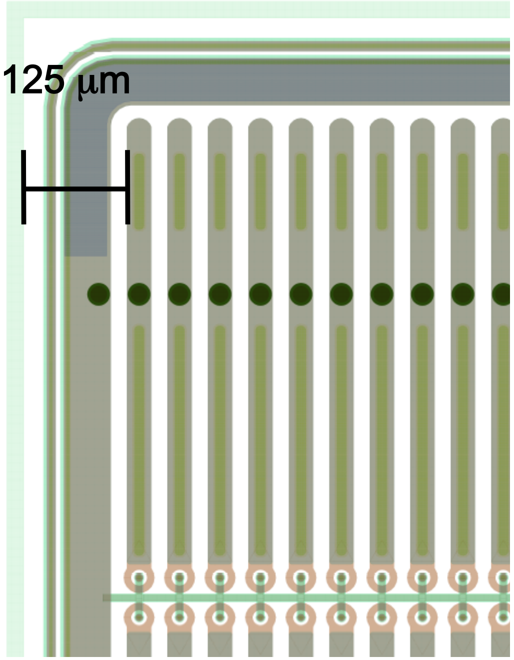
- **Active edge** n-in-p pixels with a thickness in the range (100-200) μm
- **SLID interconnection** to achieve a pitch of 25 μm
- **Inter Chip Vias (ICV)** to route signal and services to the ASIC backside

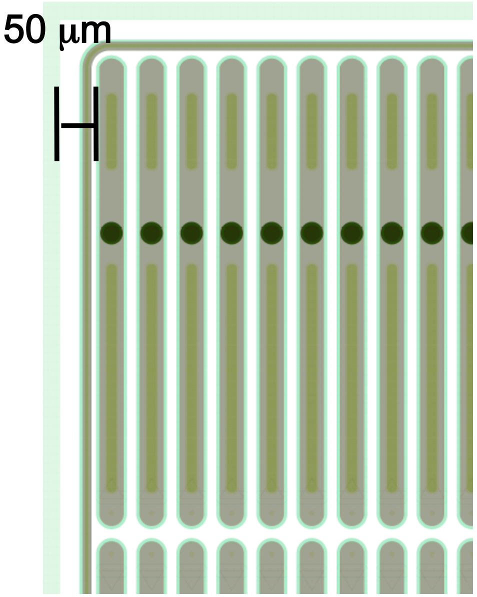
Reduction of the inactive region on the sensor side



- n-in-p pixels on FZ and MCZ material
- 100 μm and 200 μm active thickness →together with the active edges makes these sensors very attractive candidates for the inner layers in Phase II
- p-spray isolation method transferred from HLL to VTT
- Flip-chipping performed at VTT after bump-deposition on the FE-I4 chip wafers.

Geometry and IV characterization



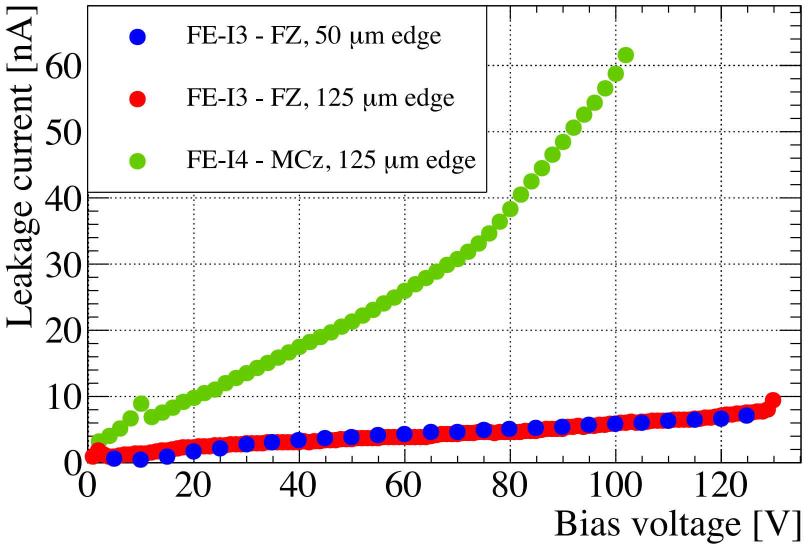


- 125 µm edge implemented In FE-I3 and FE-I4 sensors: Bias Ring + floating Guard Ring

- 50 µm implemented only in FE-I3 sensors: Floating Guard Ring

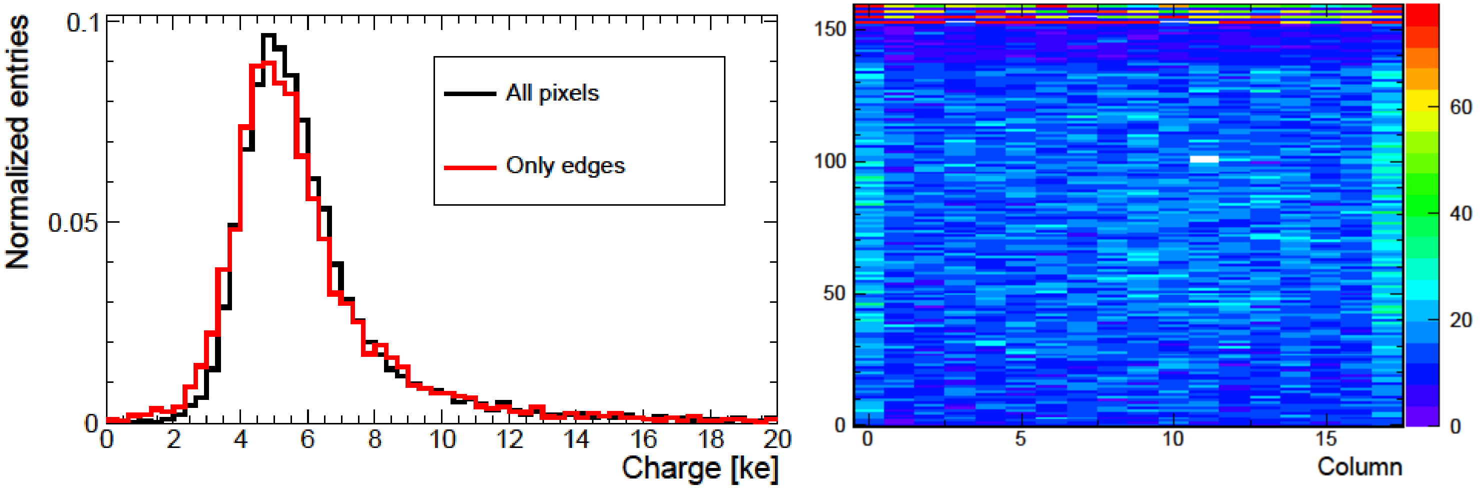
- Very low leakage current level, < 100 nA for FE-I3 and FE-I4 sensors

- Breakdown voltage at 100-110V, much higher than depletion voltage ~ 15V



A. Macchiolo, Active Edge Pixel Sensors, Hiroshima Symposium 2013

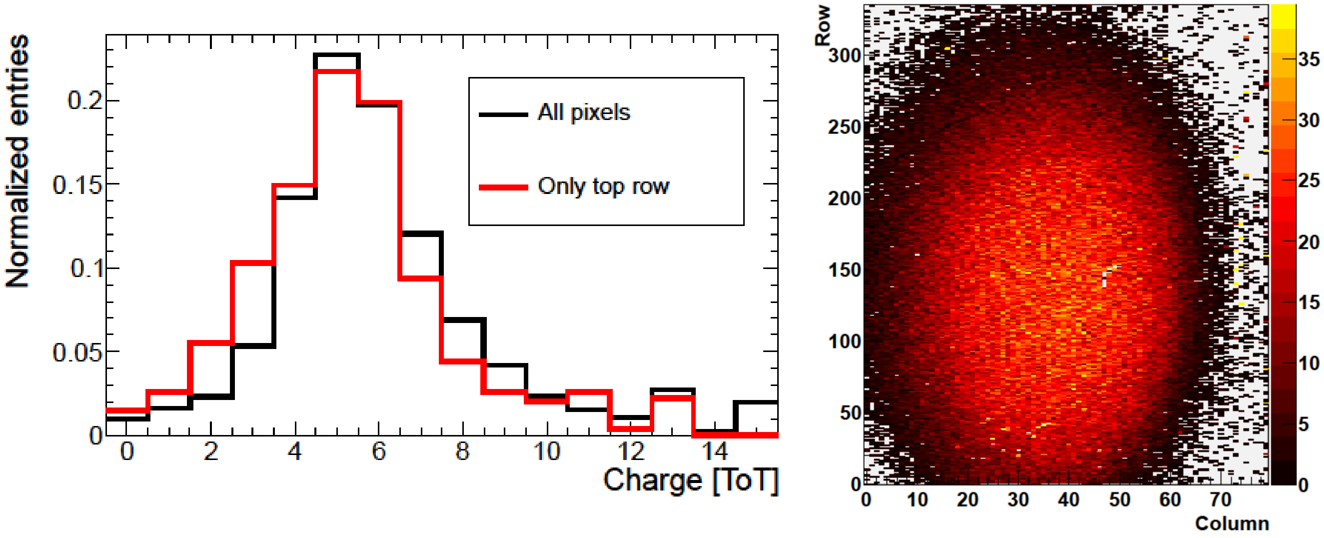
Charge collection with a ^{90}Sr a source



FE-I3

50 μm edge

V_{bias}=15 V



FE-I4

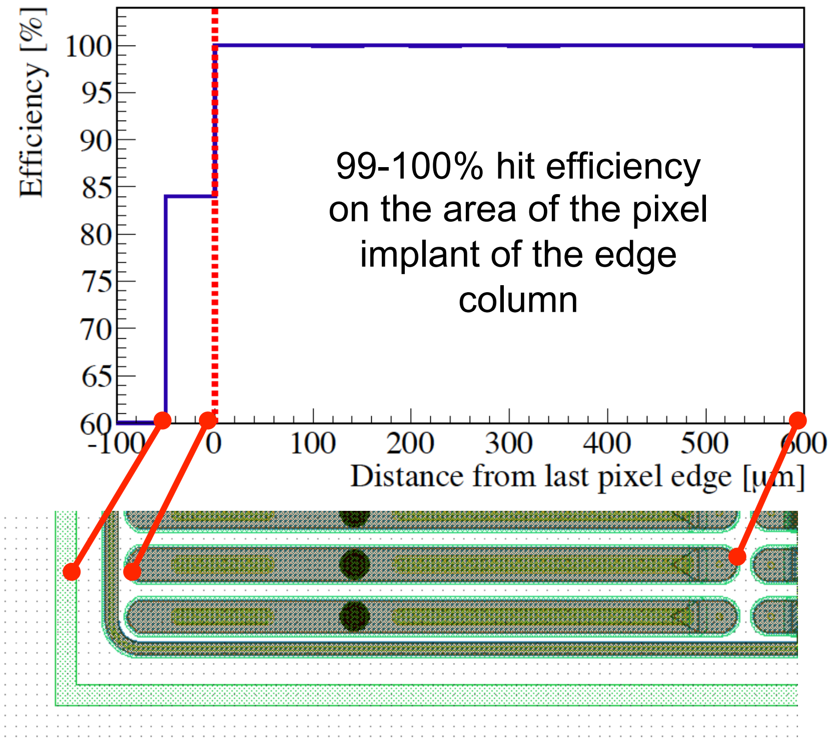
125 μm edge

V_{bias}=15 V

- ☐ Edge pixels show the same charge collection properties as the central ones

Hit efficiency in the edge region

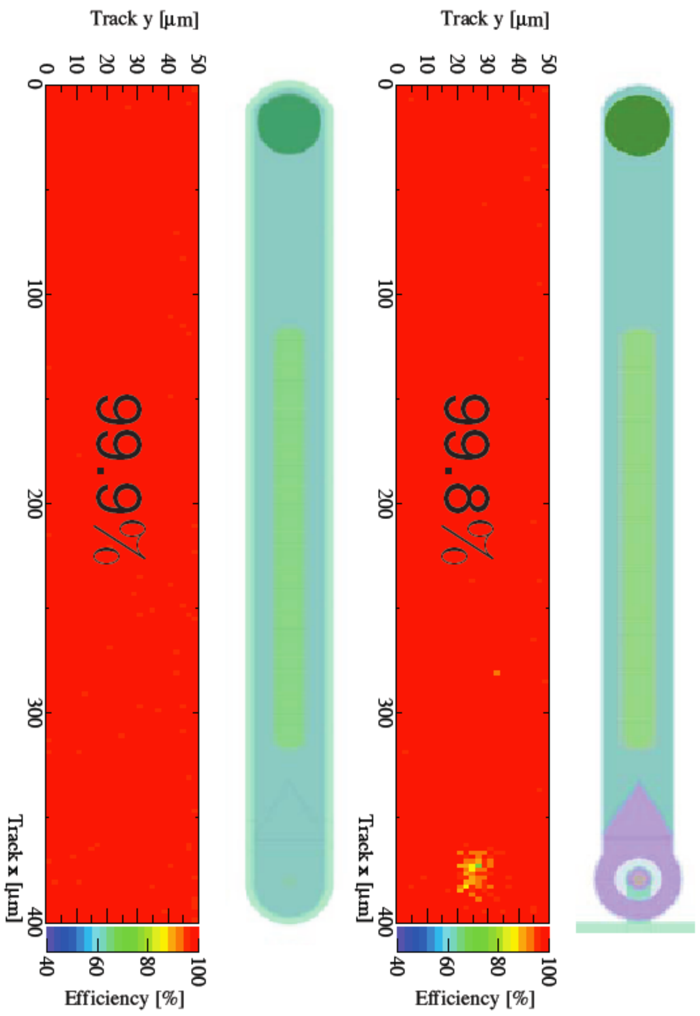
Edge Tracking Efficiency in Beam Tests at SPS



99-100% hit efficiency on the area of the pixel implant of the edge column

- ❑ 84^{+9}_{-14} % efficiency in the last 50 μm of the sensor edge, beyond last pixel implant

Global Efficiency in beam test

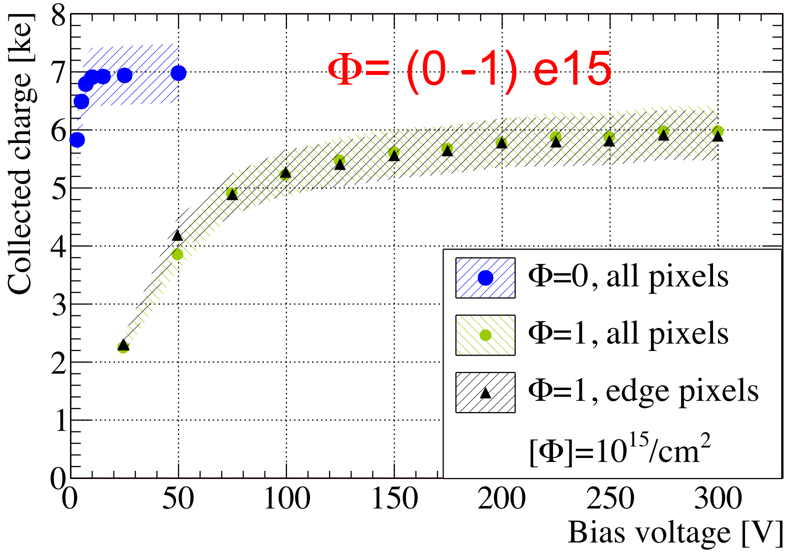


FE-I3, 50 μm edge, Vbias=20V

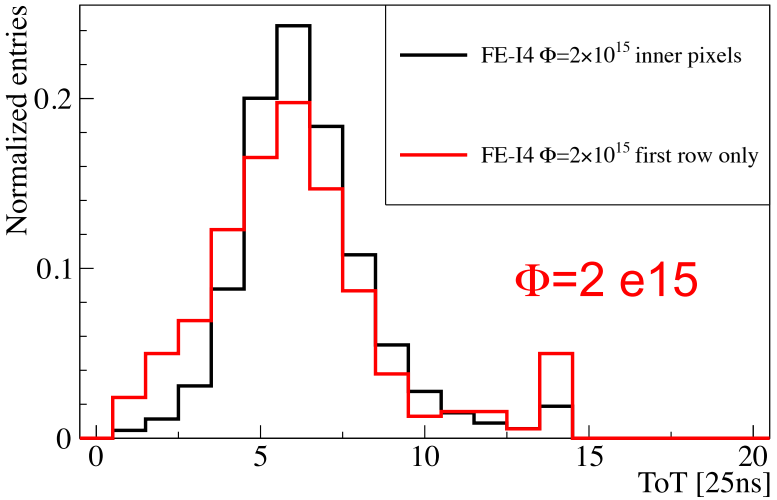
FE-I3, 125 μm edge, Vbias=20V

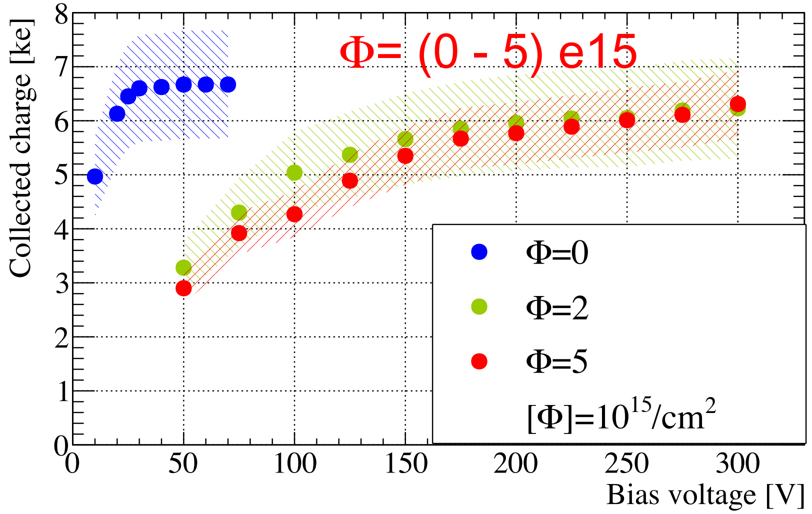
Charge collection efficiency after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT ($1x10^{15}$ n_{eq}/cm^2)



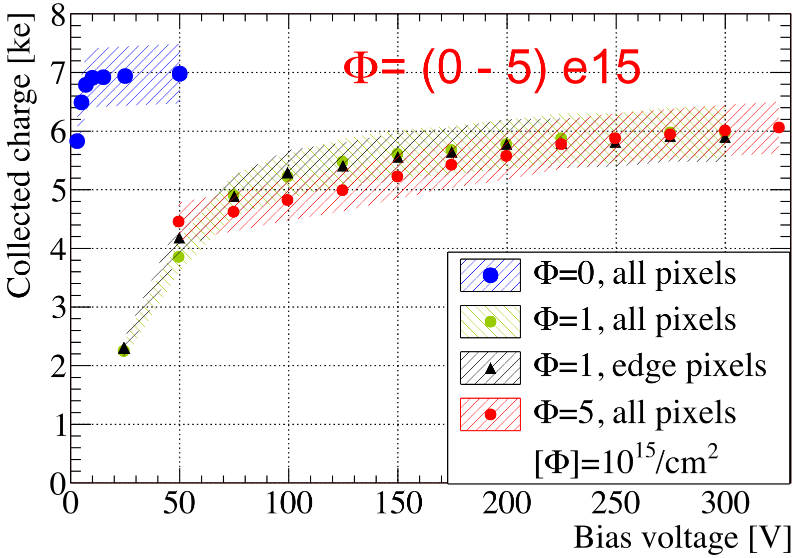
- p-type MCZ FE-I4, 100 μm thick sensor, with 125 μm slim edge, threshold 1100 e- → compatible charge collection properties between edge and internal pixels



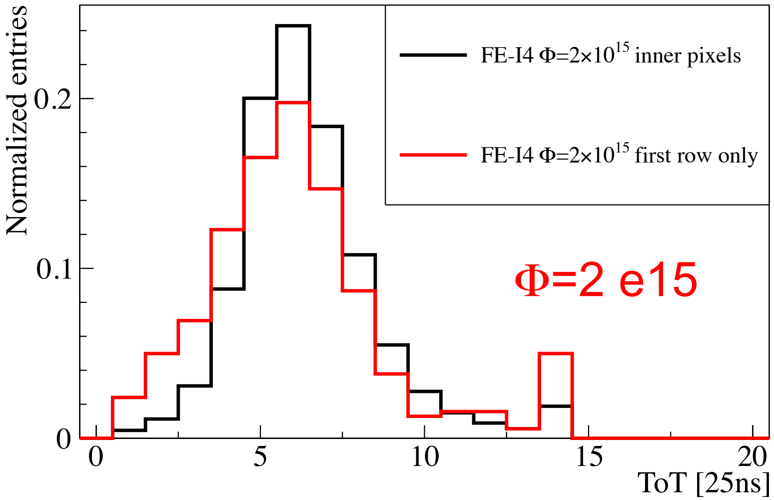


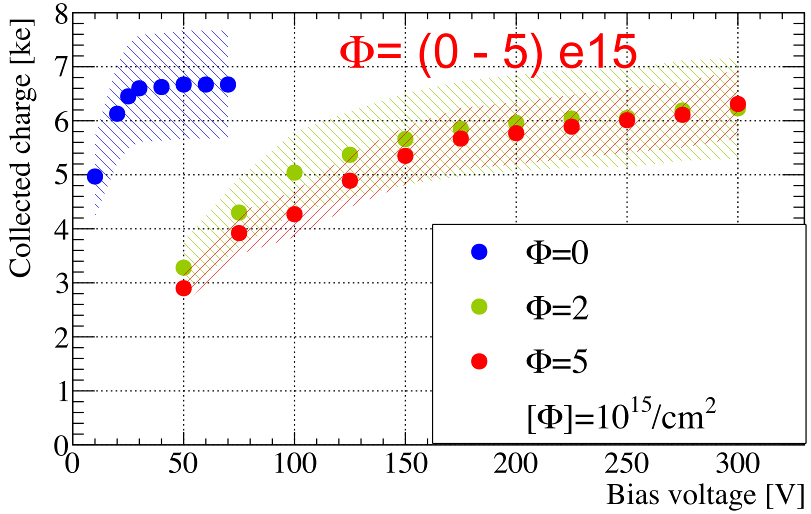
Charge collection efficiency after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → 87% CCE at 300 V for both all and edge pixels after irradiation at KIT ($1x10^{15}$ n_{eq}/cm^2) and in Ljubljana ($5x10^{15}$ n_{eq}/cm^2)



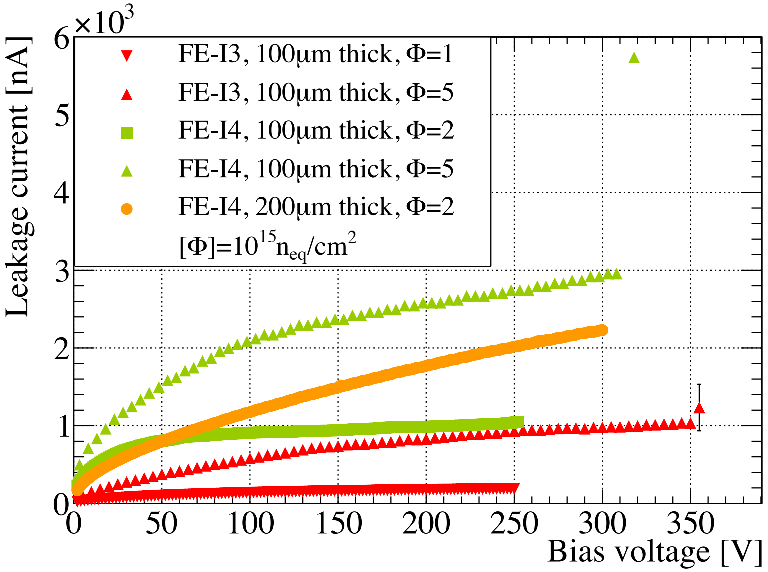
- p-type MCZ FE-I4, 100 μm thick sensor, with 125 μm slim edge, threshold 1100 e- → compatible charge collection properties between edge and internal pixels





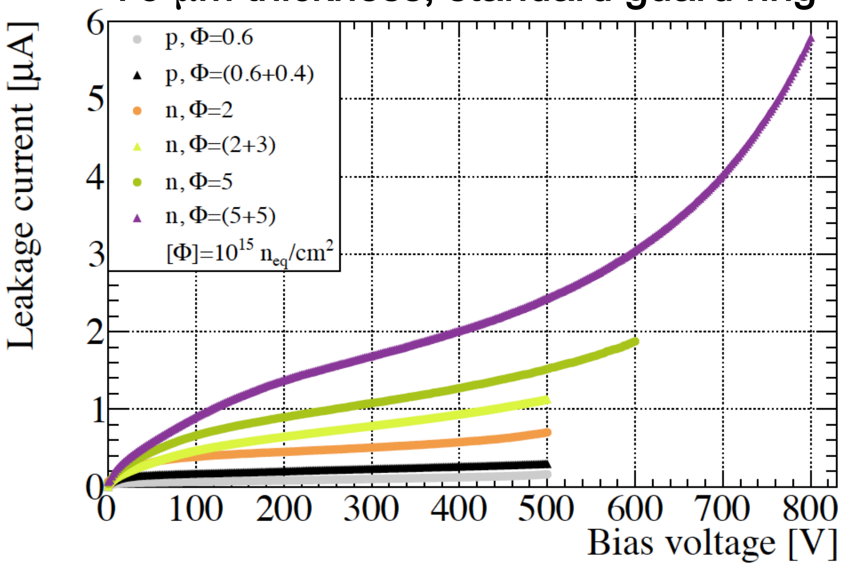
IV after irradiation

100 and 200 μm thickness, active edge

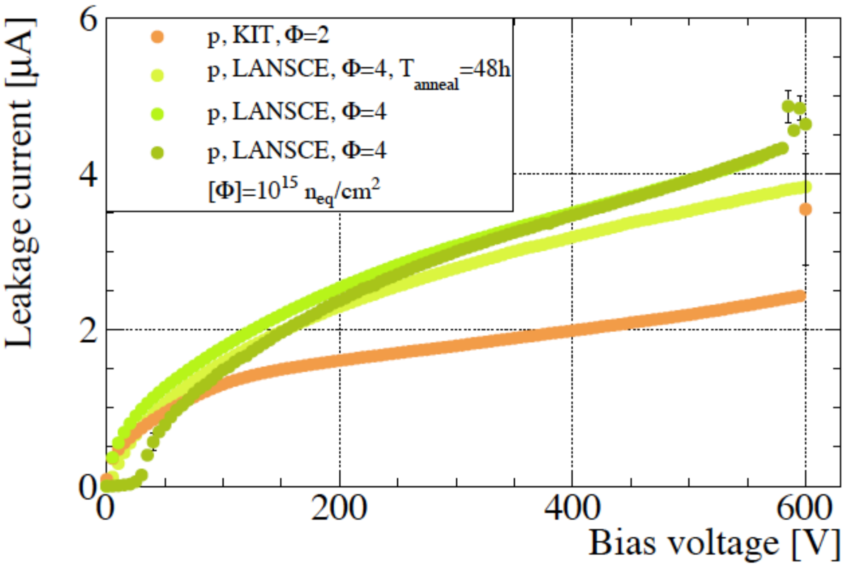


- Active edge modules irradiated up to a fluence of $5x10^{15}$ n_{eq}/ cm^2 have a breakdown voltage above the saturation voltage of the charge collection
- Lower breakdown voltages with respect to thin pixel devices with standard GR structure irradiated at the same fluence

75 μm thickness, standard guard ring



150 μm thickness,
GR with 450 μm inactive edge

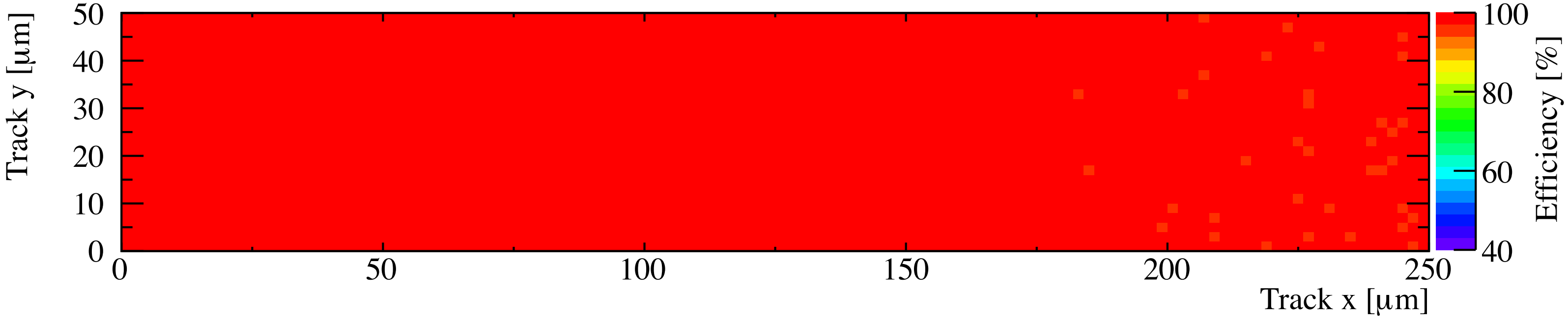


DESY test-beam – 100 μm thick sensors

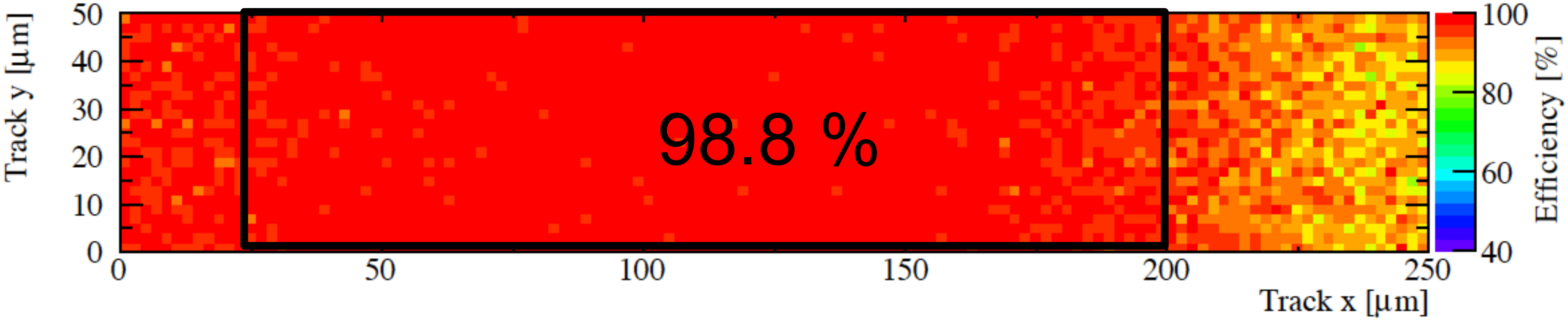
- ❑ Test-beam results from DESY test-beam 6 GeV electrons, EUDET telescope
  → due to multiple scattering the analysis of the edge efficiency is not possible

- ❑ Tuning Threshold=1600 e, 6 ToT@6ke, beam at perpendicular incidence

- ❑ VTT FZ, 100 μm thick, not irradiated → total efficiency 99.7% at 40 V

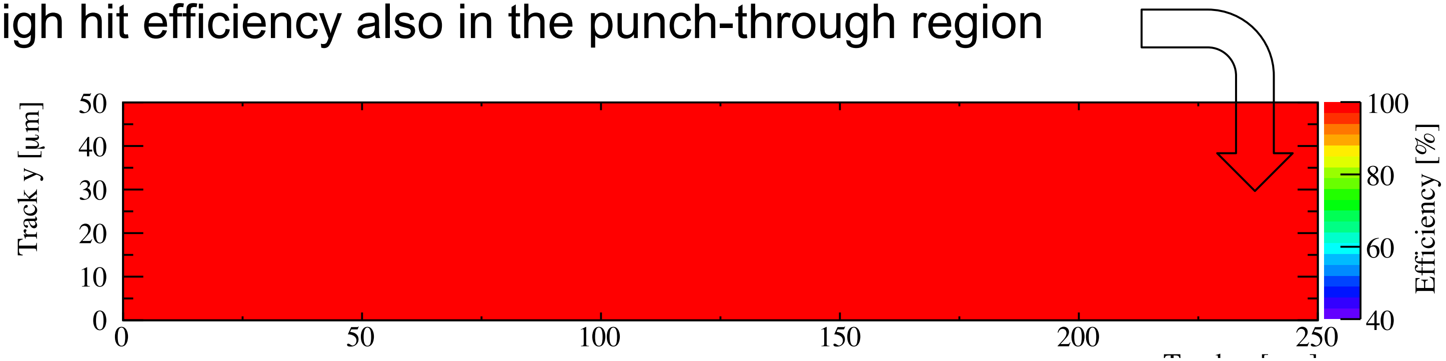


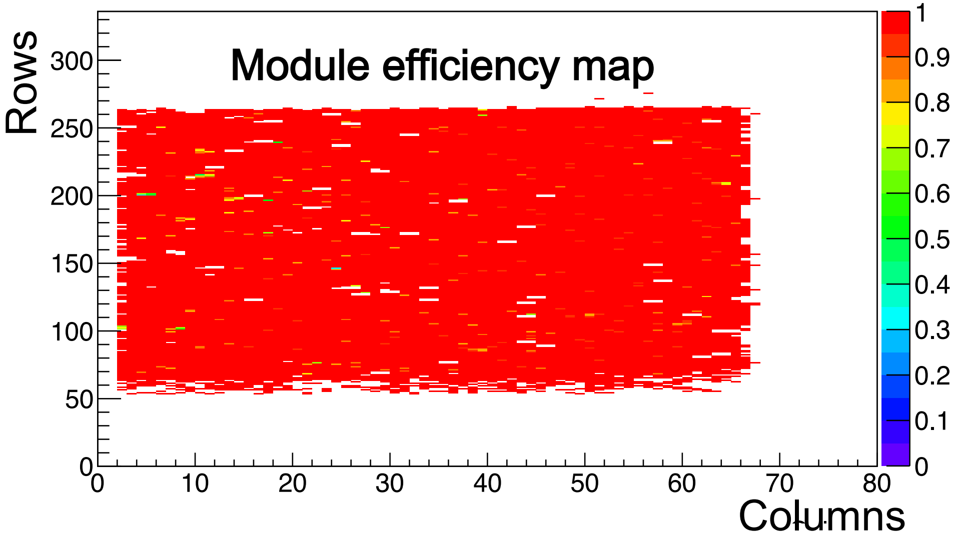
- ❑ VTT MCZ, 100 μm thick, Φ=2e15 → total efficiency 97.3% at 350 V

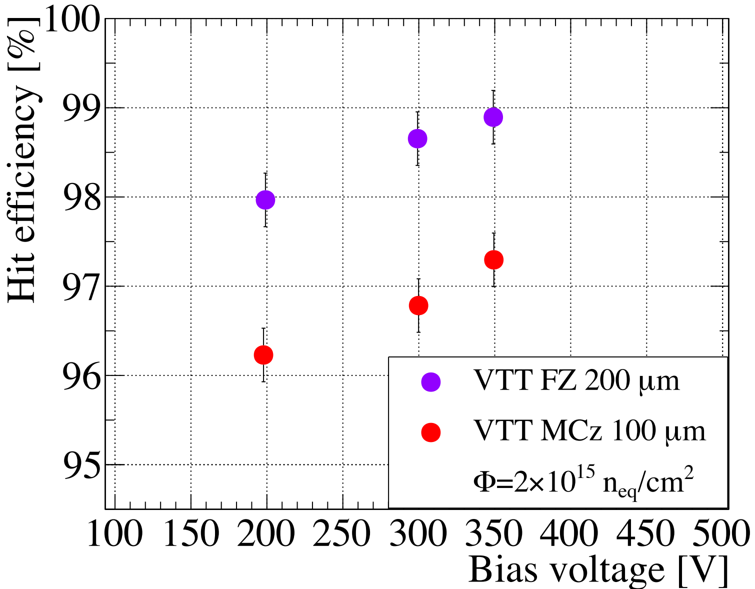


DESY test-beam – 200 µm thick sensors

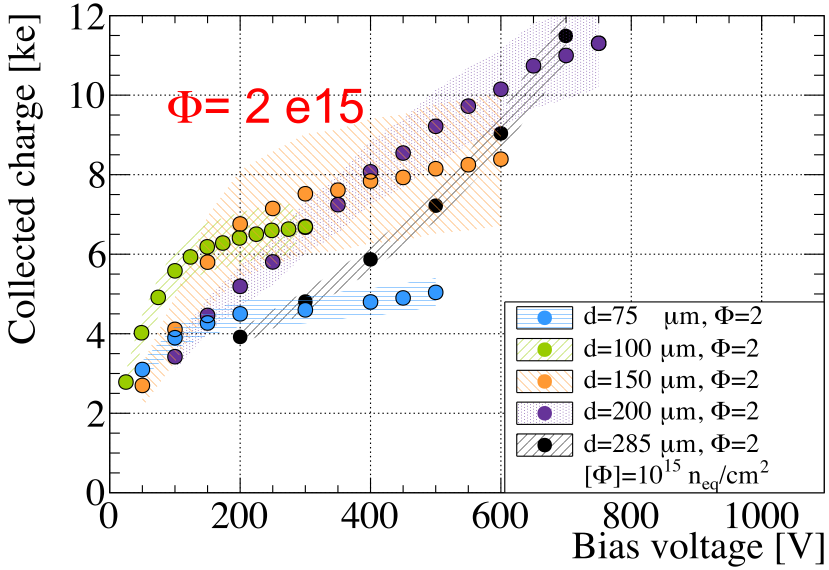
- ☐ VTT FZ, standard GR, 200 µm thick, Φ=2e15 → total efficiency 98.9% at 350 V
- ☐ Tuning Threshold=1100 e, 6 ToT@ 6 ke
- ☐ Perpendicular incidence
- ☐ High hit efficiency also in the punch-through region

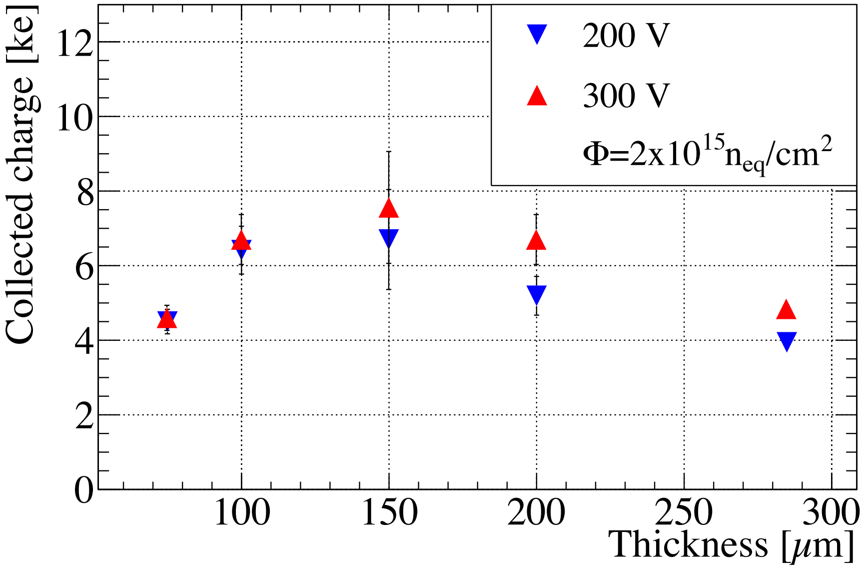


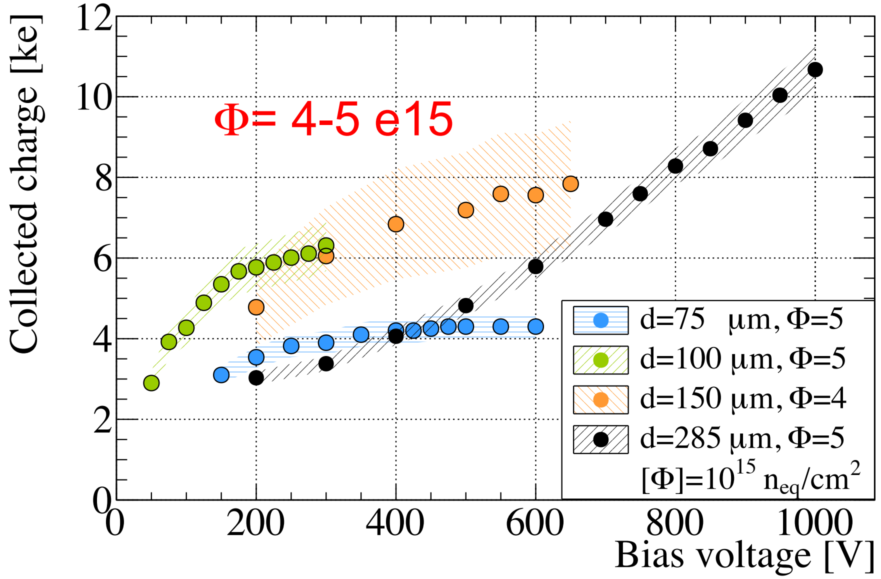




Charge collection for pixels of different thickness

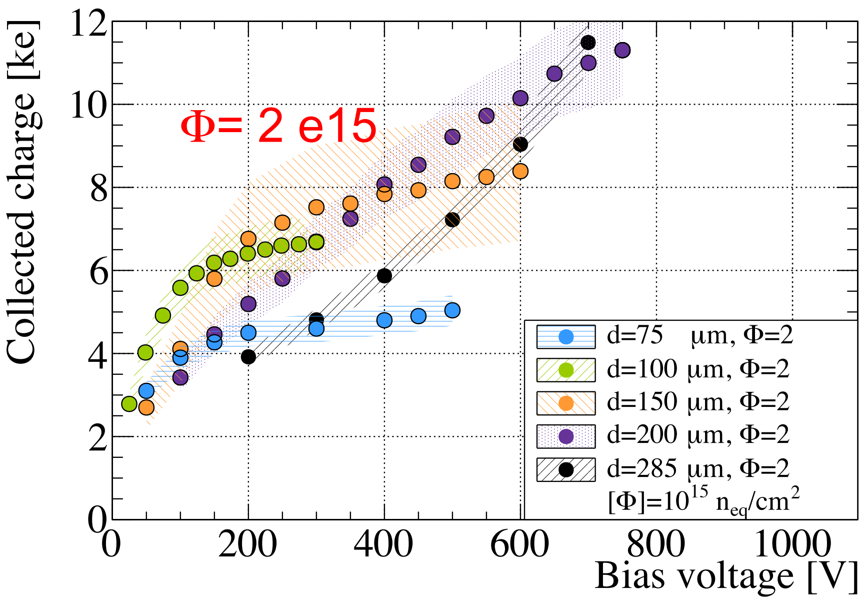


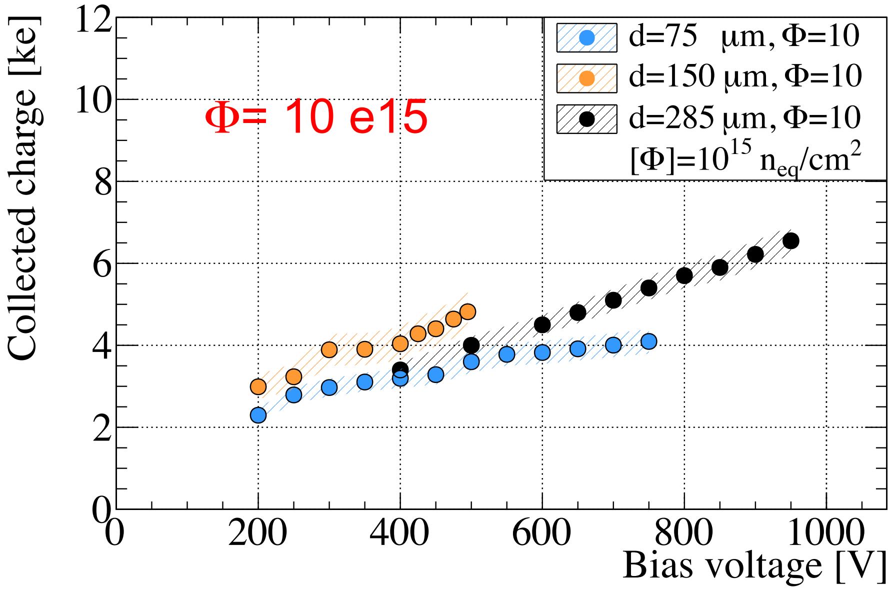


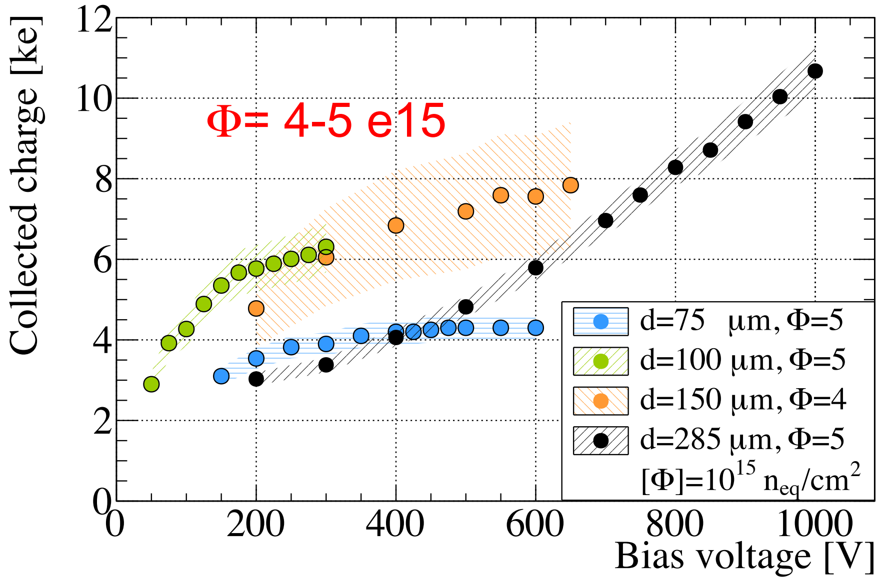


- The 100-150 μm thick sensors show higher charge collection up to a fluence of 4-5 x10^{15} n_{eq} / cm^2

Charge collection for pixels of different thickness

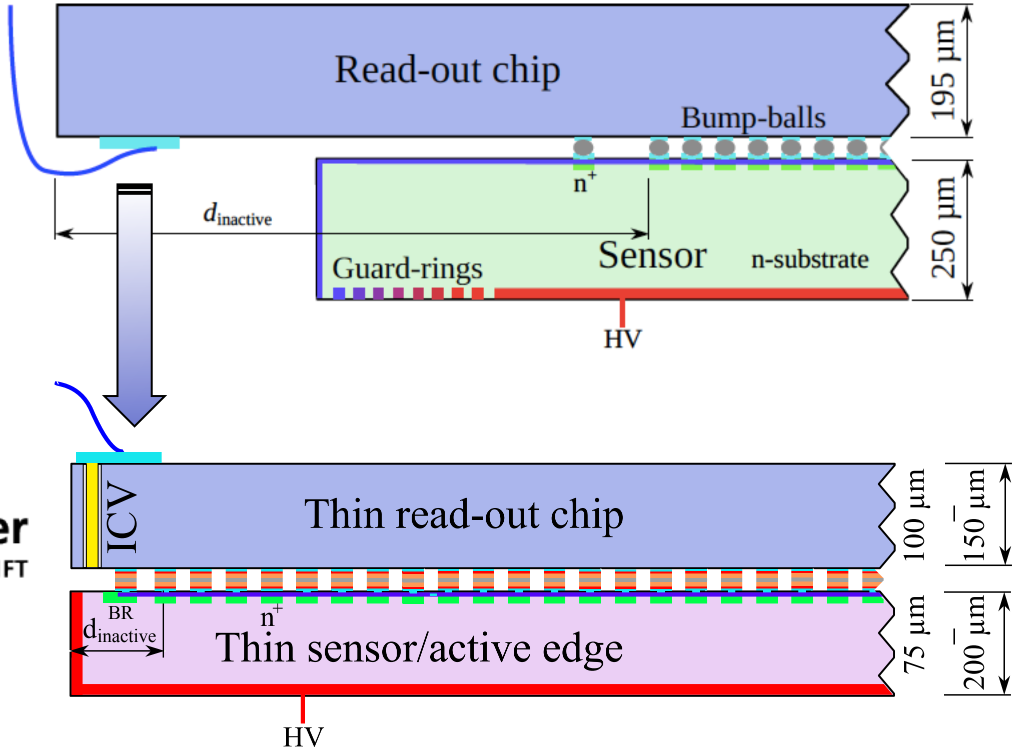






- The 100-150 μm thick sensors show higher charge collection up to a fluence of 4-5x10^{15} n_{eq} / cm^2
- At higher fluences the effect of charge trapping tends to equalize the charge collection efficiency for all thicknesses

Reduction of the inactive region on the chip side



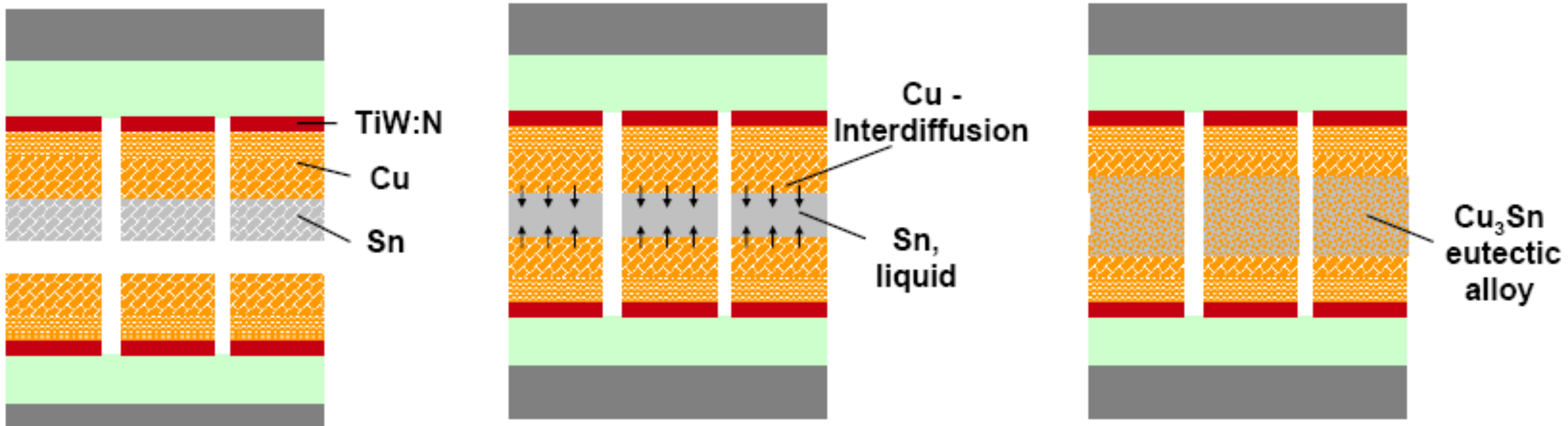
Fraunhofer
EMFT

- ❑ Project within AIDA WP3, in collaboration with Fraunhofer EMFT, to develop Inter Chip Vias to show the feasibility to transport signals and services on the backside using the existing FE-I4 chip
- ❑ Inter-Chip-Vias to be etched on each wire bonding pad, cross section ~ 10x30 μm^2
- ❑ Chip and sensor connected using SLID technology

EMFT SLID Process

Fraunhofer
EMFT

Metallization SLID (Solid Liquid Interdiffusion)



Through Mask Electroplating

Contact under Pressure and Heat
~ 5 bar, 260 – 300 °C (Sn-melt)

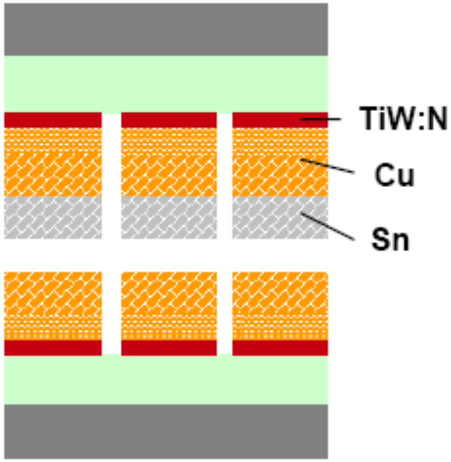
Formation of Eutectic Alloy;
$T_{melt} > 600$ °C

- ❑ Alternative to bump bonding (less process steps "lower cost" (EMFT)).
- ❑ Small pitch possible (~ 20 μm, depending on pick & place precision).
- ❑ Stacking possible (next bonding process does not affect previous bond).
- ❑ Wafer to wafer and chip to wafer possible.

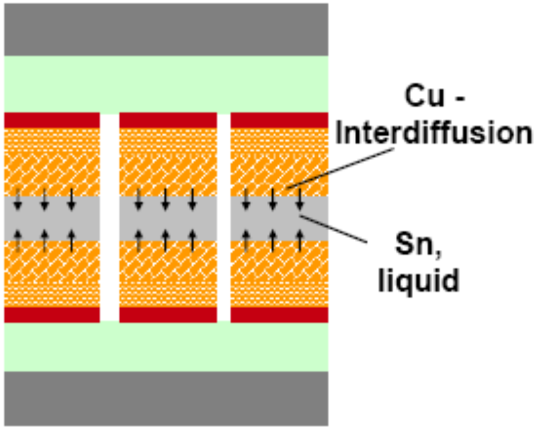
EMFT SLID Process

Metallization SLID (Solid Liquid Interdiffusion)

Fraunhofer
EMFT



Through Mask Electroplating



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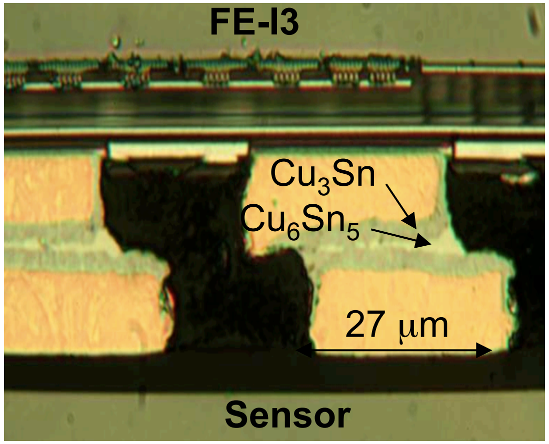

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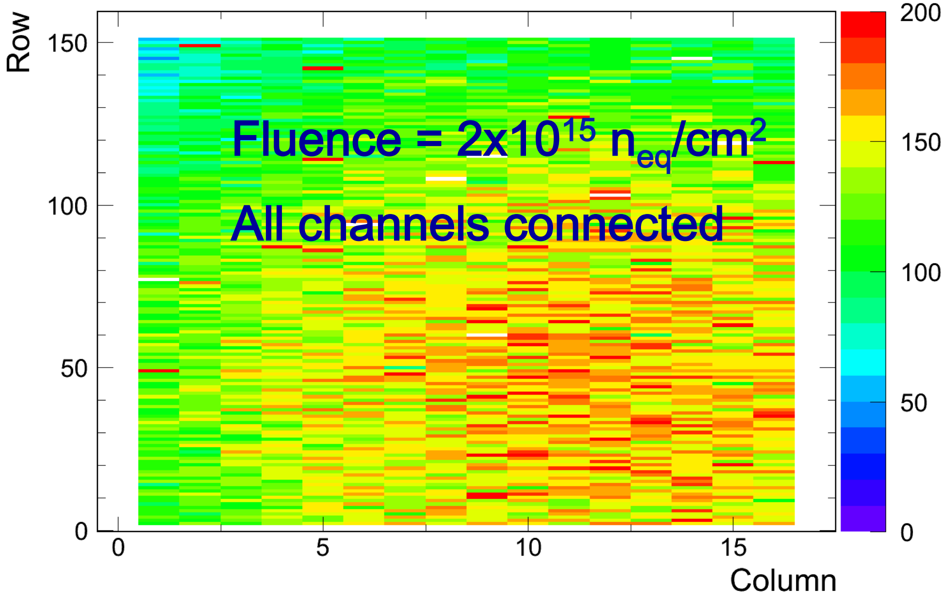
- Small pitch possible (~ 20 μm, depending on pick & place precision).
- Stacking possible (next bonding process does not affect previous bond).
- Wafer to wafer and chip to wafer possible.

Results with FE-I3 SLID pixel modules

- Noise performance comparable to detectors interconnected with bump-bonding

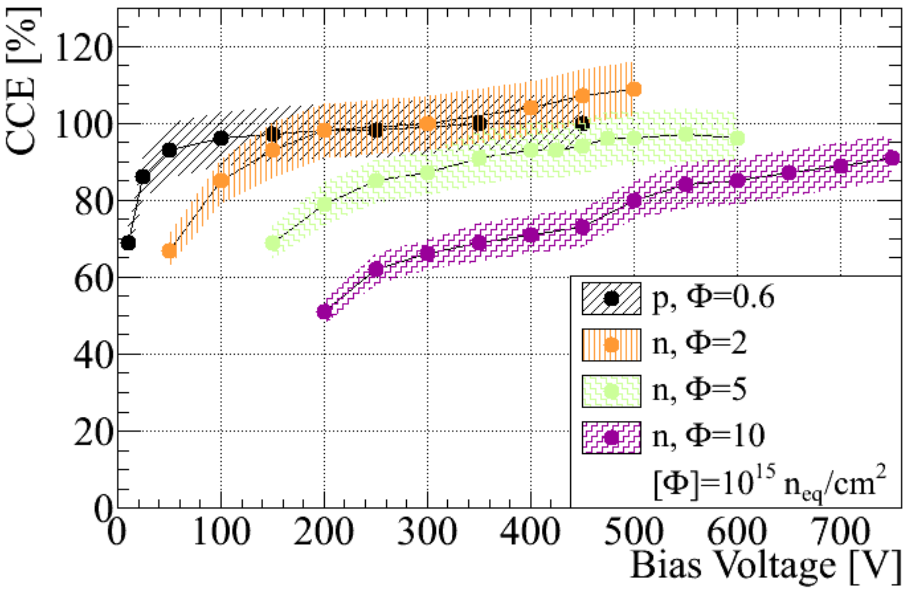
- Stable SLID interconnection after irradiation and thermal cycling



Fluence = $2x10^{15}$ n_{eq}/cm^2

All channels connected

Charge collection after irradiation

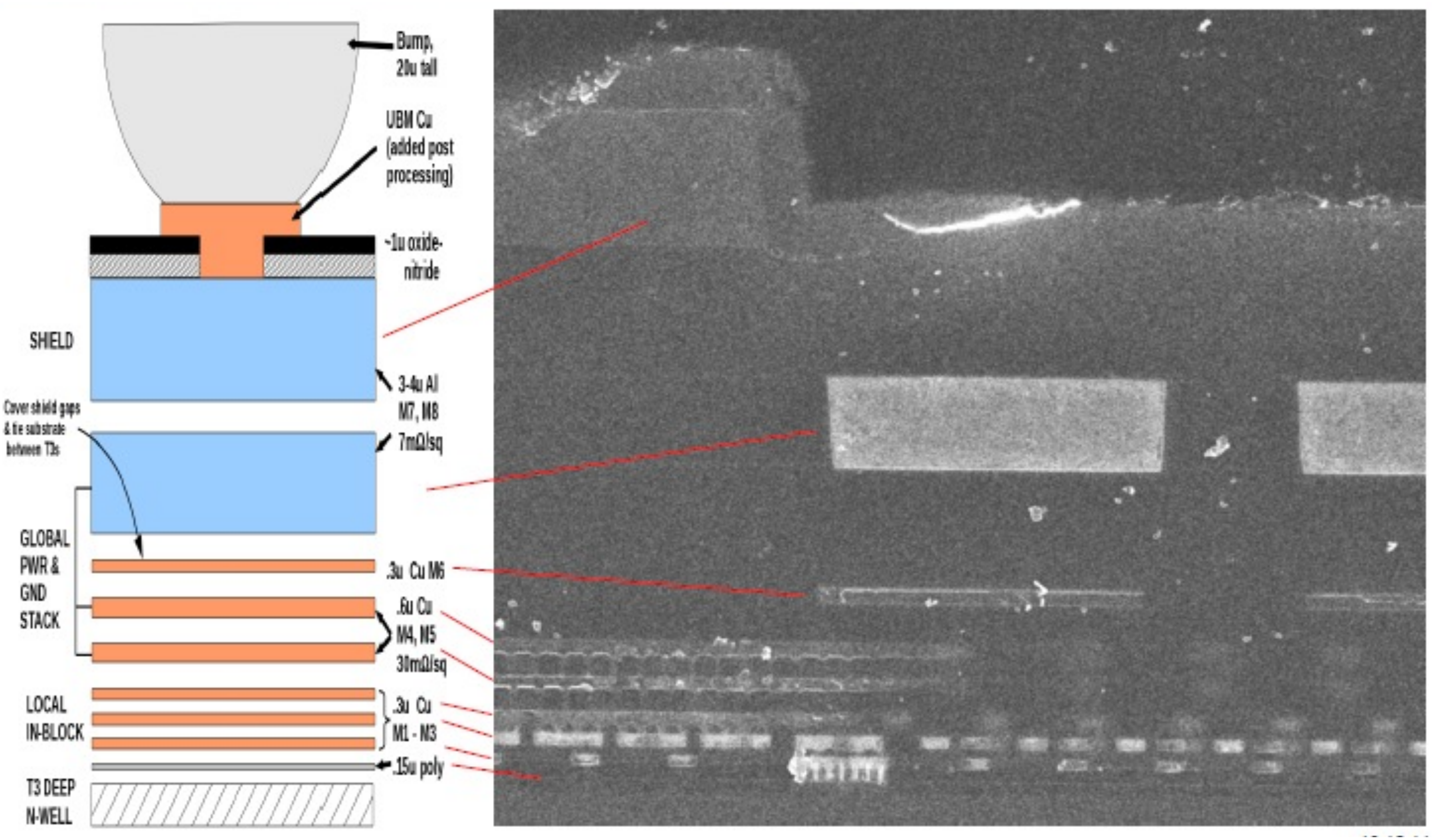


- Good Charge Collection efficiency after irradiation up to 10^{16} n_{eq}/cm^2

SLID interconnection run with FE-I4 sensors (CIS production) and chips foreseen at the end of this year

Inter Chip Vias in the FE-I4 chip

SEM analysis of the FE-I4 wire bonding pad



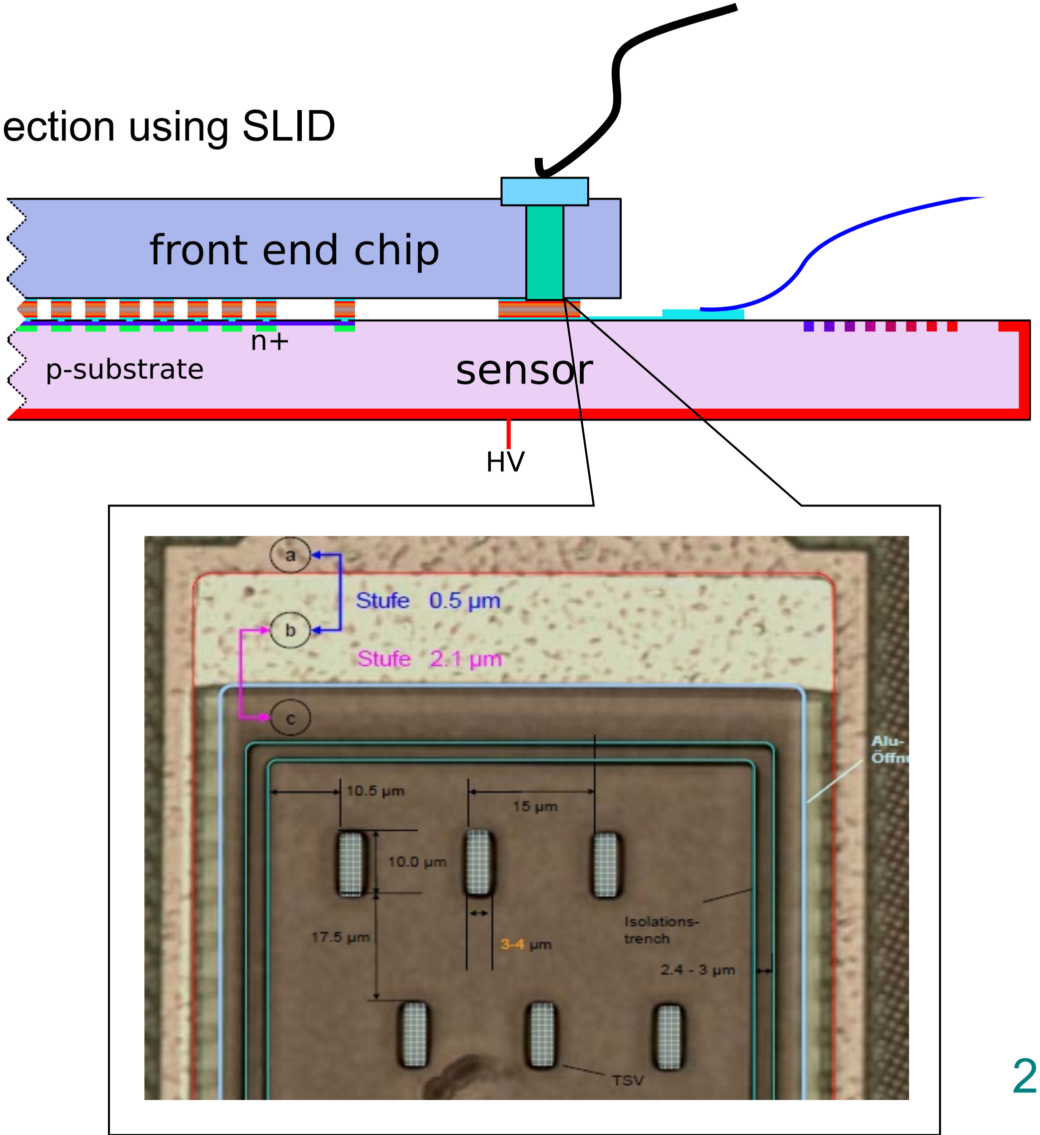
- ❑ Most of the eight FE-I4 metal layers are present in the wire bonding pads → not possible to etch ICV from the front-side
- ❑ Design and test of the ICV layout on test-wafers in on-going: target cross-section 10x30 μm^2 with a global chip thickness of 100-150 μm

Inter Chip Vias on FE-I3 chips

☐ ICV etched in the read-out chip on the front-side on every wire bonding pad of the FE-I3 chip to route signal and services to the ASIC backside

- ASIC thinned to 60 µm
- thin sensors /ASIC interconnection using SLID

Fraunhofer
EMFT

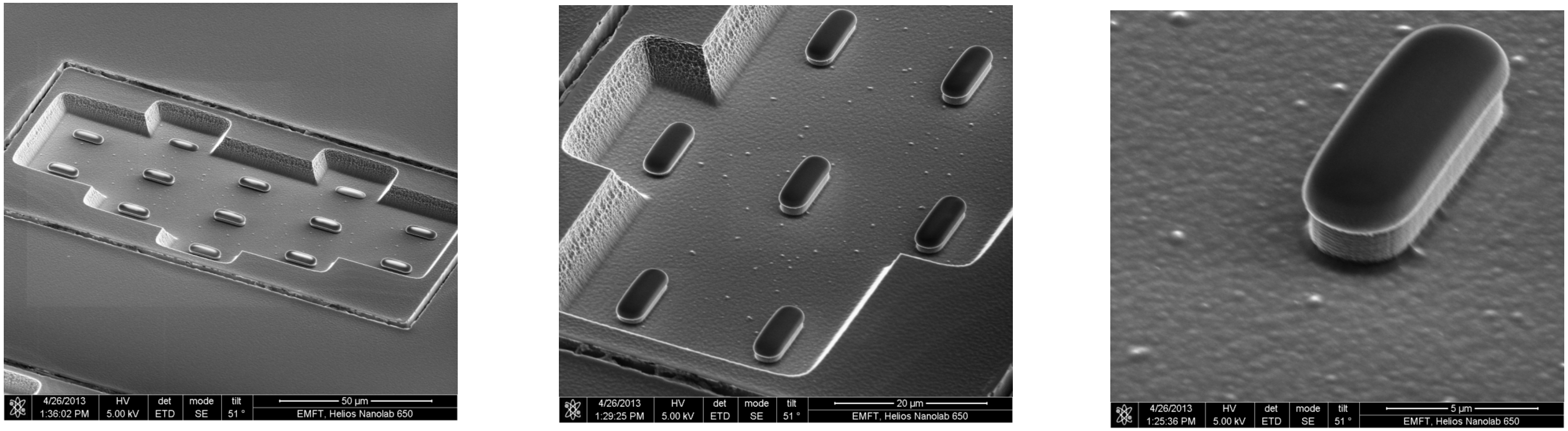


☐ Processing sequence:

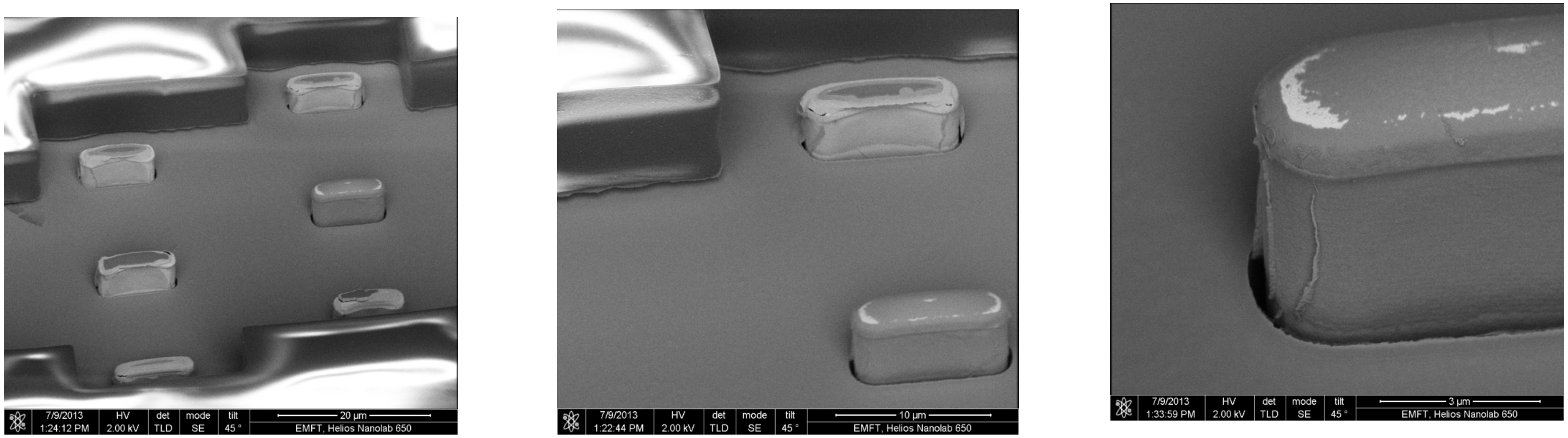
- Via- and trench etching in Bosch-process, TSV cross-section of 3x10 μm^2
- insulation with TEOS (low T)
- filling of vias with Tungsten
- attachment to handle-wafer on the top side and thinning to desired thickness of chip ~ 60 μm
- redistribution layer on the backside
- SLID-interconnection to sensor wafer.

Inter Chip Vias in FE-I3: problems encountered (I)

- TSV preparation from back side after wafer thinning to 60 μm
  - Preparation of ICV within isolation trench: dry recess of silicon

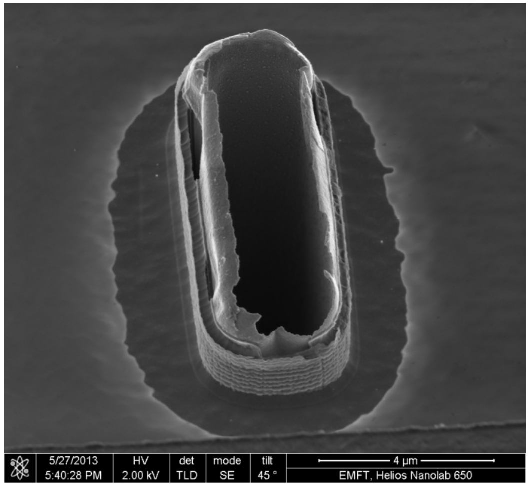


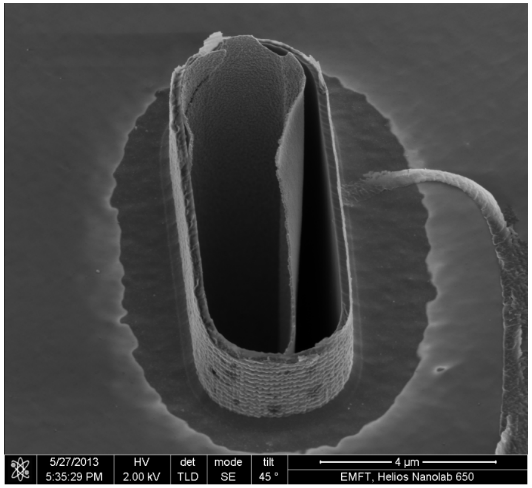
- and after removal of backside isolation oxide within the trench

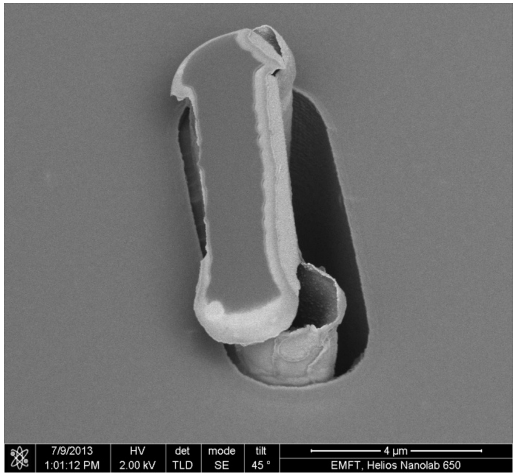


Inter Chip Vias in FE-I3: problems encountered (II)

- After etching of the isolation oxide of each ICV, it was observed that the W filling was not present and the ICVs were void.







- Only TiN-CVD layer visible, done before W deposition as an adhesion layer
- No W, only 60 nm thick TiN-coverage as electrical contact between frontside and backside available → very high resistance for TSV-pin
- We are in discussions with EMFT to see what still can be learned from this production

Summary and outlooks

- Excellent performance of active edge sensors demonstrated before and after irradiation up to a fluence of $5\text{x}10^{15}$ n_{eq} / cm^2

- Charge collection efficiency studies show that thin devices (100-150) μm deliver a slightly higher charge at moderate bias voltage up to a fluence of $5\text{x}10^{15}$ n_{eq} / cm^2

- New production of FE-I4 chips with active edges foreseen at ADVACAM → apply to the FE-I4 modules the design proven with FE-I3 → 50 μm inactive edge and pixels without punch-through structure

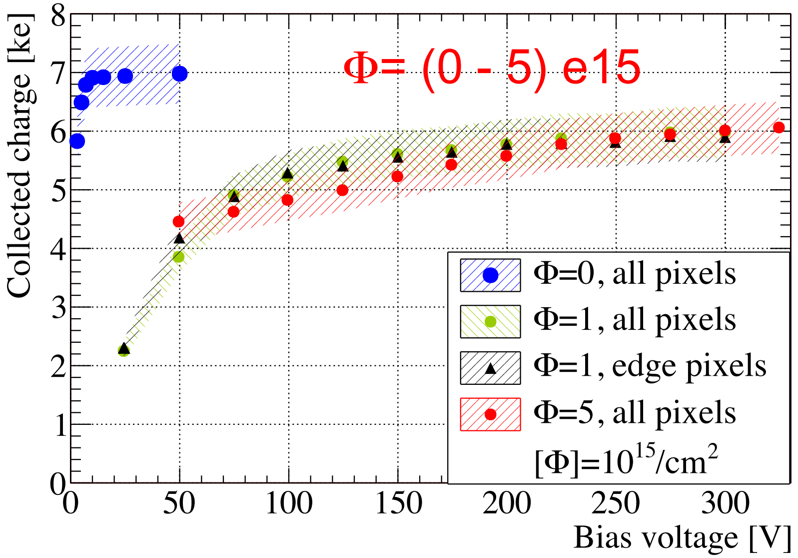
- Further investigation of the SLID interconnection with FE-I4 modules

- Problems encountered in the processing of ICVs on the FE-I3 chip, ICVs on the FE-I4 chip under development at EMFT

Additional material

Charge collection efficiency after irradiation

- FE-I3 100 μm thick sensor with 125 μm slim edge, threshold 1500 e- → irradiated in Ljubljana at 5x10^{15} n$_{eq}$/cm^2



- Landau distribution obtained at the DESY test-beam with 4 GeV electrons