

Active edge pixel sensors and development of four-side buttable modules using vertical integration technologies

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We present an R&D activity focused on the development of novel modules for the upgrade of the ATLAS pixel system at the High Luminosity LHC (HL-LHC). They consist of n-in-p pixel sensors, 100 or 200 μm thick, produced at VTT (Finland) with an active edge technology, to considerably reduce the dead area at the periphery of the device. The sensors are interconnected with solder bump bonding to the ATLAS FE-I3 and FE-I4 read-out chips, and characterized by means of scans with radioactive sources and beam tests at the CERN-SPS and DESY. The results of these measurements will be discussed for devices before and after irradiation up to a fluence of $5 \times 10^{15} \text{ n}_{\text{eq}} / \text{cm}^2$.

We will also report on the R&D activity to obtain Inter Chip Vias (ICVs) on the ATLAS read-out chip in collaboration with the Fraunhofer Institute EMFT. This step is meant to prove the feasibility of the signal transport to the newly created readout pads on the backside of the chips allowing for four side buttable devices without the presently used cantilever for wire bonding. The read-out chips with ICVs will be interconnected to thin pixel sensors, 75 μm and 150 μm thick, with the Solid Liquid Interdiffusion (SLID) technology, which is an alternative to the standard solder bump-bonding.

Author: MACCHIOLO, Anna (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D))

Co-authors: MOSER, Hans-Günther (Max-Planck-Institut für Physik); ANDRICEK, Laci (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D)); WEIGELL, Philipp (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D)); RICHTER, Rainer (MPI for Physics); Dr NISIUS, Richard (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D)); TERZO, Stefano (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D))

Presenter: MACCHIOLO, Anna (Max-Planck-Institut fuer Physik (Werner-Heisenberg-Institut) (D))

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