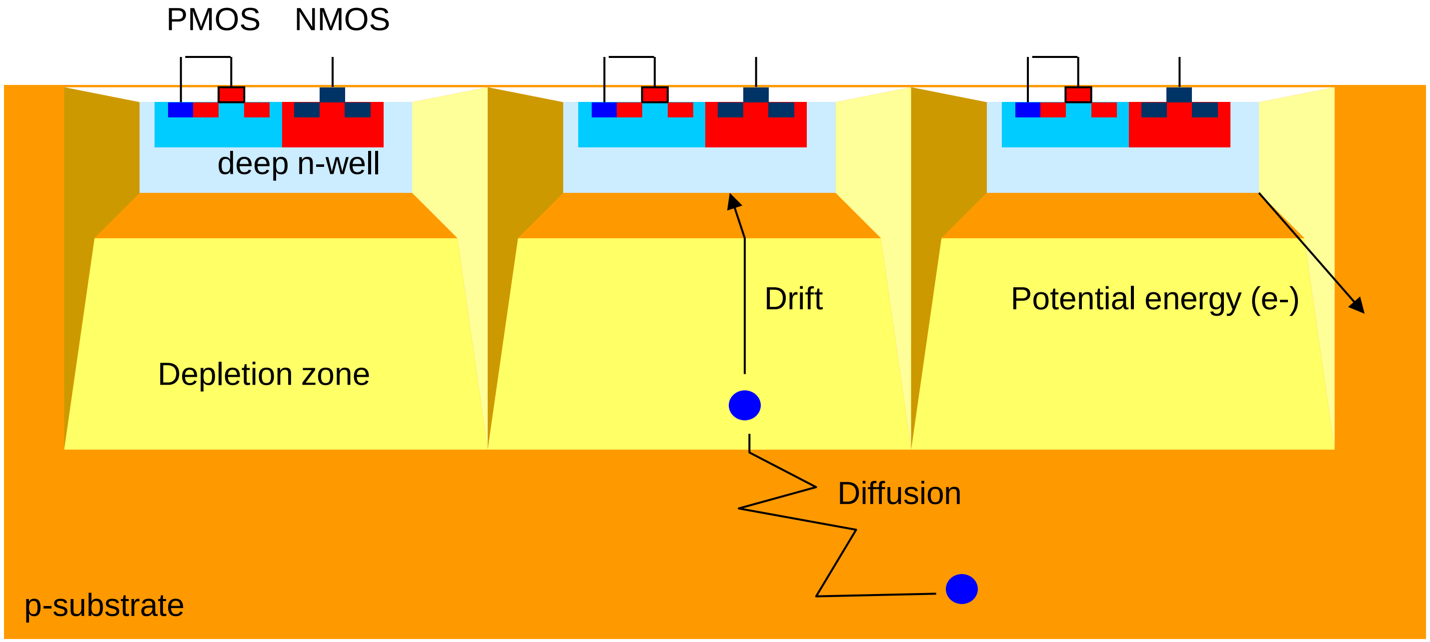
High-Voltage Pixel Sensors for ATLAS Upgrade

Ivan Peric
for HVCMOS collaboration

University of Heidelberg, Germany

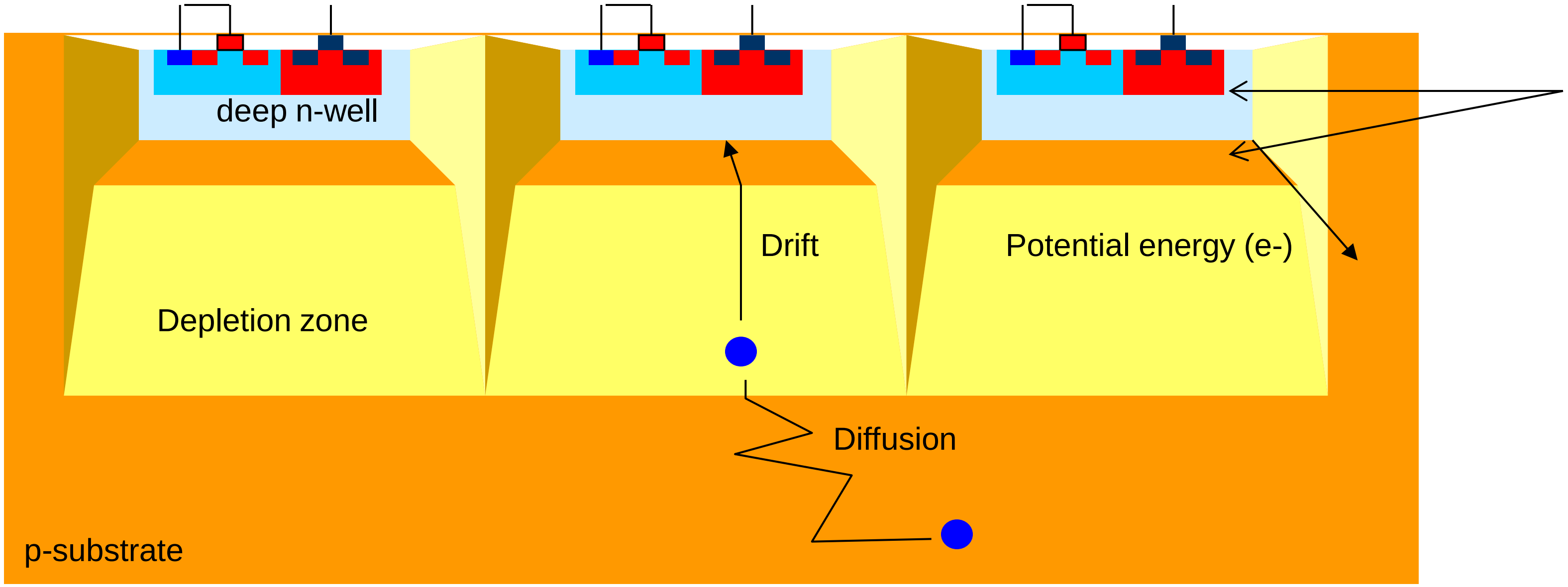
HVCMOS detectors

- HV CMOS detectors *(particle detectors in standard HV-CMOS technologies)* are depleted active pixel detectors
- Main charge collection mechanism is drift (certain signal part is collected by diffusion as well)
- Implemented in commercial CMOS (HV) technologies (350nm and 180nm)



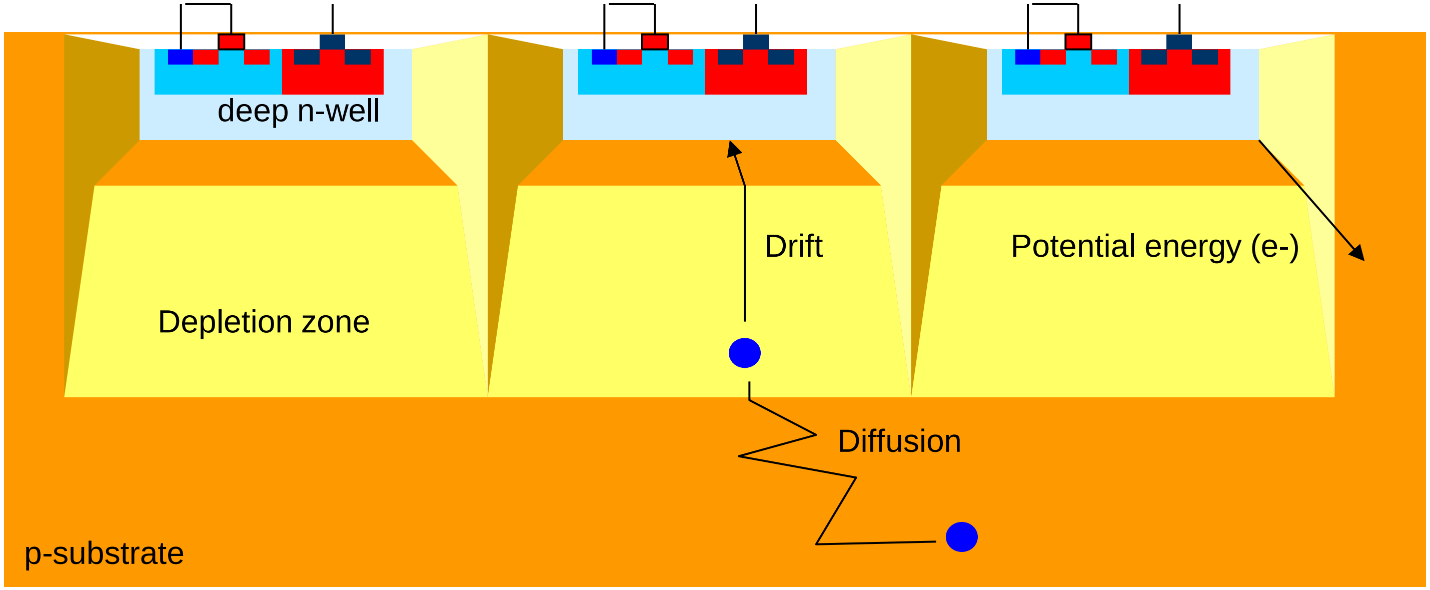
HVCMOS detectors

- Collection electrode is a deep-n-well in a p-substrate
- Pixel electronics is embedded in the n-well (PMOS: directly, NMOS in a P-well)
- Can be implemented in many commercial technologies (we tried also 65nm UMC CMOS); however the possibility to bias the n-well with a relatively high voltage is important
- Best properties offer HV CMOS technologies – the n-well is deep enough so that reverse voltages of up to ~120V can be used (no punch through between p-well and substrate)



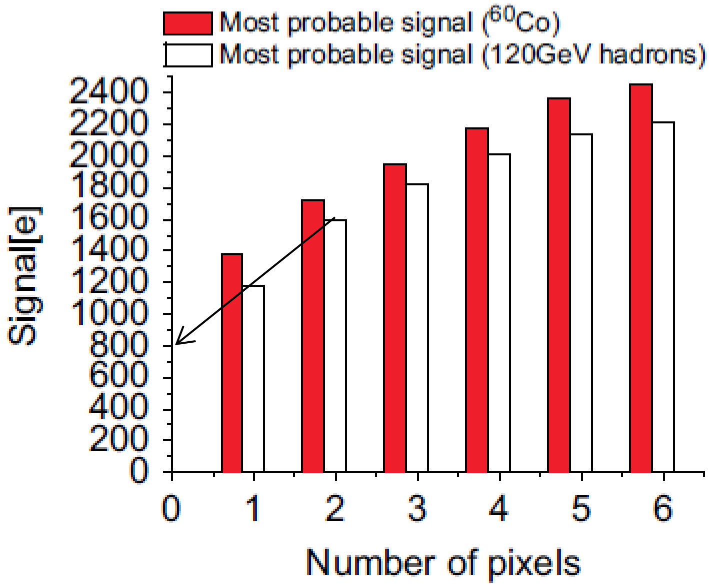
HVCMOS detectors

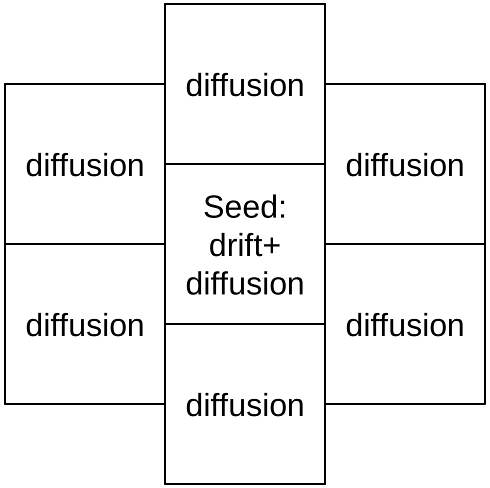
- Example for AMS: 20/10 Ωcm (350/180nm CMOS) substrate resistance -> acceptor density ~ 10^{15} cm^{-3}
- Depleted layer thickness estimation from the technology datasheet (area capacitance) for 60V bias (120 max): 10µm (350nm), 7µm (180nm)
- Typical measured MIP signal for a 50 µm x 50 µm pixel in AMS 0.35 µm (60V bias): 1800e (we estimate about 800e from depleted region and about 1000e by diffusion)



HVCMOS detectors

- Example for AMS: 20/10 Ωcm (350/180nm CMOS) substrate resistance -> acceptor density ~ 10^{15} cm^{-3}
- Depleted layer thickness estimation from the technology datasheet (area capacitance) for 60V bias (120 max): 10µm (350nm), 7µm (180nm)
- Typical measured MIP signal for a 50 µm x 50 µm pixel in AMS 0.35 µm (60V bias): 1800e (we estimate about 800e from depleted region and about 1000e by diffusion)




diffusion

diffusion

diffusion

Seed:
drift+
diffusion

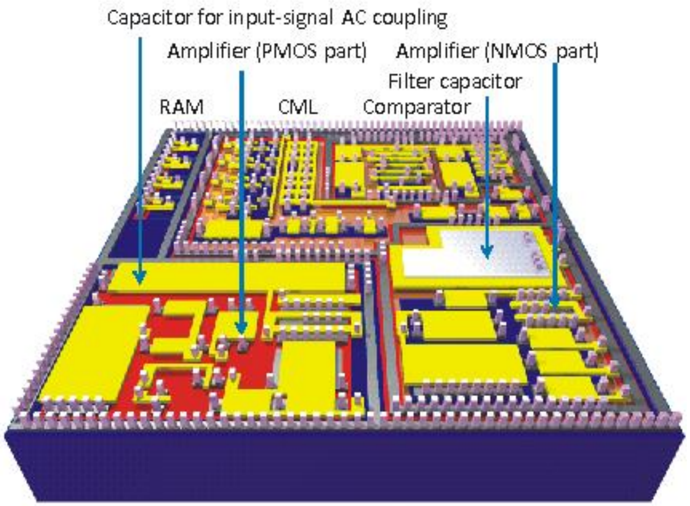
diffusion

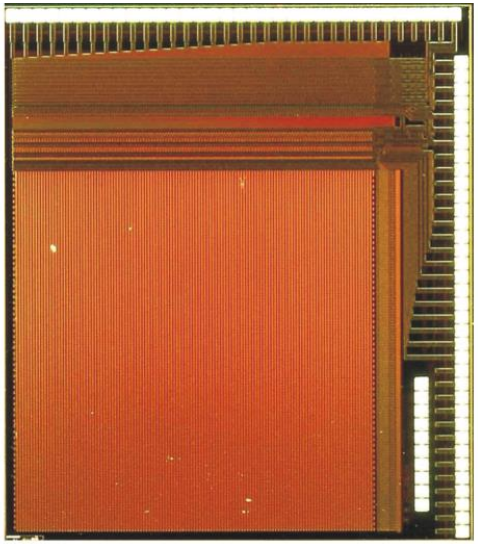
diffusion

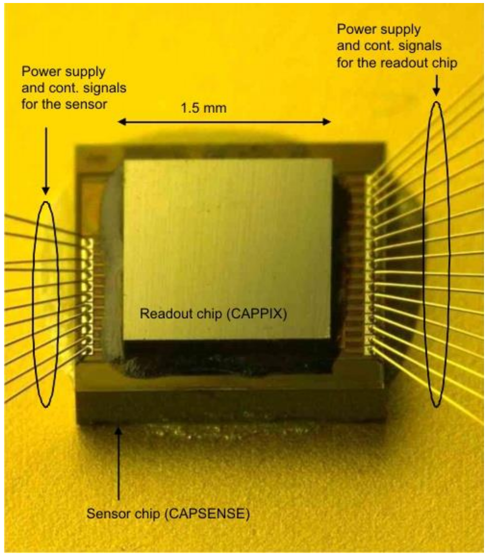
diffusion

Development in 350nm Technology

- Two development periods: 1) general development and 2) applications
- In 1) we used AMS 0.35µm technology
- Several prototypes have been designed
- Three detector types:
- A) Monolithic detector with intelligent CMOS pixels
- Pixel electronic is rather complex – CMOS based charge sensitive amplifier, usually discriminator, threshold tune…
- B) Monolithic detector with 4-PMOS-transistor pixel and rolling shutter RO
- C) Capacitively coupled hybrid detectors
- Good results, >98% efficiency in test-beam, high radiation tolerance

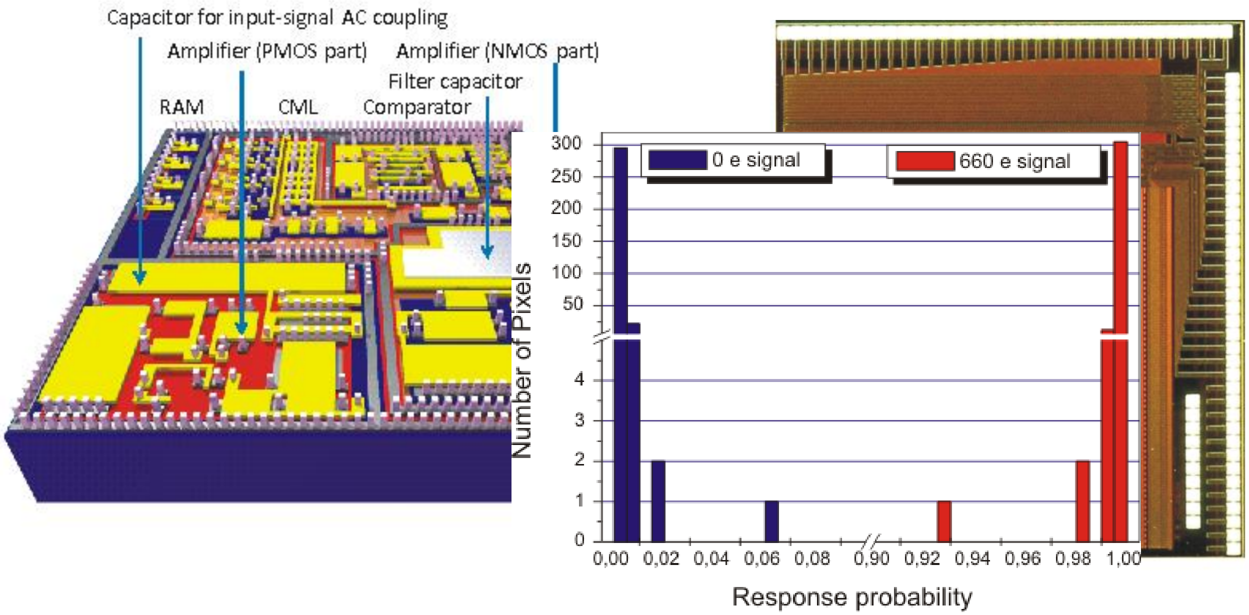


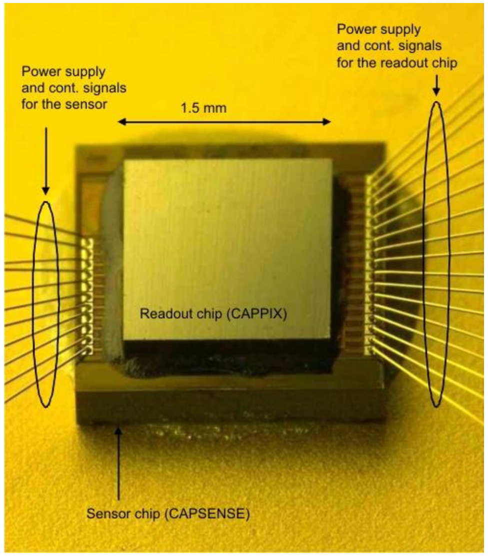




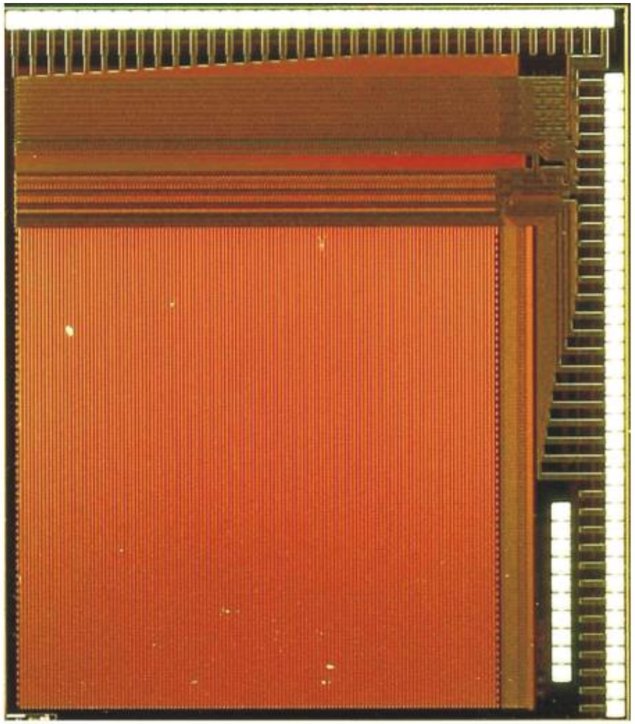
Development in 350nm Technology

- Two development periods: 1) general development and 2) applications
- In 1) we used AMS 0.35µm technology
- Several prototypes have been designed
- Three detector types:
- A) Monolithic detector with intelligent CMOS pixels
- Pixel electronic is rather complex – CMOS based charge sensitive amplifier, usually discriminator, threshold tune…
- B) Monolithic detector with 4-PMOS-transistor pixel and rolling shutter RO
- C) Capacitively coupled hybrid detectors
- Good results, >98% efficiency in test-beam, high radiation tolerance

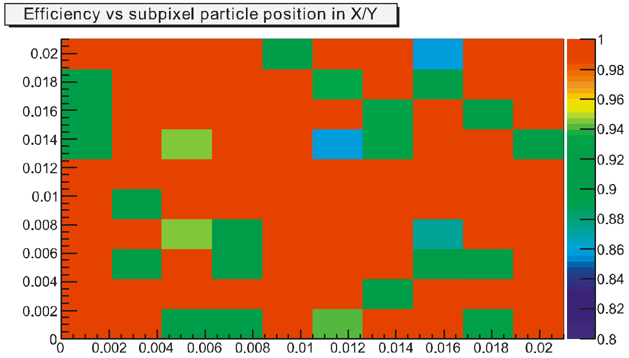




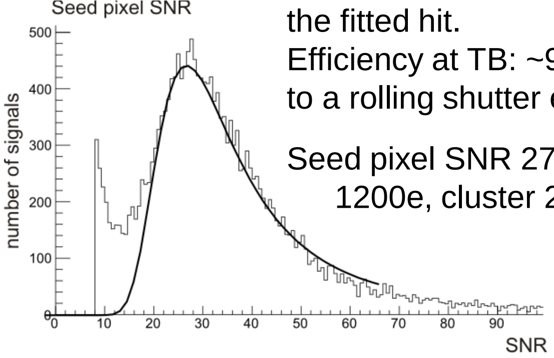
Test-Beam Results



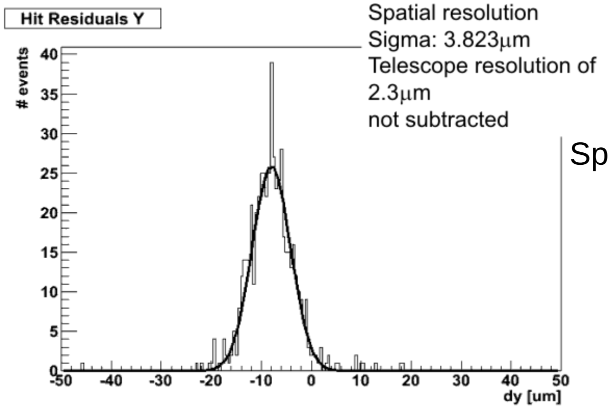
Simple (4T) integrating pixels with pulsed reset and rolling shutter RO
21x21 µm pixel size



Efficiency vs. the in-pixel position of the fitted hit.
Efficiency at TB: ~98% (probably due to a rolling shutter effect)



Seed pixel SNR 27, seed signal 1200e, cluster 2000e

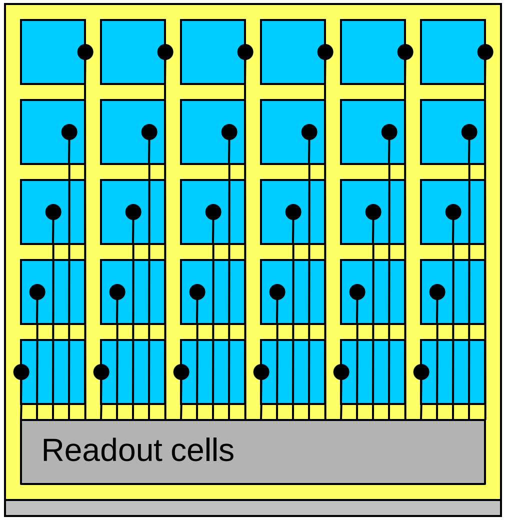


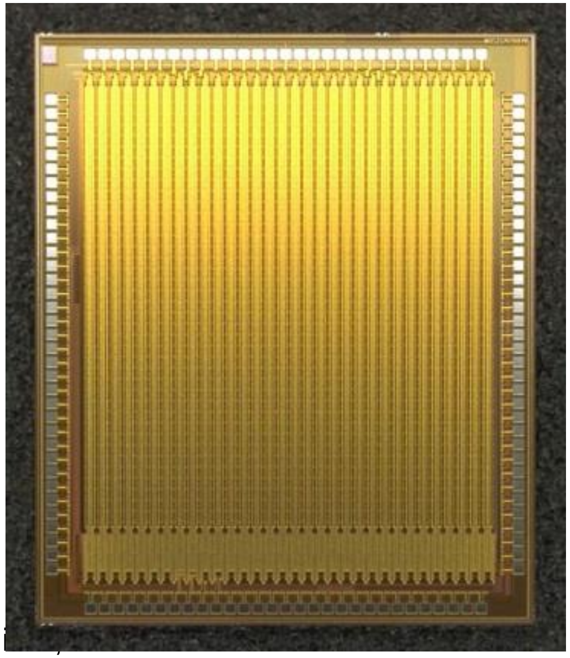
Spatial resolution
Sigma: 3.823µm
Telescope resolution of 2.3µm
not subtracted

Spatial resolution 3-3.8µm

Development for Mu3e Detector

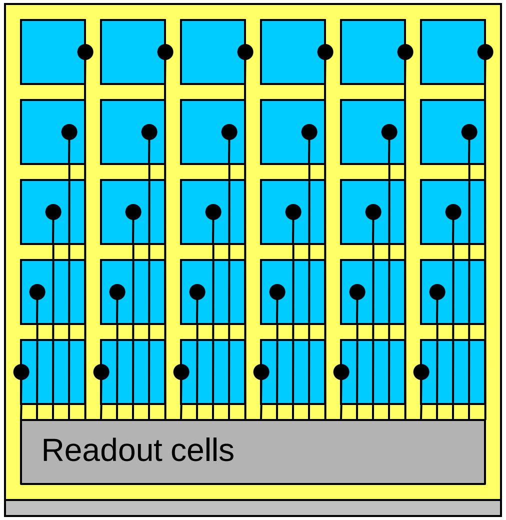
- The first applications of HVCMOS detectors will be the Mu3e experiment at PSI and the luminosity monitor for Panda experiment (GSI)
- 180nm HVCMOS technology chosen due to lower power consumption
- Low particle energy, thin detector required => monolithic pixel detector, thinned to 50µm
- Pixels contain only CSAs, every pixel connected to its readout cell, placed at the chip periphery, by an individual wire
- The concept is feasible for large pixels (80µm x 80µm)
- Advantages: minimal pixel capacitance, optimal SNR, separation of digital and analog circuits
- Disadvantage: inactive periphery (about 5%)
- Collaboration: Heidelberg PI and ZITI, PSI, ETH und University Zürich, University Geneva

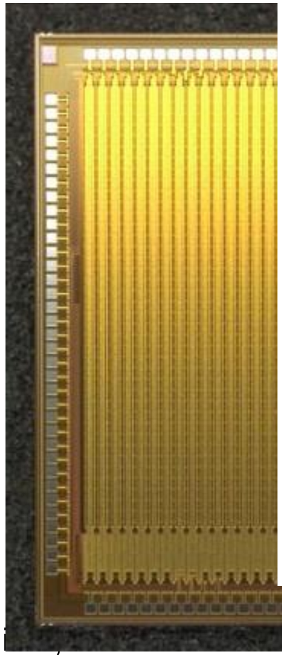


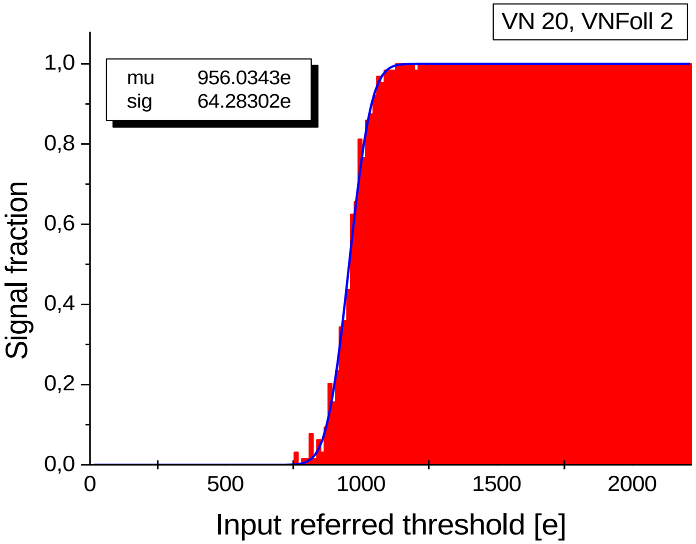


Development for Mu3e Detector

- The first applications of HVCMOS detectors will be the Mu3e experiment at PSI and the luminosity monitor for Panda experiment (GSI)
- 180nm HVCMOS technology chosen due to lower power consumption
- Low particle energy, thin detector required => monolithic pixel detector, thinned to 50µm
- Pixels contain only CSAs, every pixel connected to its readout cell, placed at the chip periphery, by an individual wire
- The concept is feasible for large pixels (80µm x 80µm)
- Advantages: minimal pixel capacitance, optimal SNR, separation of digital and analog circuits
- Disadvantage: inactive periphery (about 5%)
- Collaboration: Heidelberg PI and ZITI, PSI, ETH und University Zürich, University Geneva

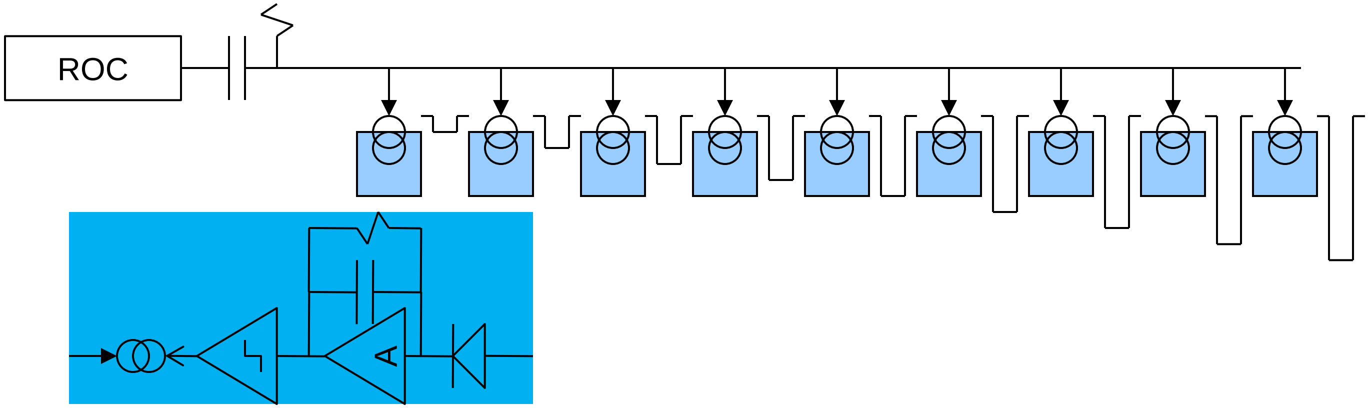






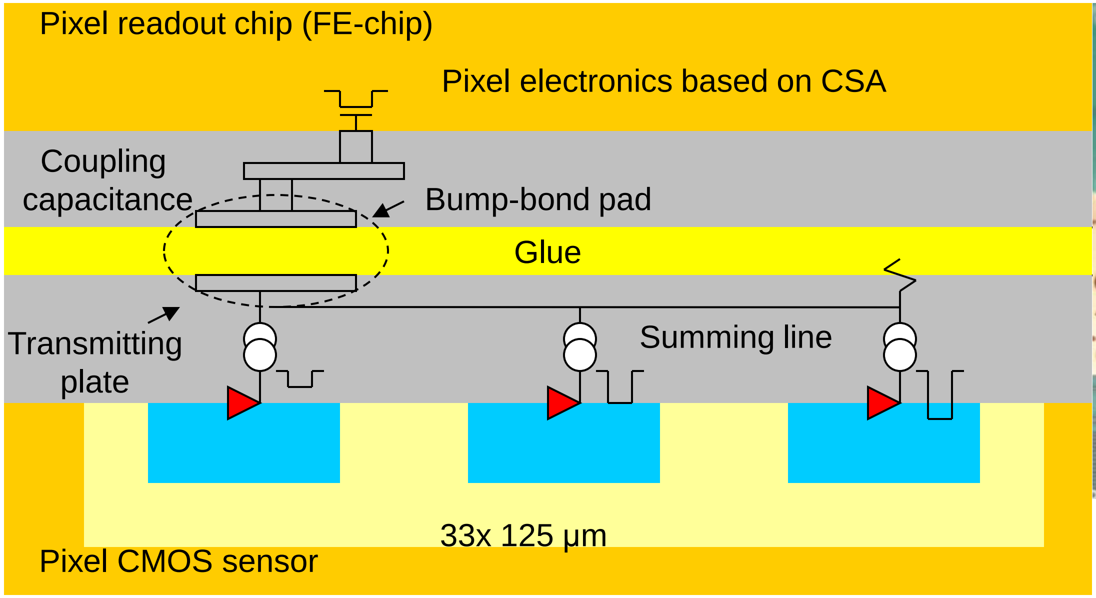
Development for ATLAS

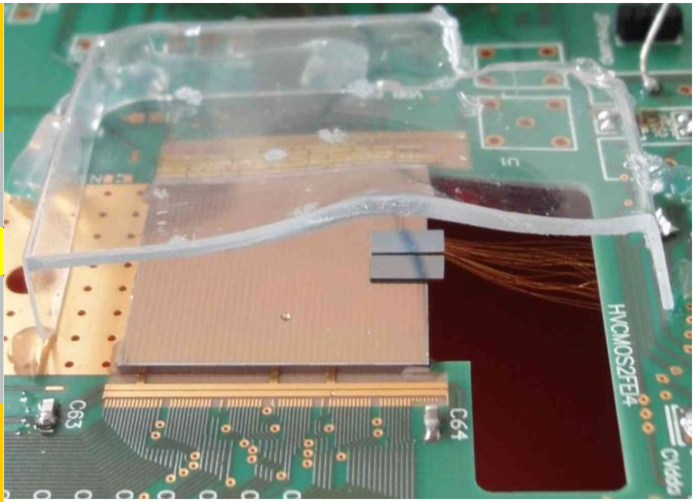
- Also the use in HL LHC ATLAS upgrade is investigated
- Concept: The use of active HVCMOS sensors as replacement for the standard strip- and pixel-sensors and the use of existing (or slightly modified) readout ASICs
- Group of pixels connected to one readout channel, address information is coded as signal amplitude
- Realization: one pixel contains: CSA, comparator, threshold tune circuit and the address generator
- Address signals of the grouped-pixels are summed and connected to the input of the RO-channel
- Collaboration: CPPM, CERN, Universities of Geneva, Bonn, Göttingen, Glasgow, Liverpool, Heidelberg, LBNL,…



Pixel Readout

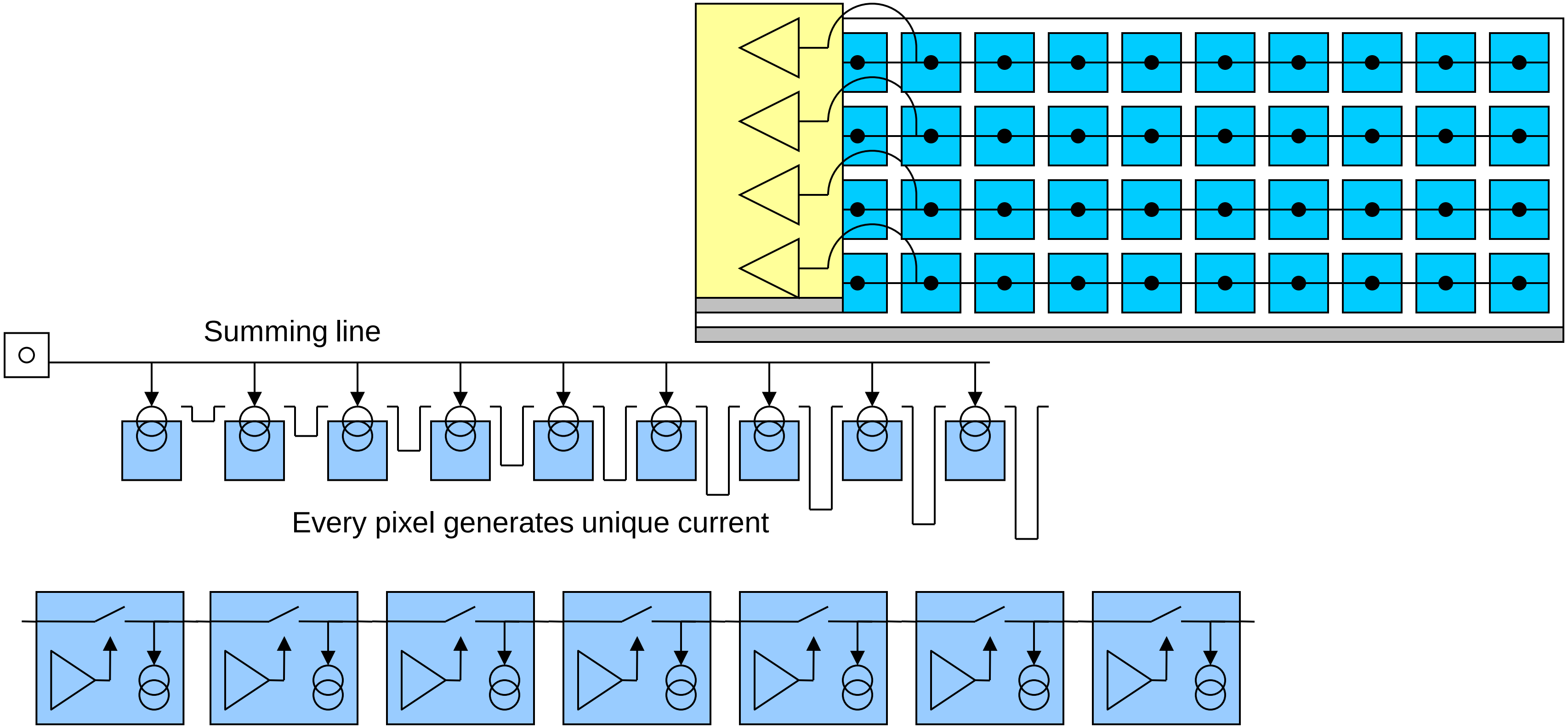
- Pixel readout: three pixels connected to one readout channel of the ATLAS FEI-chip (FEI4)
- Capacitive sensor-to-chip signal transmission, no need for bump bonds
- Advantages: smaller pixels, different pixel geometries can be combined with one ASIC (e.g. for the end caps), little material, fast readout, good resolution for large incident angles





Strip Readout

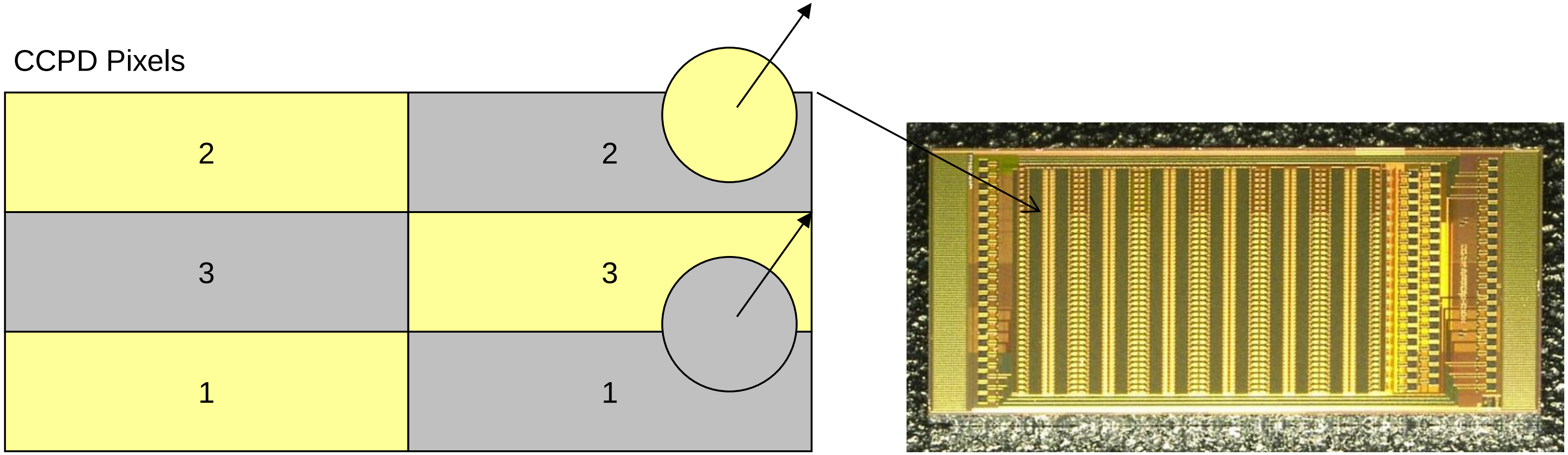
- Strip readout: larger number of pixels (e.g. 100) grouped into segmented strips, readout with an amplitude sensitive strip-readout chip (multichannel chip)
- Advantages: Pixel detector (nxn pixels) is readout with a relatively small number of analog channels (~n) – in contrast to rolling shutter readout, time resolution is high
- Less material than in the case of the hybrid pixel detector and a similar time resolution.
- If summing scheme can cope with two simultaneous hits, the concept can work at relatively high occupancies (e.g. 8 particles / cm^2 / 25ns)



Experimental Results

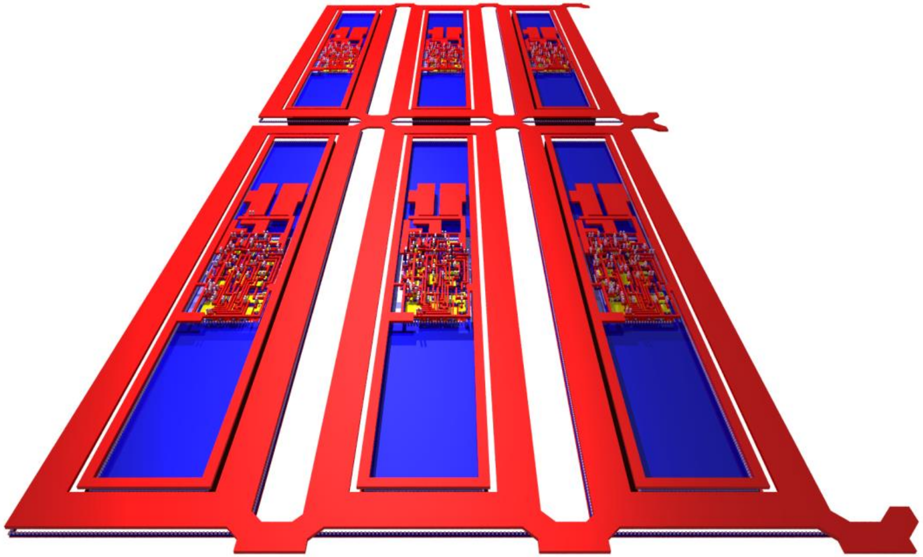
- Results of the project
- A small detector prototype chip “CCPD” has been designed
- CCPD can be readout with both a strip- and a pixel-readout chip
- Stand-alone readout is also possible
- Two chip iterations
- 1) optimized for small noise
- 2) optimized for radiation tolerance

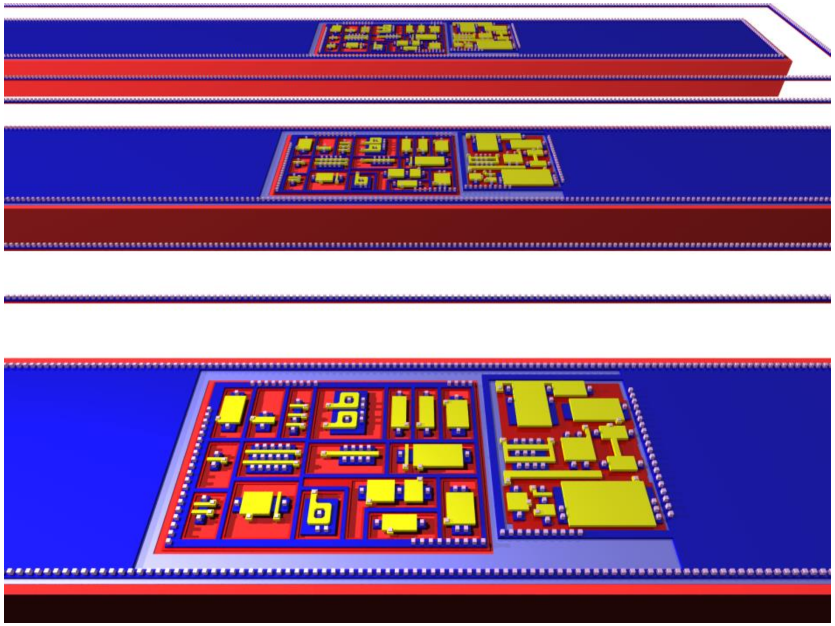
CCPD Pixels



Experimental Results

- Results of the project
- A small detector prototype chip “CCPD” has been designed
- CCPD can be readout with both a strip- and a pixel-readout chip
- Stand-alone readout is also possible
- Two chip iterations
- 1) optimized for small noise
- 2) optimized for radiation tolerance



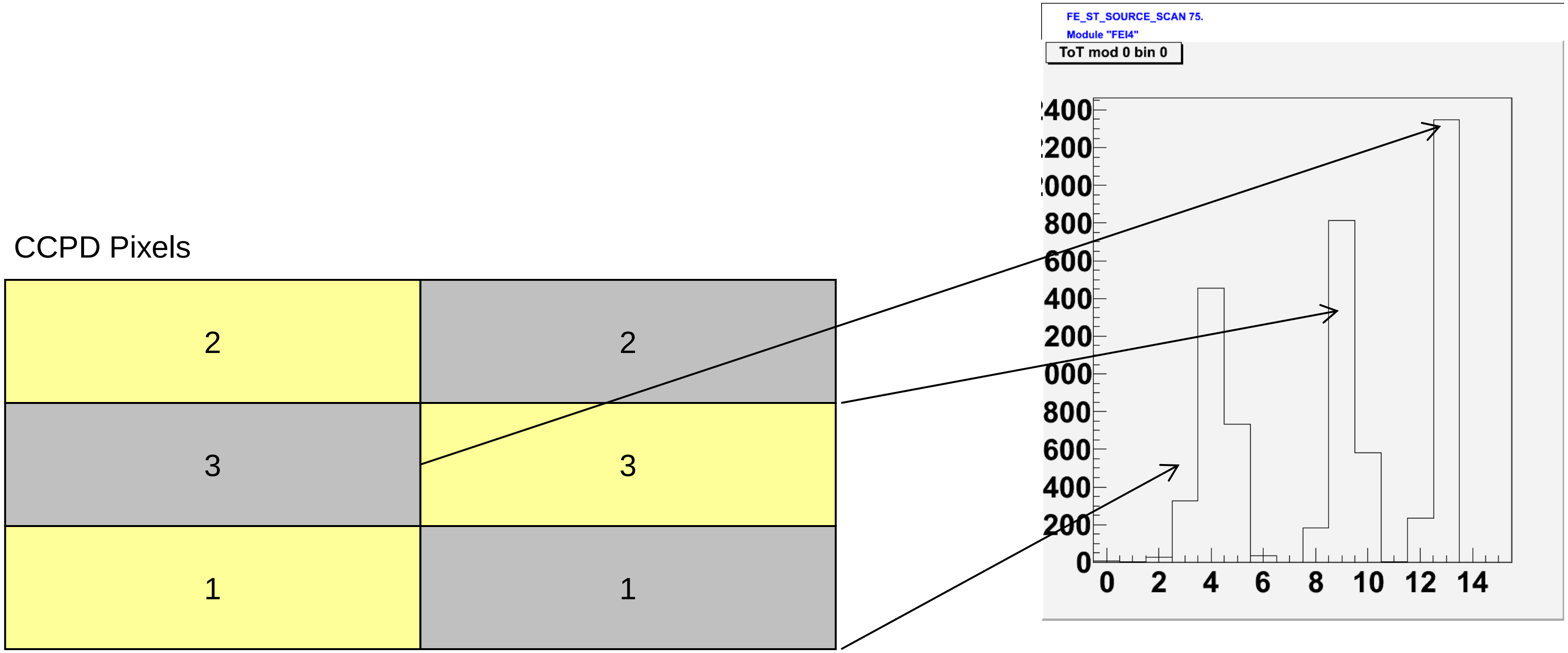


Experimental Results

- Three testing programs:
- 1) Test in standalone modus: a) lab tests with electric signals (using charge injection circuit) and b) measurements with radioactive sources. Goals: functionality tests, measurements of noise, threshold dispersion, and the MIP signal amplitude
- 2) Irradiations
- 3) Tests with pixel readout chip (it works - three addresses can be distinguished, first testbeam measurement done, time stamp distribution ok => good time resolution)
- 4) Tests with strip readout chip (still to be done)

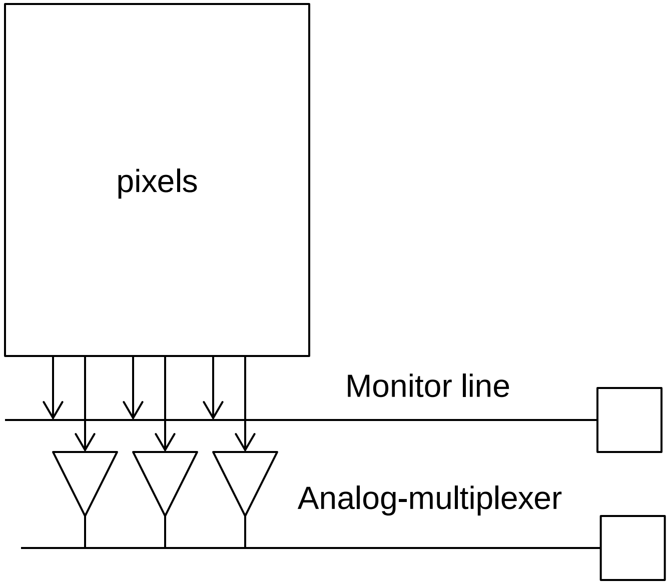
Signal amplitudes measured by FEI4

CCPD Pixels



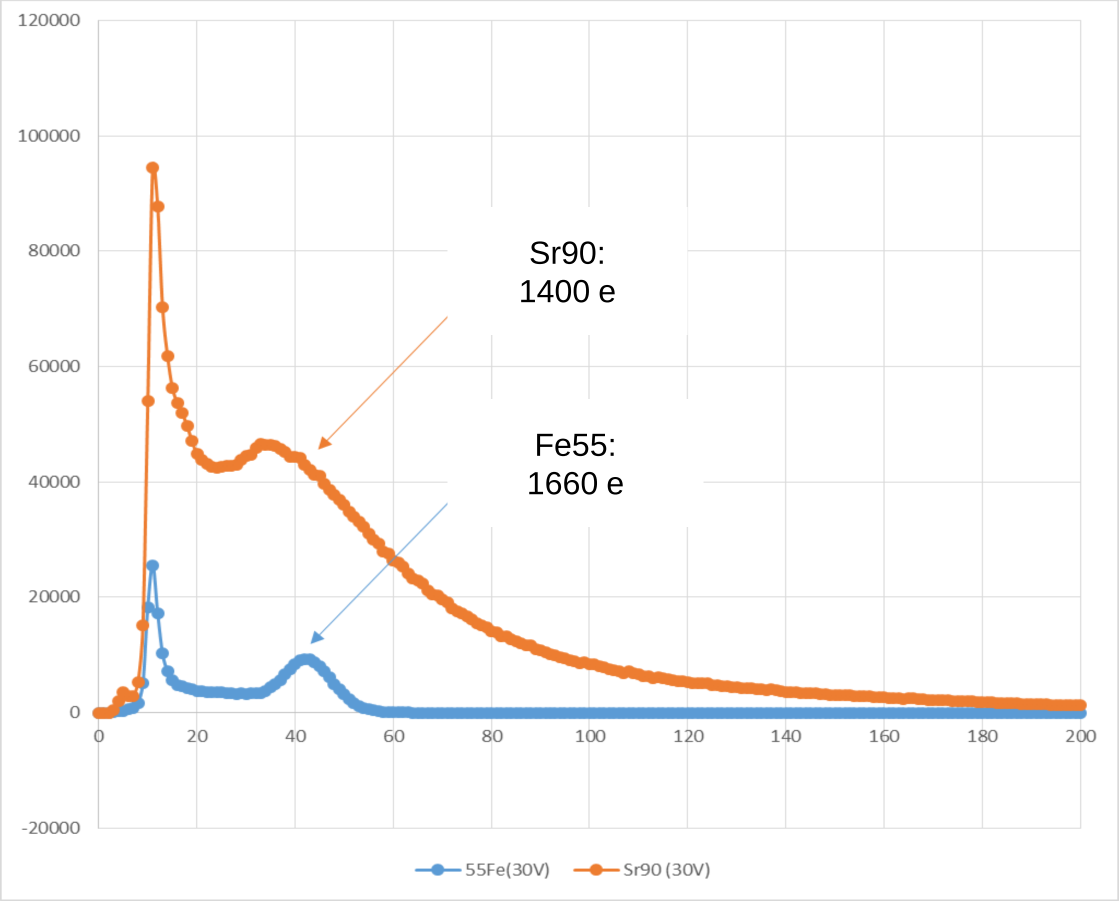
Standalone Tests

- Test in the standalone mode:
- Pixel addresses connected to a monitor line that can be accessed from outside via single IO pad
- Several CSA outputs can be measured directly – allows spectral measurements



MIP Signal

- Several CSA outputs can be measured directly – allows spectral measurements
- Measured Sr-90 MPW signal at rather low 30V bias voltage (maximal 120V) ~1350e (we estimate 400e from depleted region **at 30V** – diffusion part 950e)
- Estimated MIP signal for 60V bias: 1500e

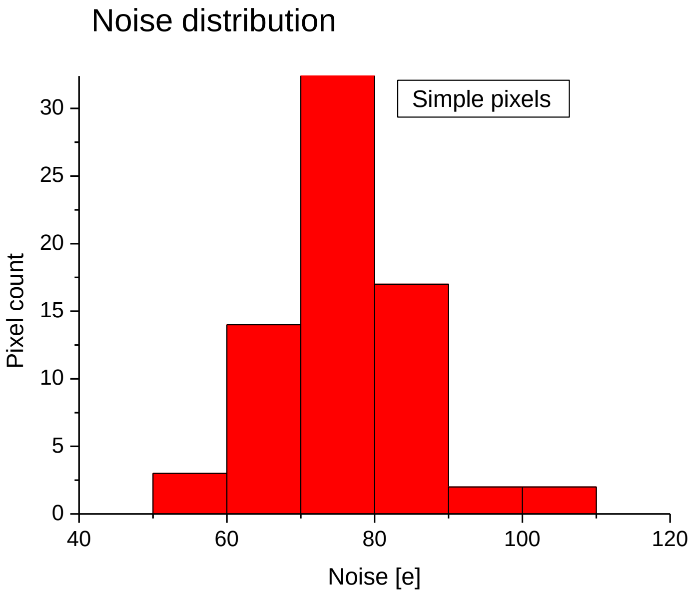


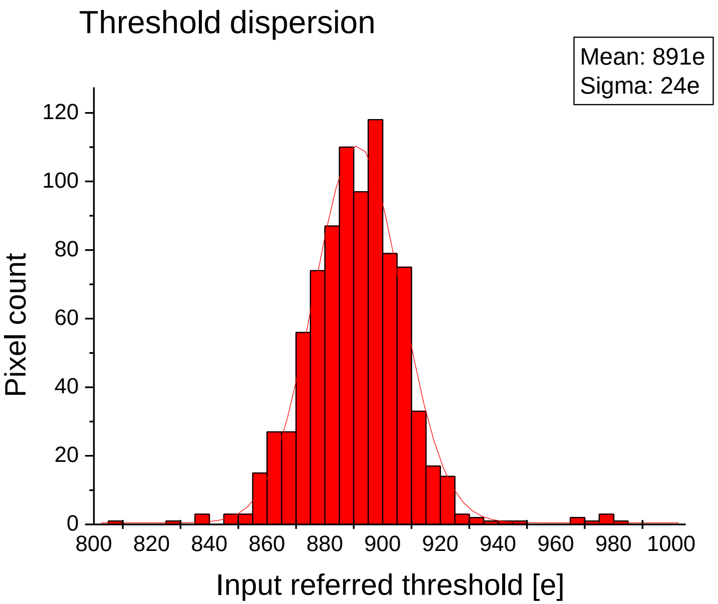
Sr90:
1400 e

Fe55:
1660 e

Noise and Threshold Dispersion

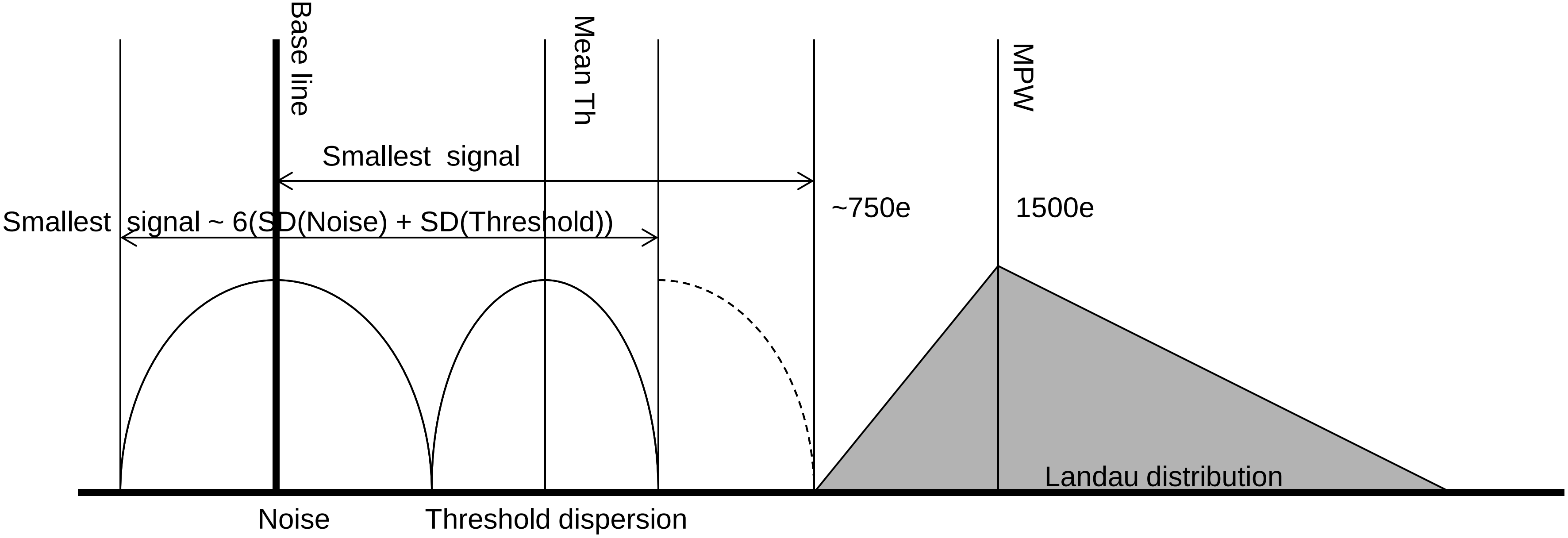
- Threshold and injection scans – noise, threshold dispersion
- Results for CCPD2 optimized for radiation hardness (not for low noise)
- Average pixel noise ~ 75e (large spread)
- Threshold tuning: dispersion ~ 25e
- Estimated MIP signal at 60V: 1500e





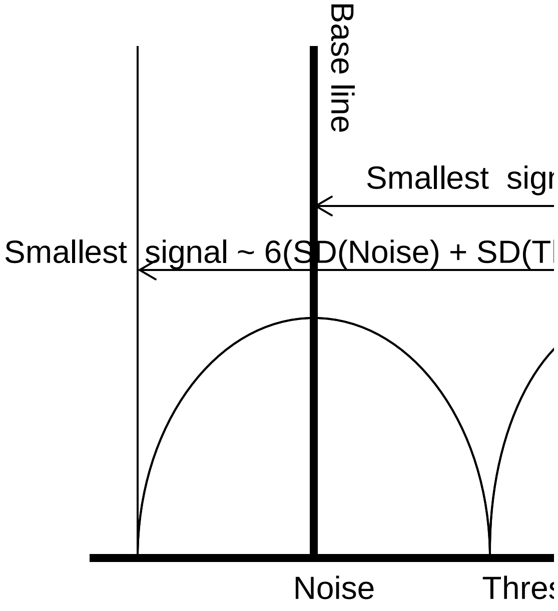
Noise and Threshold Dispersion

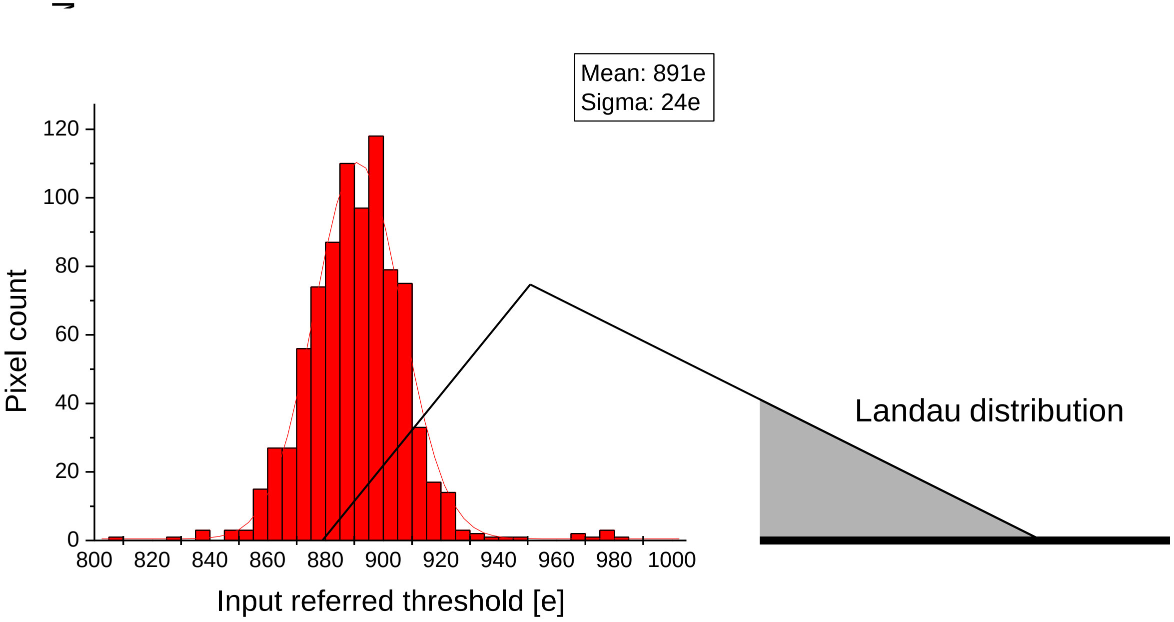
- Average pixel noise ~ 75e (large spread)
- Threshold tuning: dispersion ~ 25e
- Estimated MIP signal at 60V: 1500e
- Required:
- 6 x SD(Noise) + 6 x SD(Threshold) = Smallest signal
- 6 x SD(Noise) + 6 x SD(Threshold) = 600e
- Question: what is the smallest signal for a MPW of 1500e? (probably ~ 1500/2 = 750 e)



Noise and Threshold Dispersion

- Average pixel noise ~ 75e (large spread)
- Threshold tuning: dispersion ~ 25e
- Estimated MIP signal at 60V: 1500e
- Required:
- 6 x SD(Noise) + 6 x SD(Threshold) = Smallest signal
- 6 x SD(Noise) + 6 x SD(Threshold) = 600e
- Question: what is the smallest signal for a MPW of 1500e? (probably ~ 1500/2 = 750 e)
- In theory ok, but we still need to improve threshold tuning, so far we achieved a mean value of ~800e, 400e is required





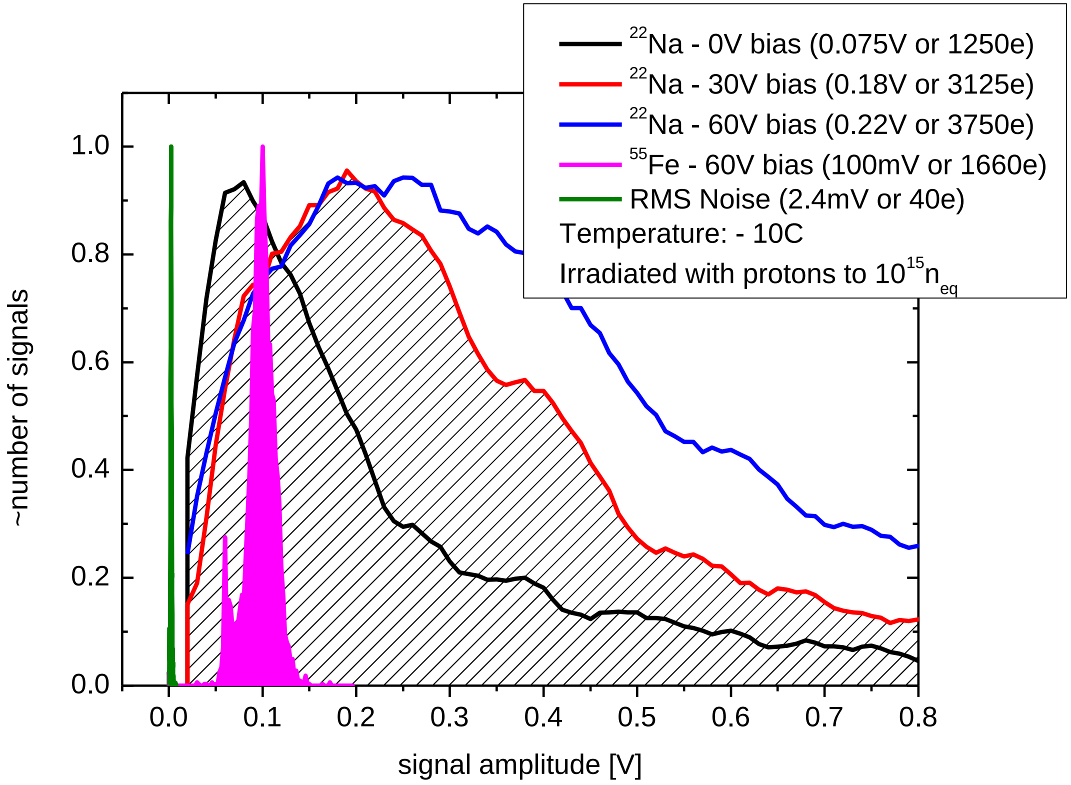
Irradiations – older Results

- Irradiation studies:
- Two damage mechanisms: nonionizing and ionizing
- Results are generally promising, but we still do not have the results from a test-beam measurement with irradiated devices
- Older results (AMS 0.35µm technology)
- X-ray irradiation up to 60 Mrad (rad-hard device layout – enclosed transistors, chip on during irradiation) – increased noise and leakage current observed - after annealing and cooling they return to normal noise

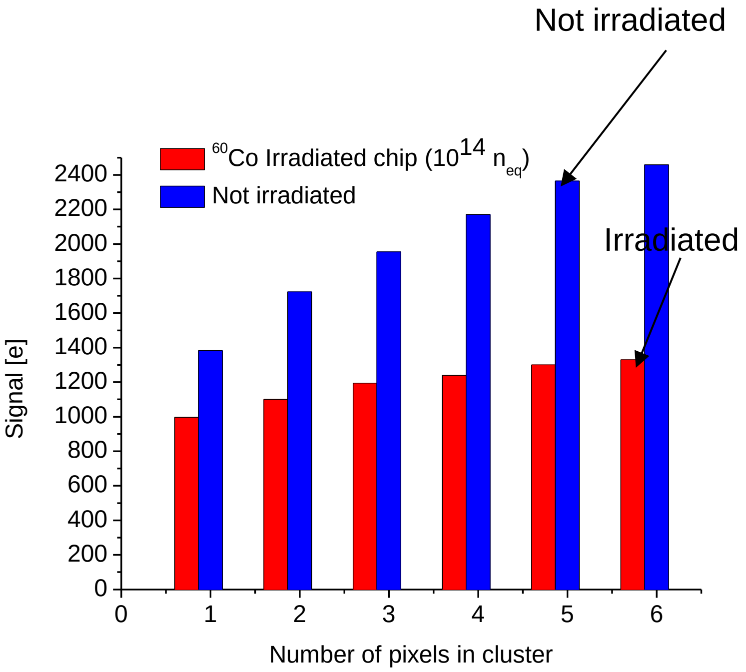
Irradiations – older Results

- Older results:
- Proton irradiation to 10^{15} neq/cm^2 (standard device layout, chip off during irradiation) – increased leakage and noise – the MIP signal does not decrease significantly – diffusion still works?
- Neutron irradiation to 10^{14} neq/cm^2 (rolling shutter chip) – increased leakage and noise – diffusion part of the signal is decreased

Proton irradiation

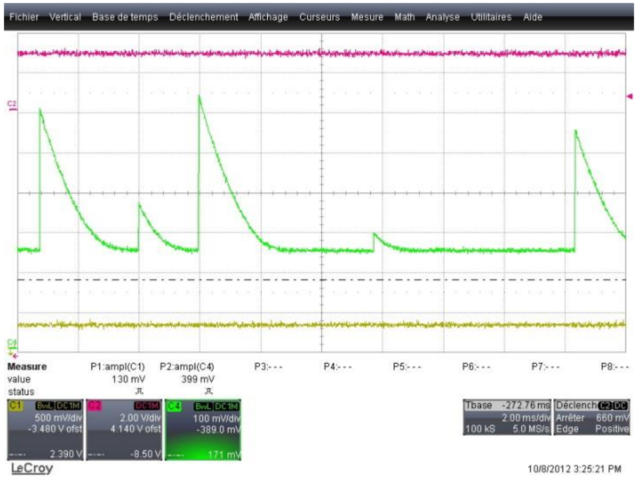


Neutron irradiation



Irradiations – CCPD1

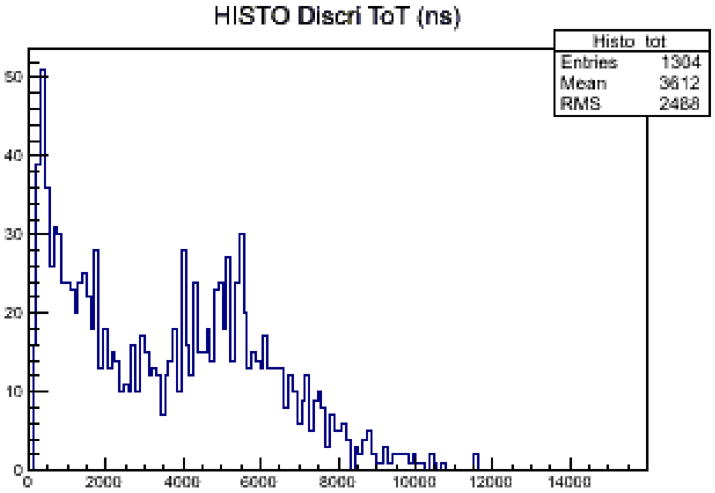
- 1) Two sets of detectors have been irradiated to 435 Mrad and 80 Mrad with protons at the PS (CERN) (chips on during irradiation)
- 2) X-ray irradiation to 50 Mrad (chips on during irradiation)
- 3) Neutron irradiation to 10^{16} neq/cm^2 (chips off during irradiation, only nonionizing damage)
- Influence of ionizing radiation higher than expected. Despite of that, Sr-90 spectrum can be measured after 80Mrad (proton irradiation)



```
Measure   P1:ampl(C1)  P2:ampl(C4)  P3:---  P4:---  P5:---  P6:---  P7:---  P8:---
value          130 mV       399 mV
status

C1 BwL DC1M     C2 DC1M        C4 BwL DC1M      Tbase  -272.76 ms   Déclench C2 DC
 500 mV/div      2.00 V/div     100 mV/div              2.00 ms/div Arrêter  660 mV
-3.480 V ofst   4.140 V ofst   -389.0 mV        100 kS   5.0 MS/s   Edge    Positive
     2.390 V        -8.50 V       171 mV
                                                10/8/2012 3:25:21 PM
```

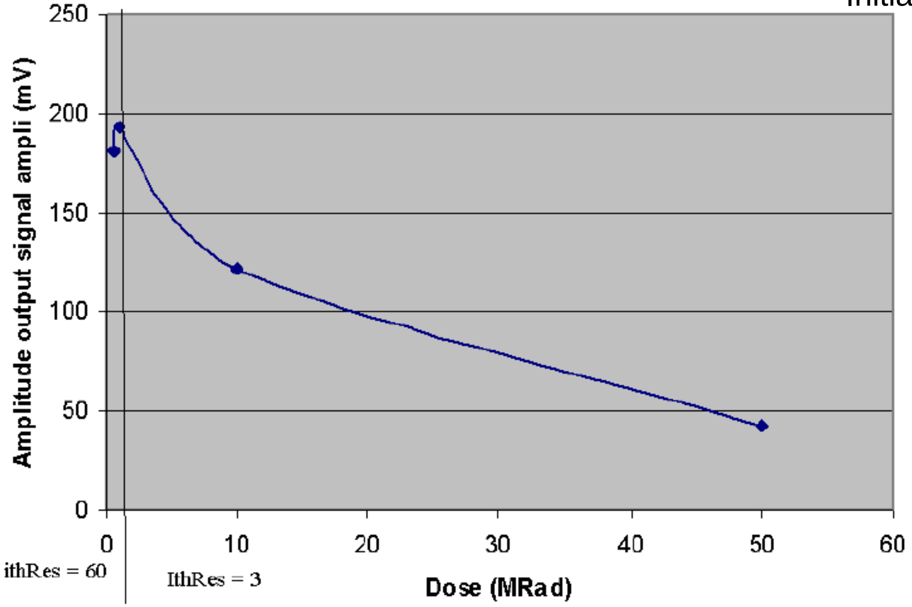
CCPD1 at 380 Mrad (810^{15} n$_{eq}$) proton-irradiation
Beam signals



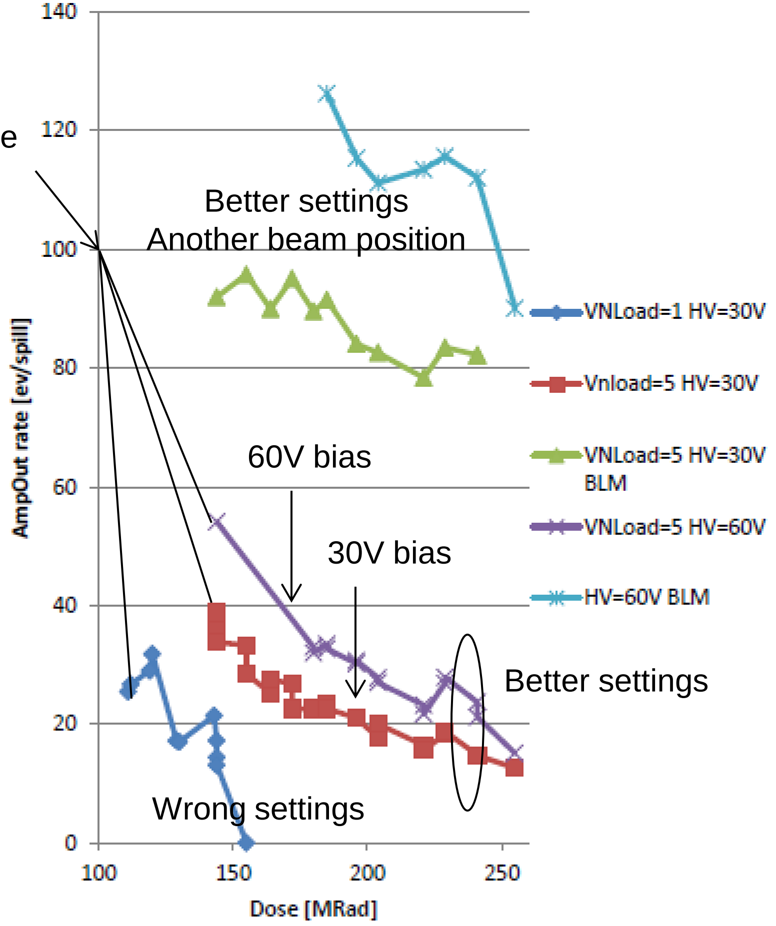
CCPD1 irradiated to 80 Mrad with protons
Sr-90 spectrum

Irradiations – CCPD1

- Chips were affected by x-ray irradiation (ionizing) strongly - large amplifier gain drop
- The chip irradiated to 435 Mrad works (responds to test signals), but particle signals can not be distinguished from noise after about 380 Mrad (gain drop too high – high threshold, large leakage, activation, cooling not possible)



CCPD1 irradiated with x-rays
Amplifier gain loss



Initial rate

Better settings
Another beam position

60V bias

30V bias

Better settings

Wrong settings

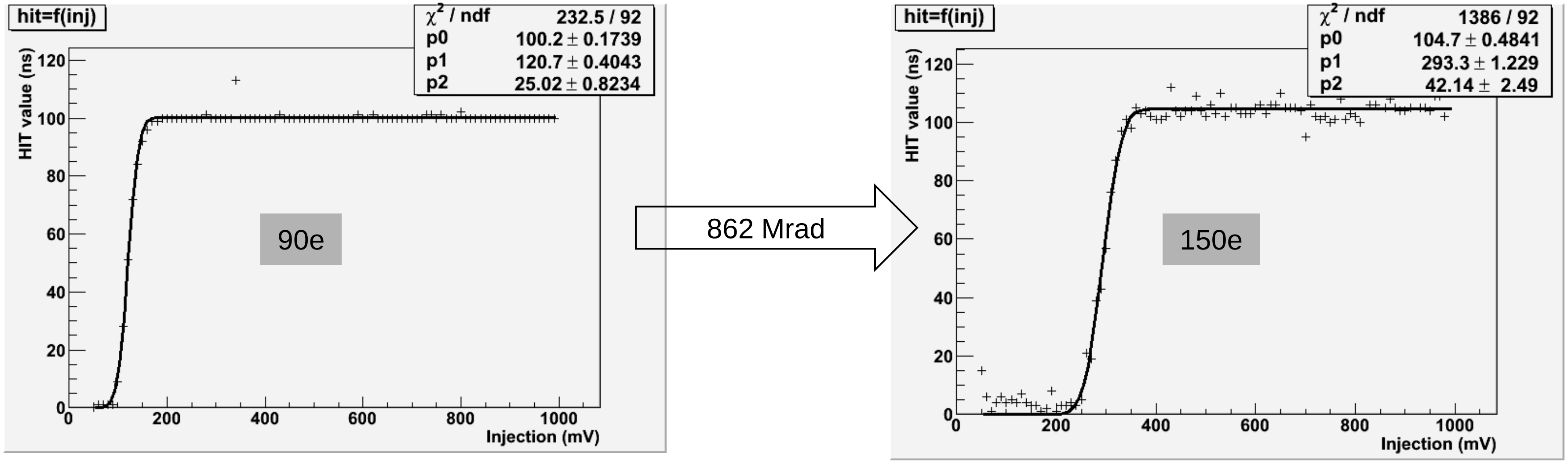
CCPD1 irradiated to with protons
Count rate

Irradiations – CCPD1

- The detector irradiated with neutrons (10^{16} neq/cm^2) works (capacitively readout by FEI4), particles can be clearly detected at the room temperature, testbeam measurement has been done and will give us the rough estimation about the efficiency (setup is not optimized – e.g. no threshold tuning done)

CCPD2: X-Ray Irradiation to 862 Mrad

- Several weak points in design have been identified that cause CCPD1 to be susceptible to ionizing radiation (symptoms are: gain drop and base line shift)
- The weak pints have been fixed in CCPD2 (at expense of a slightly higher noise)
- CCPD2 implements three pixel types, fully rad hard, partially rad hard and a simple pixel that uses positive feedback and has a CMOS comparator
- A detector has been irradiated to 862 Mrad with x-rays. (chips on during the irradiation, 2 hours of annealing at 70C after each 100Mrad)
- Result for one partially rad hard pixel: input referred noise before irradiation 25mV (90 e)
- Input referred noise after irradiation 40mV (150 e) at room temperature
- We observe that amplifiers work with reduced bias current (2µA instead of 5µA) – probably only partially rad hard pixels are affected – bias NMOS diode can be affected by oxide charge

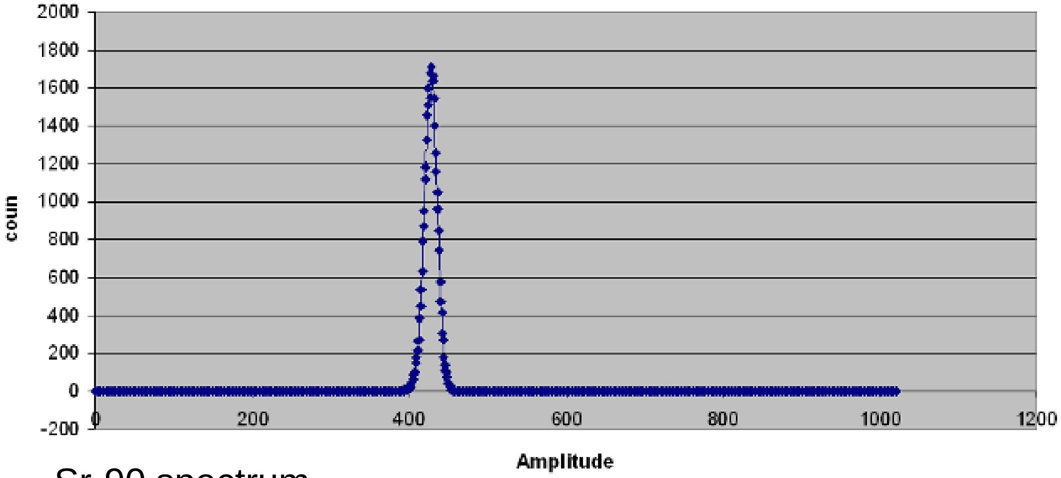


CCPD2: X-Ray Irradiation to 862 Mrad

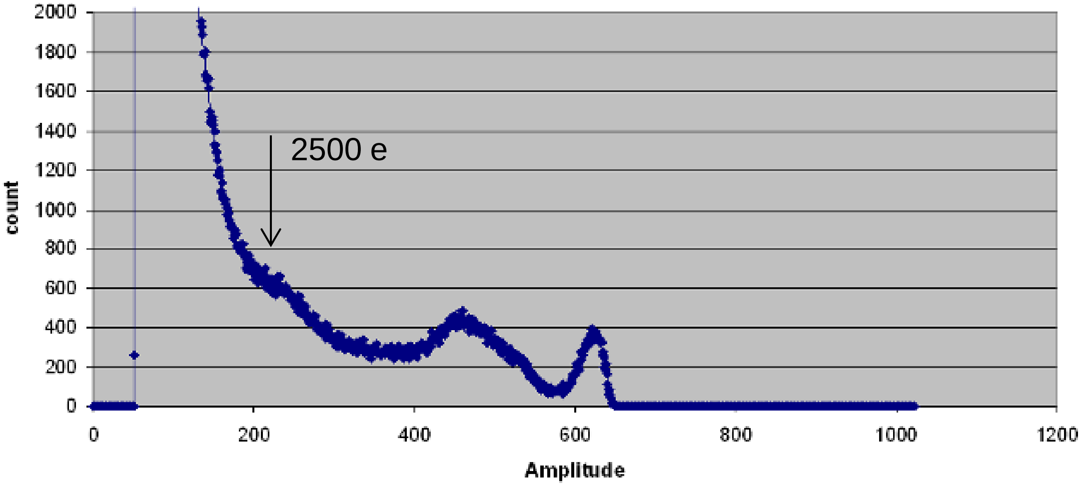
- The noise increase can be addressed to
- 1) Gain drop (by factor of two for the pixel)
- 2) Bias current drop (2µA instead of 5µA per amplifier) (under this condition we would have only 48 mA preamp current consumption per cm^2 detector area)
- 3) HV leakage current

CCPD2: X-Ray Irradiation to 862 Mrad

- Sr-90 spectra have been recorded before and after irradiation - no sign of signal loss at sensor
- 1V Injection (5000 e): 430 mV



- Sr-90 spectrum

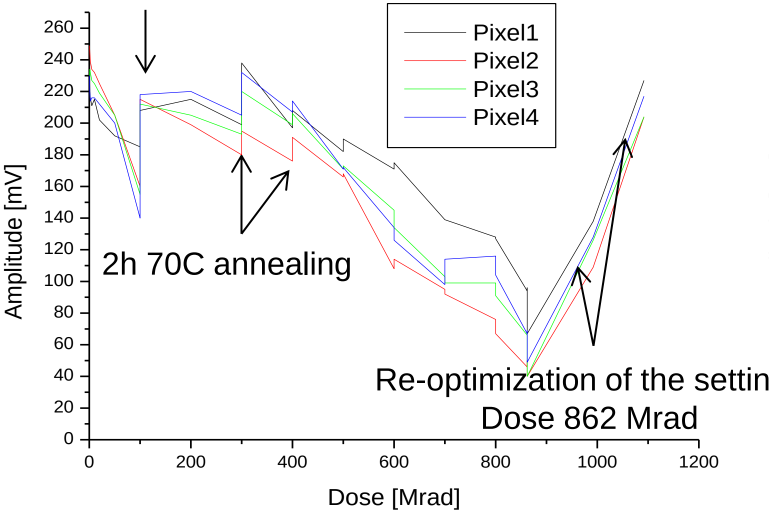


CCPD2: X-Ray Irradiation to 862 Mrad

- Several effects are still not understood
- The cause of the gain drop
- Several possibilities:
- Observed drop in the amplifier bias current
- Possible decrease of the feedback resistance, due to ionizing damage in the feedback transistor => shaping time decrease
- Notice that the fully rad hard pixels are not significantly affected

Fully rad-hard pixels

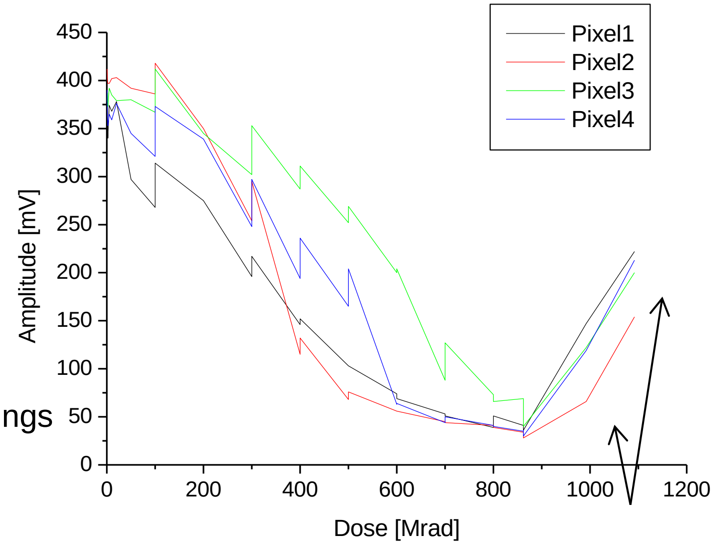
10 days annealing



2h 70C annealing

Re-optimization of the settings
Dose 862 Mrad

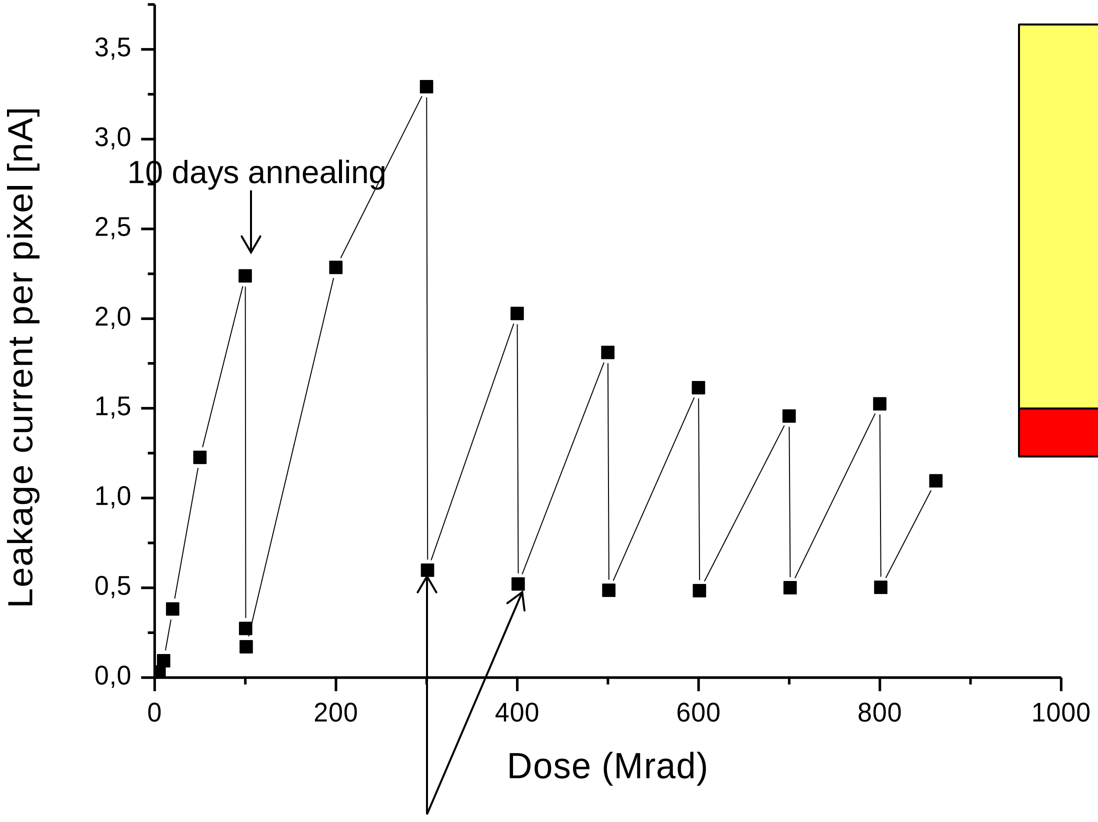
Partially rad-hard pixels



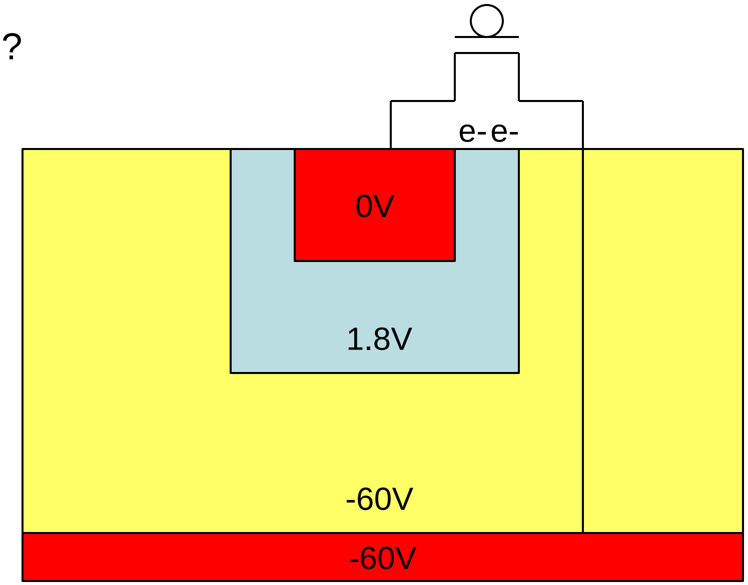
Re-optimization of the settings
Dose 862 Mrad

CCPD2: X-Ray Irradiation to 862 Mrad

- Several effects are still not understood
- The origin of HV leakage current
- The current gets higher for lower (!) n-well voltage
- Parasitic PMOS? trapping of electrons in SiO2?
- Injection of holes into n-well and their flow to p-substrate?
- Tunneling of trapped holes from SiO2 to substrate?



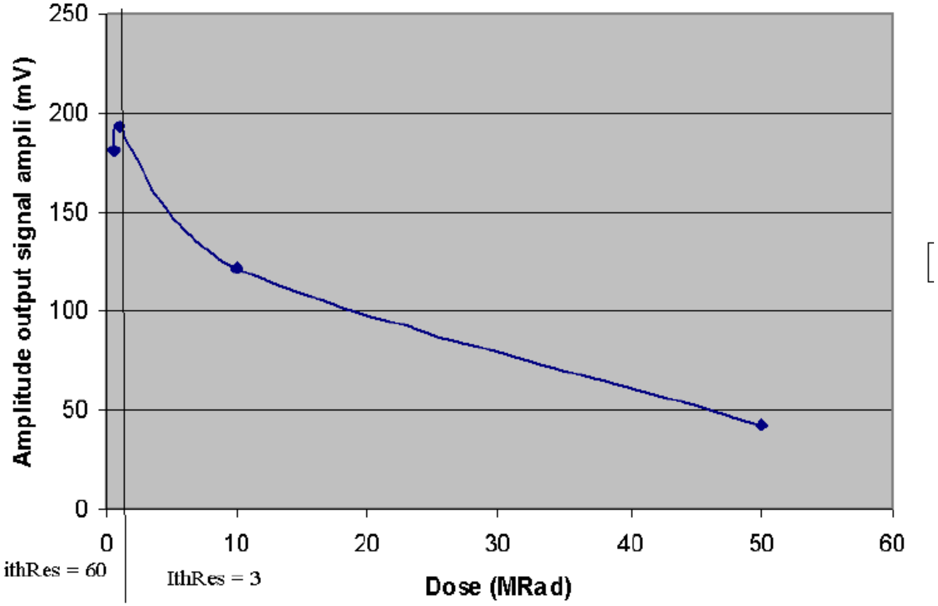
2h 70C annealing

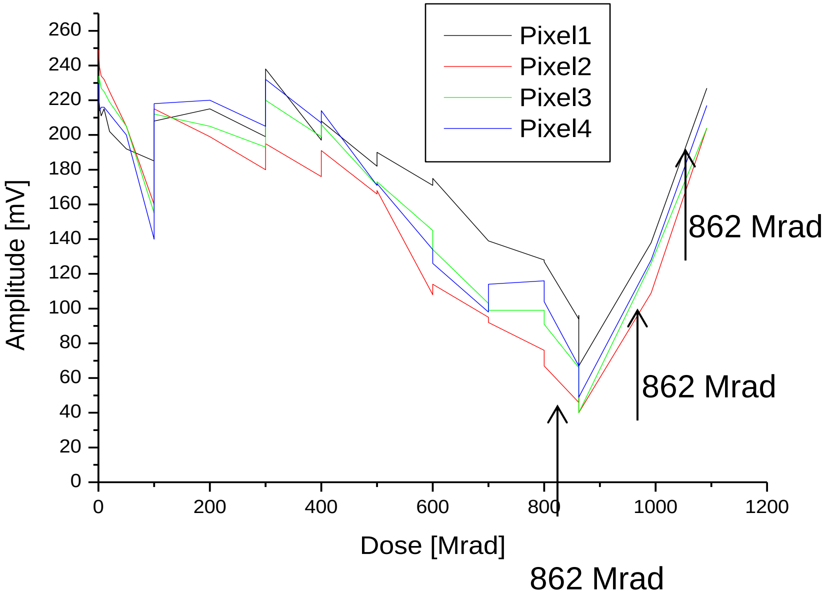


Possible cause of leakage current?

CCPD2: X-Ray Irradiation to 862 Mrad

- The radiation hardening measures done for CCPD2 seem to be successful



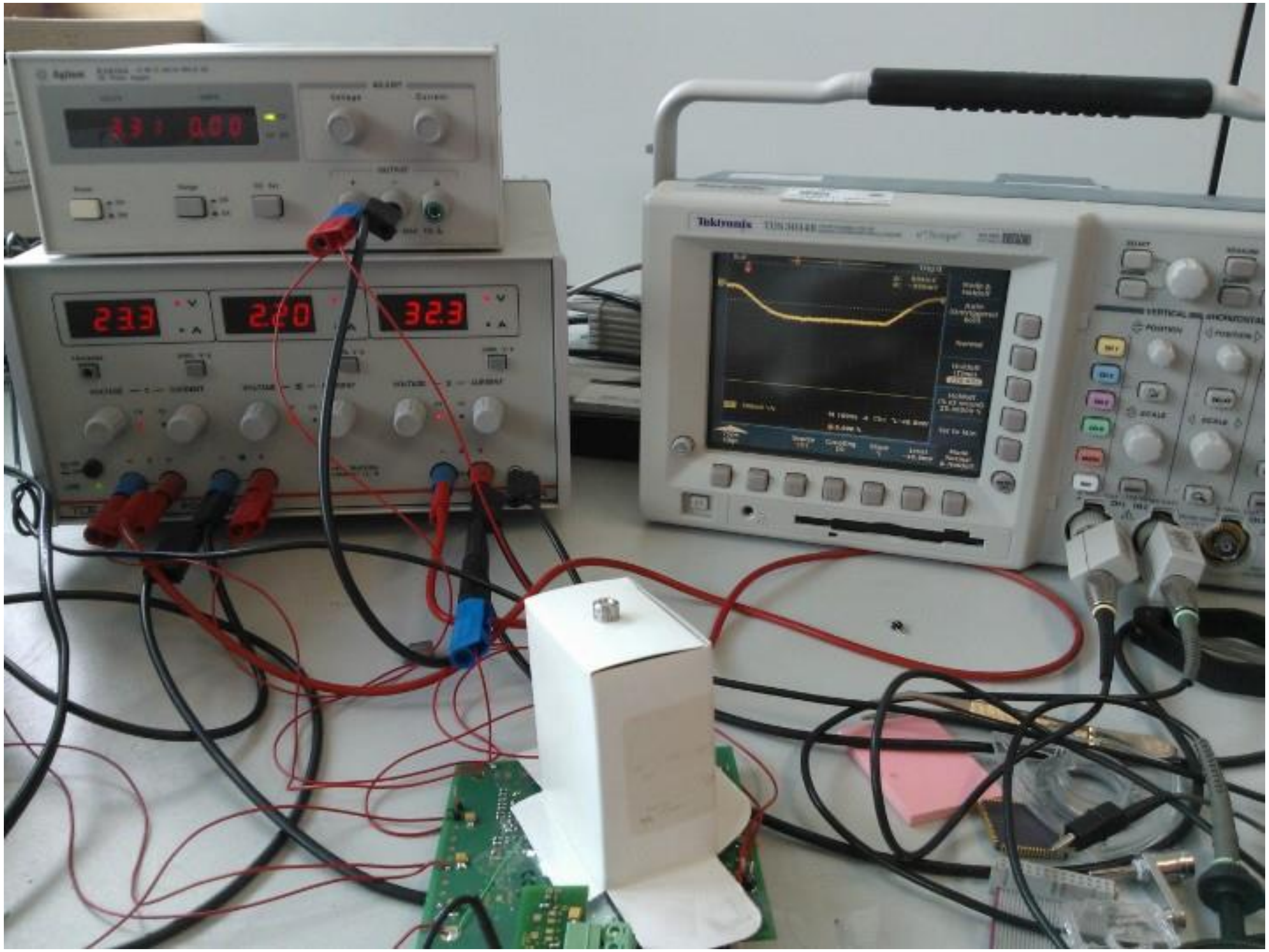


CCPD1 irradiated with x-rays
Amplifier gain loss

CCPD2 irradiated with x-rays
Amplifier gain loss
Rad hard pixels

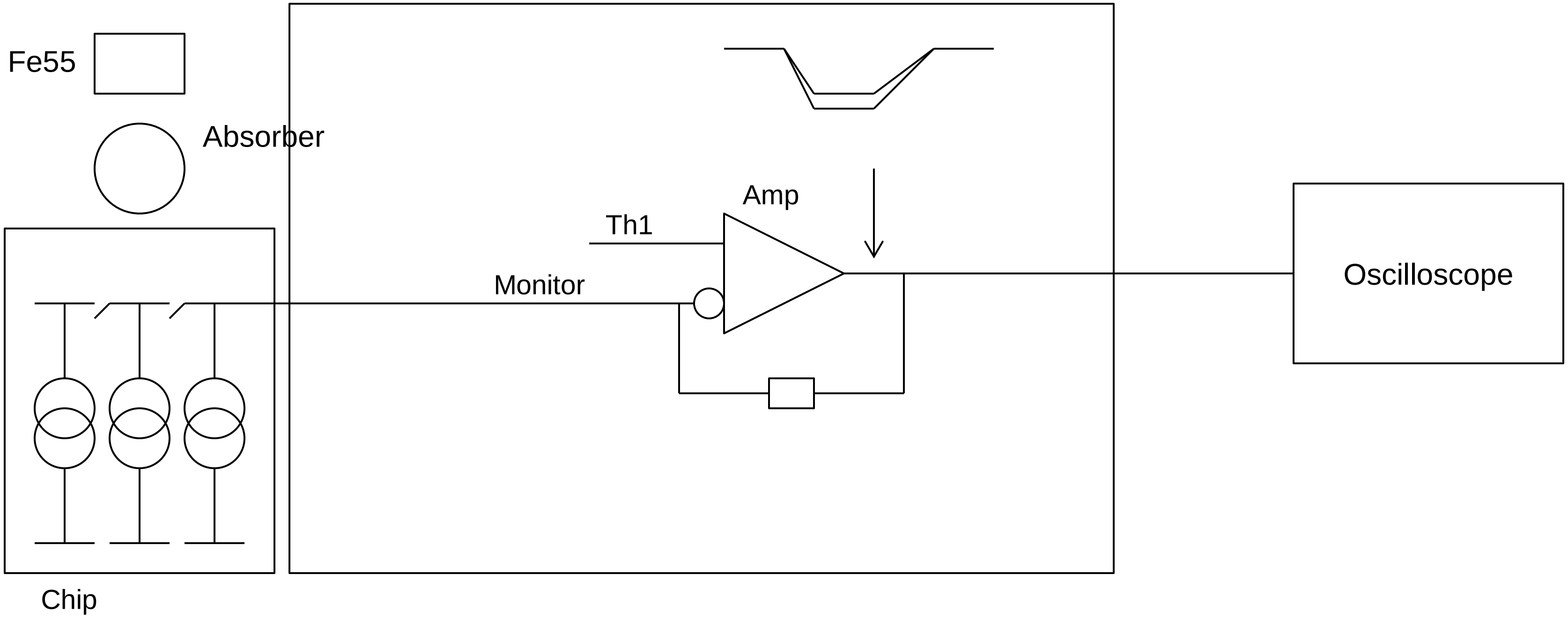
Segmented Strip Measurements

- Setup



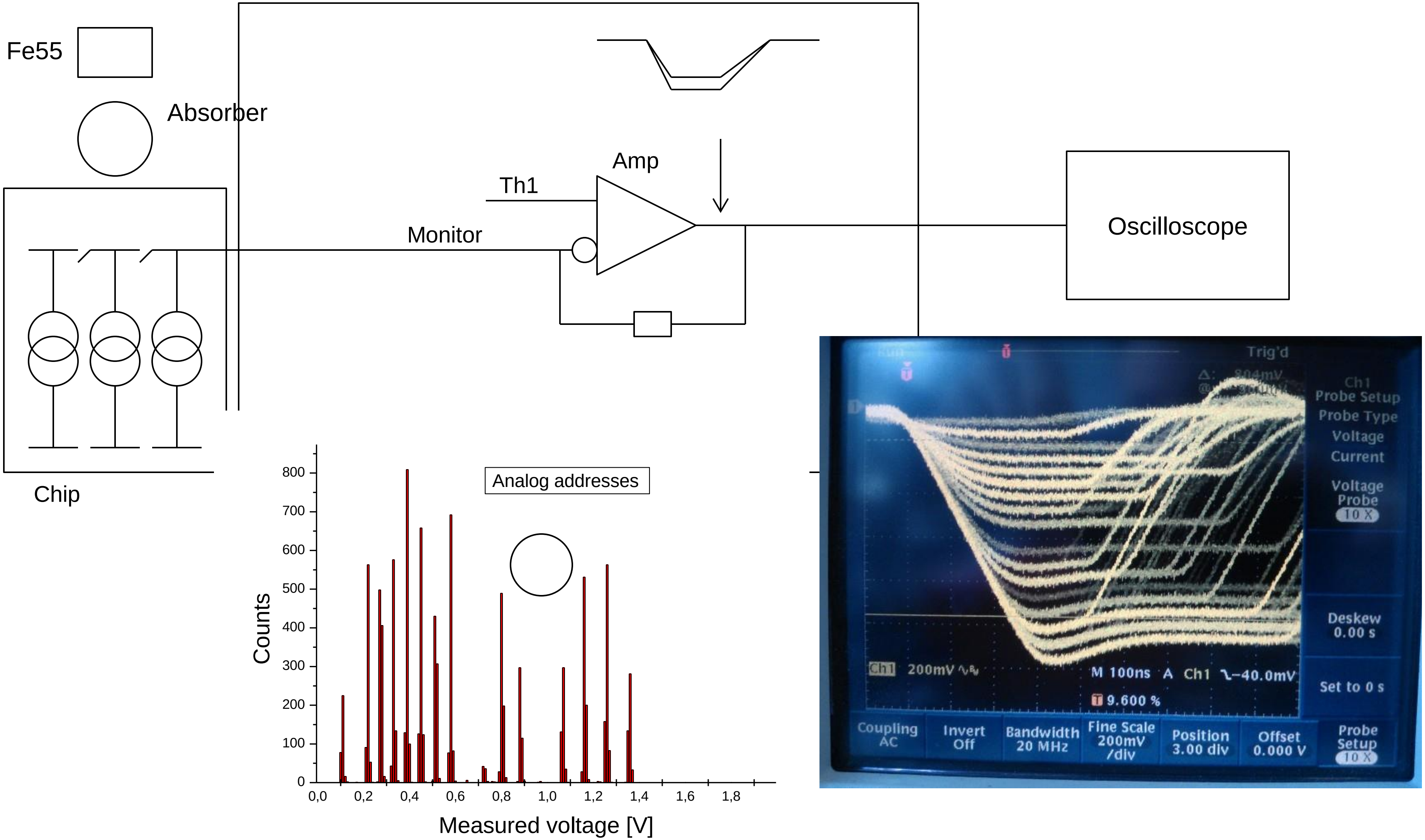
Segmented Strip Measurements

- Strip measurement circuit



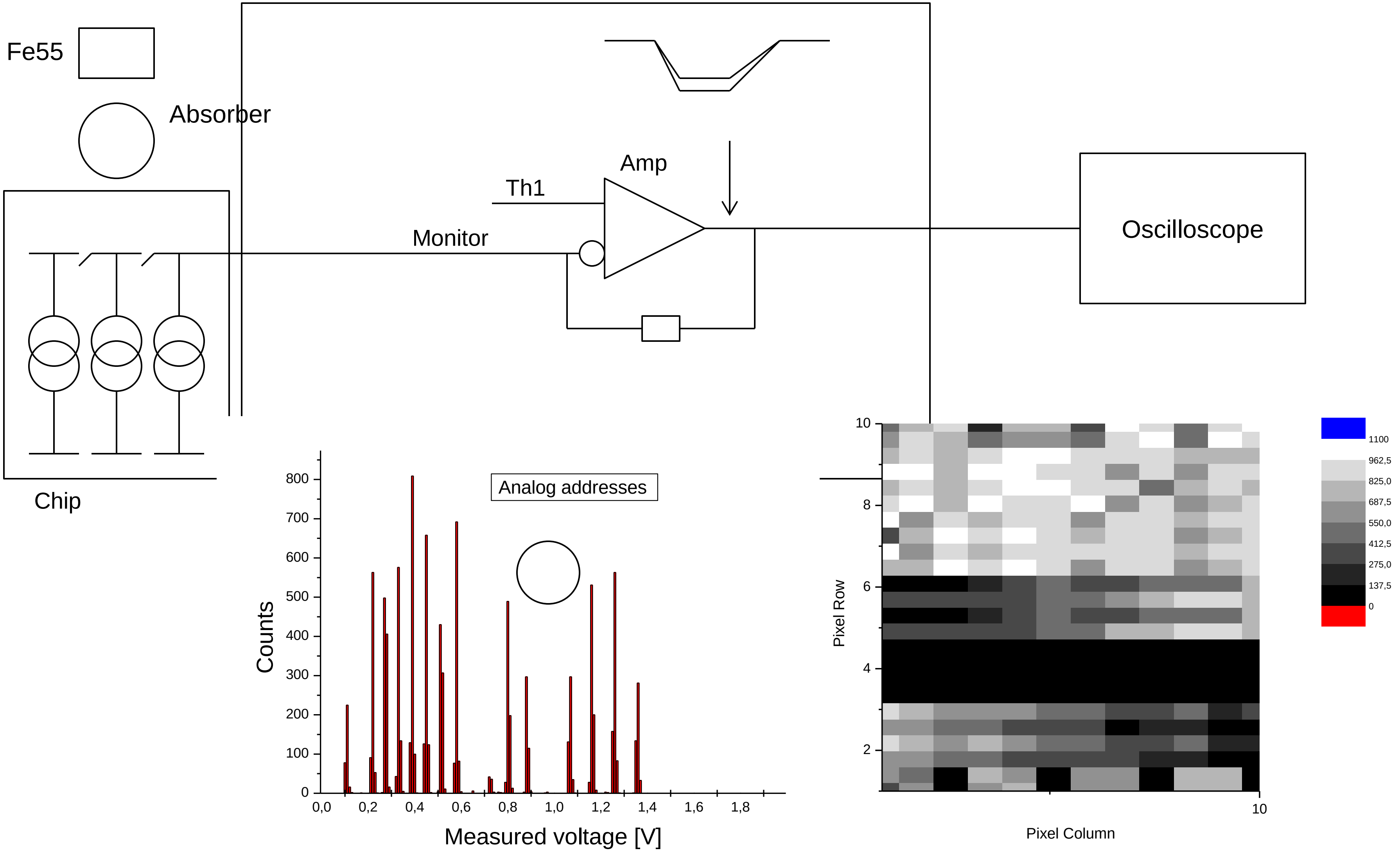
Segmented Strip Measurements

- Strip measurement circuit



Segmented Strip Measurements

- Strip measurement circuit



Conclusion

- We are investigating the use of HVCMOS detector for HLLHC ATLAS upgrade
- Test detectors CCPD1 (rad soft design) and CCPD2 (rad hard design) work
- MIP signal (1500 e), noise (75e) and threshold dispersion (25 e) values are good enough for efficient detection, however threshold tuning still have to be improved
- CCPD1 has been irradiated with x-rays, protons and neutrons, it is affected by ionizing radiation stronger than expected, however operation up to ~80Mrad is possible
- CCPD2 has been irradiated to 860Mrad with x-rays, it works, noise doubled at room T
- The noise increase can be mitigated by cooling and design optimization
- Irradiations of CCPD2 with neutrons and protons are planned
- Operation after 10^{15-16} neq/cm^2 could be possible if the diffusion signal is not entirely lost after these fluencies
- Plans for the next small test-detector
- Optimization of noise by increasing feedback resistance, bias current, etc.
- Optimization of pixel geometry
- Design and production of a larger test-detector (e.g. 1 cm^2) planned for 2014

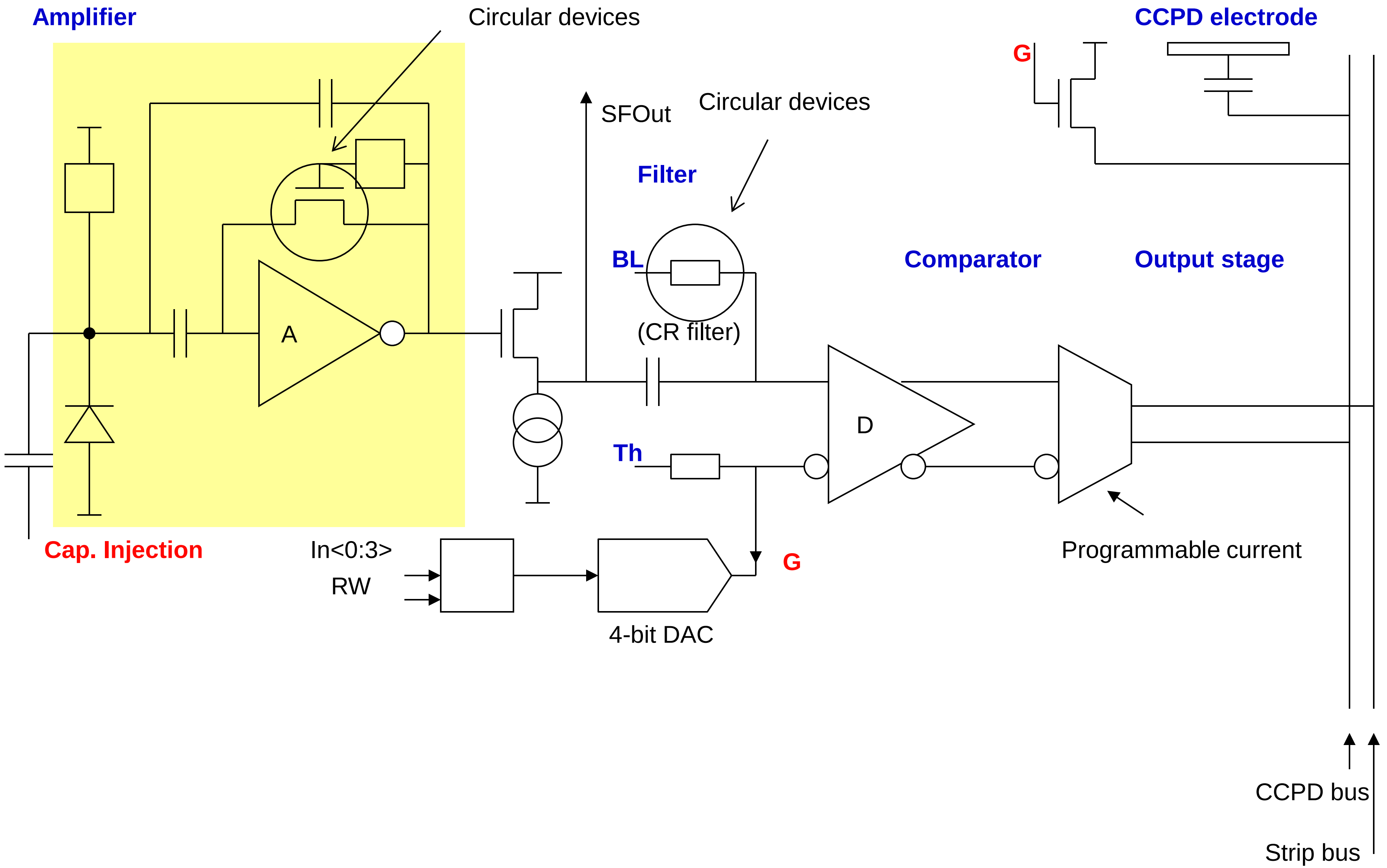
Properties of HVCMOS Detectors

- Good properties:
- Fast charge collection (field ~ 6-8.5V/µm, collection time ~ 100ps)
- High radiation tolerance
- Thinning is possible (active region several 10µm at the surface)
- Relatively cheap due to the use of a commercial process (1.5 kEUR / 8inch wafer)
- Disadvantages:
- Small depleted region, relatively small primary- (drift collected) signal, pixel capacitance ~100fF for larger pixels
- We expect that the drift-collected signal does not decrease with irradiation, the question is how much of the diffusion part remains
- SNR can be improved using the charge sensitive amplifier at the cost of increased power
- Main challenges: achieve good detection efficiency and low time walk for a given power budget
- Simulation example for 30µm x 125µm pixel: a good SNR and a time walk of about 10ns can be achieved at the power consumption of about 100mW/cm^2
- Some limitations arise from the fact that the electronic is placed inside the collecting electrode
- Additional capacitance, crosstalk
- Solution: the use of simplified pixel electronics

Thank you!

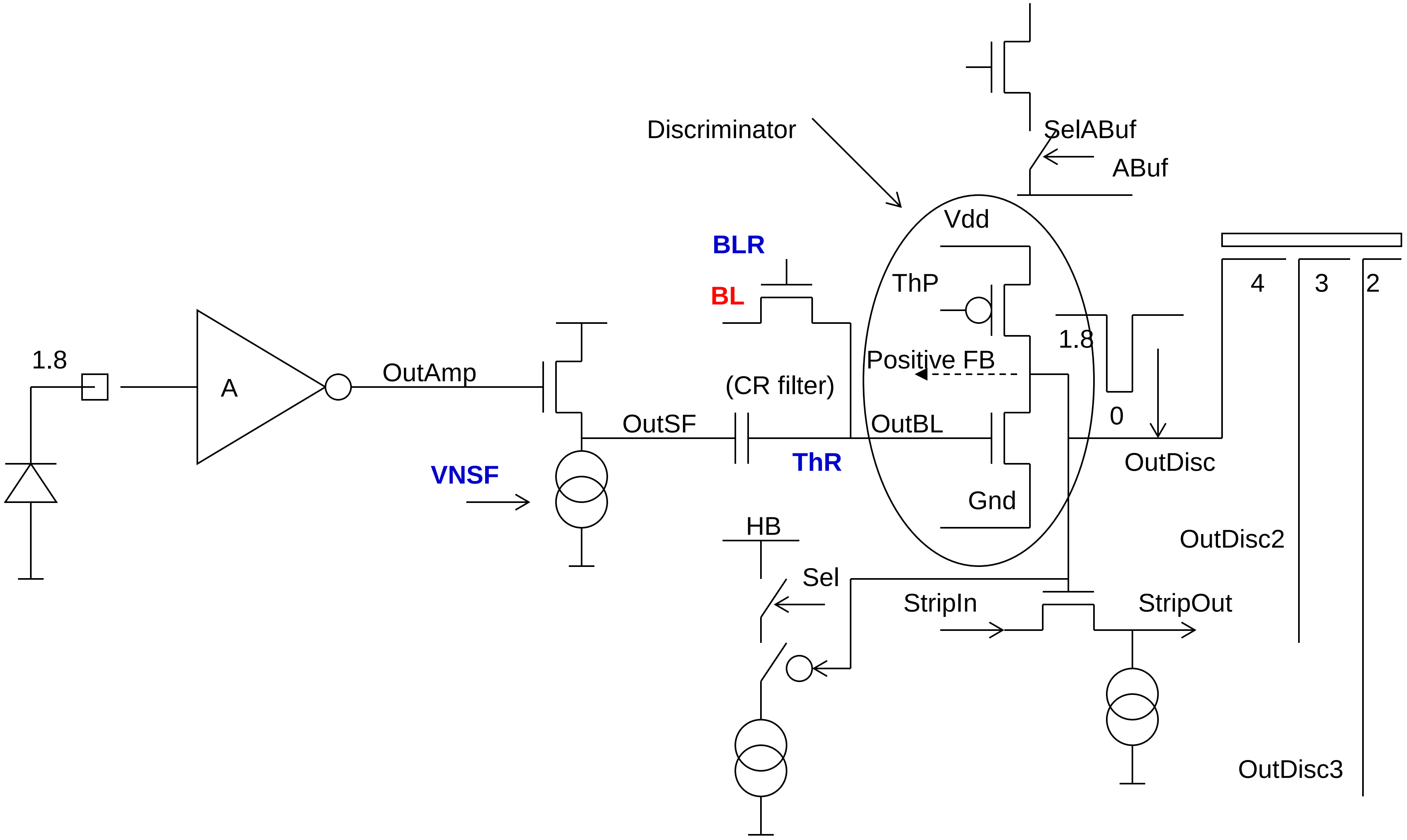
Backup Slides

Pixel electronics (1)



Ivan Peric, 9th Hiroshima Symposium, Hiroshima, 2013

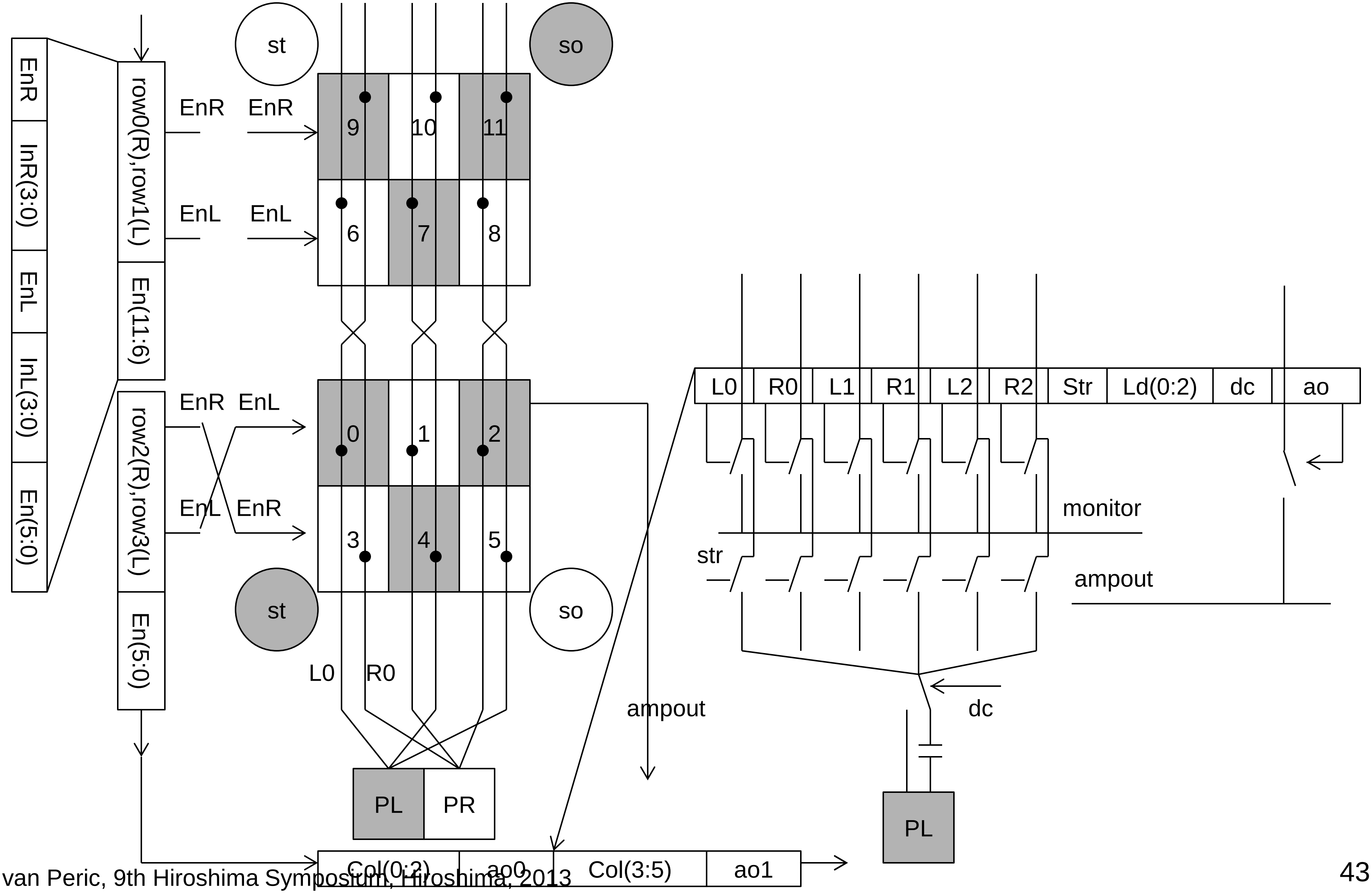
Simple Pixel



Ivan Peric, 9th Hiroshima Symposium, Hiroshima, 2013

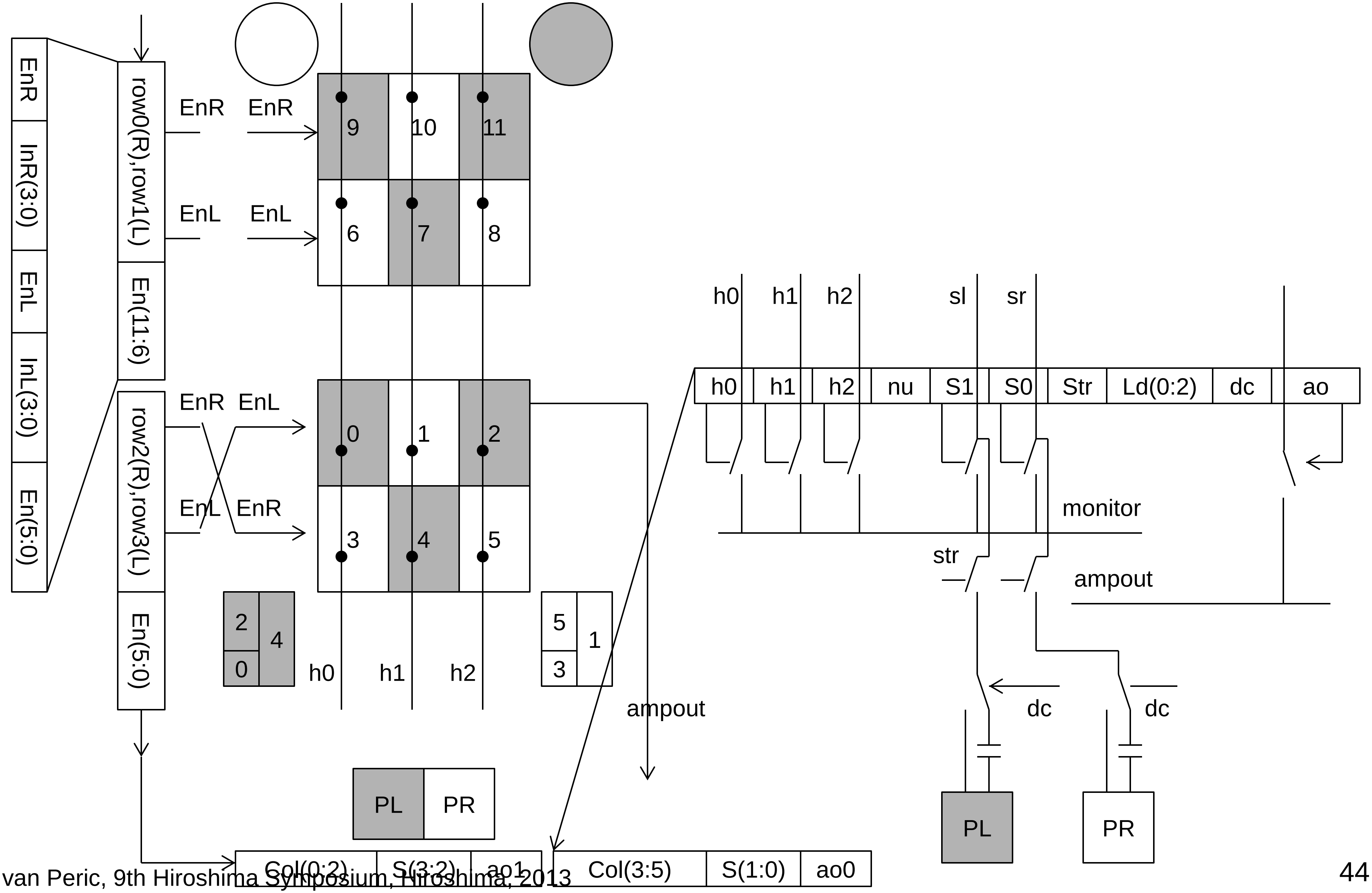
Standard pixel

EnL/R=1 - enables CCPD, disables hitbus/strip



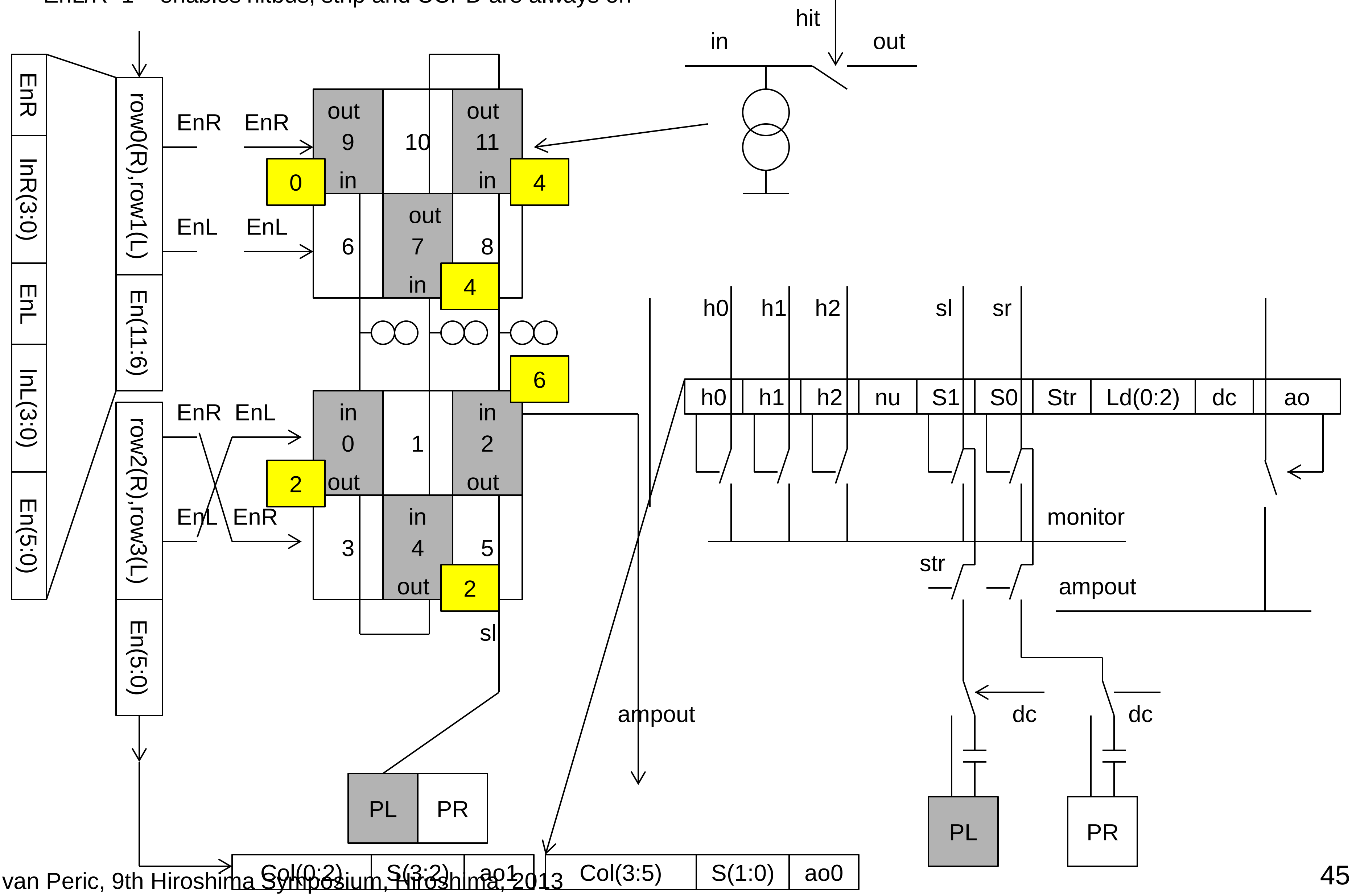
Simple Pixel

EnL/R=1 – enables hitbus; strip and CCPD are always on



Simple Pixel

EnL/R=1 – enables hitbus; strip and CCPD are always on



Simple Pixel

EnL/R=1 – enables hitbus; strip and CCPD are always on