FAST FRONT-END ELECTRONICS FOR SEMICONDUCTOR TACKING DETECTORS: Trends and Perspectives

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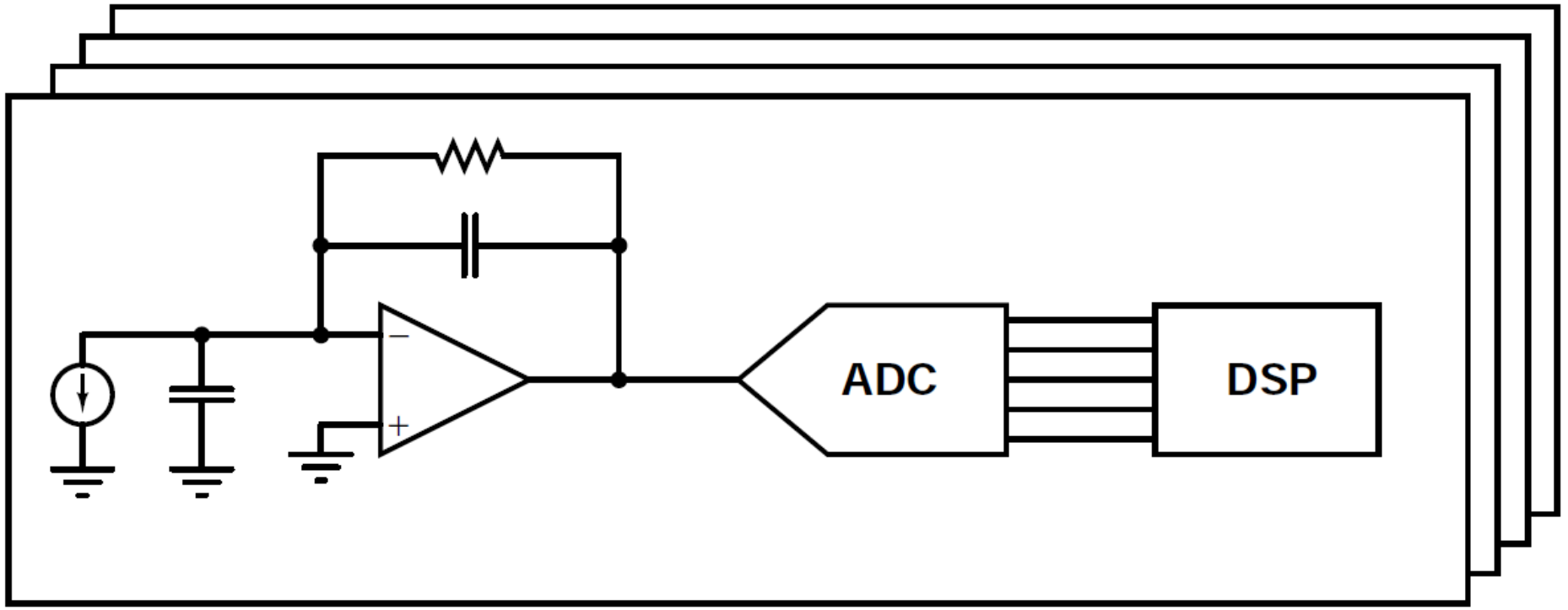
An interesting processing chain



- **Digital signal processing** naturally suited to **deep submicron** CMOS technologies.
- Possibility of applying **corrections** before event selection:very interesting to reject **common mode** noise.
- Accuracy of **feature extraction** does **not** depend on the accuracy of the **analog components**.

FE with DSP: state of the art

Super-Altro 16: A Front-End System on Chip for DSP Based Readout of Gaseous Detectors

P. Aspell, M. De Gaspari, E. França, E. García García, L. Musa
IEEE Trans. Nucl. Sci., vol. 60, No. 2, April 2013.

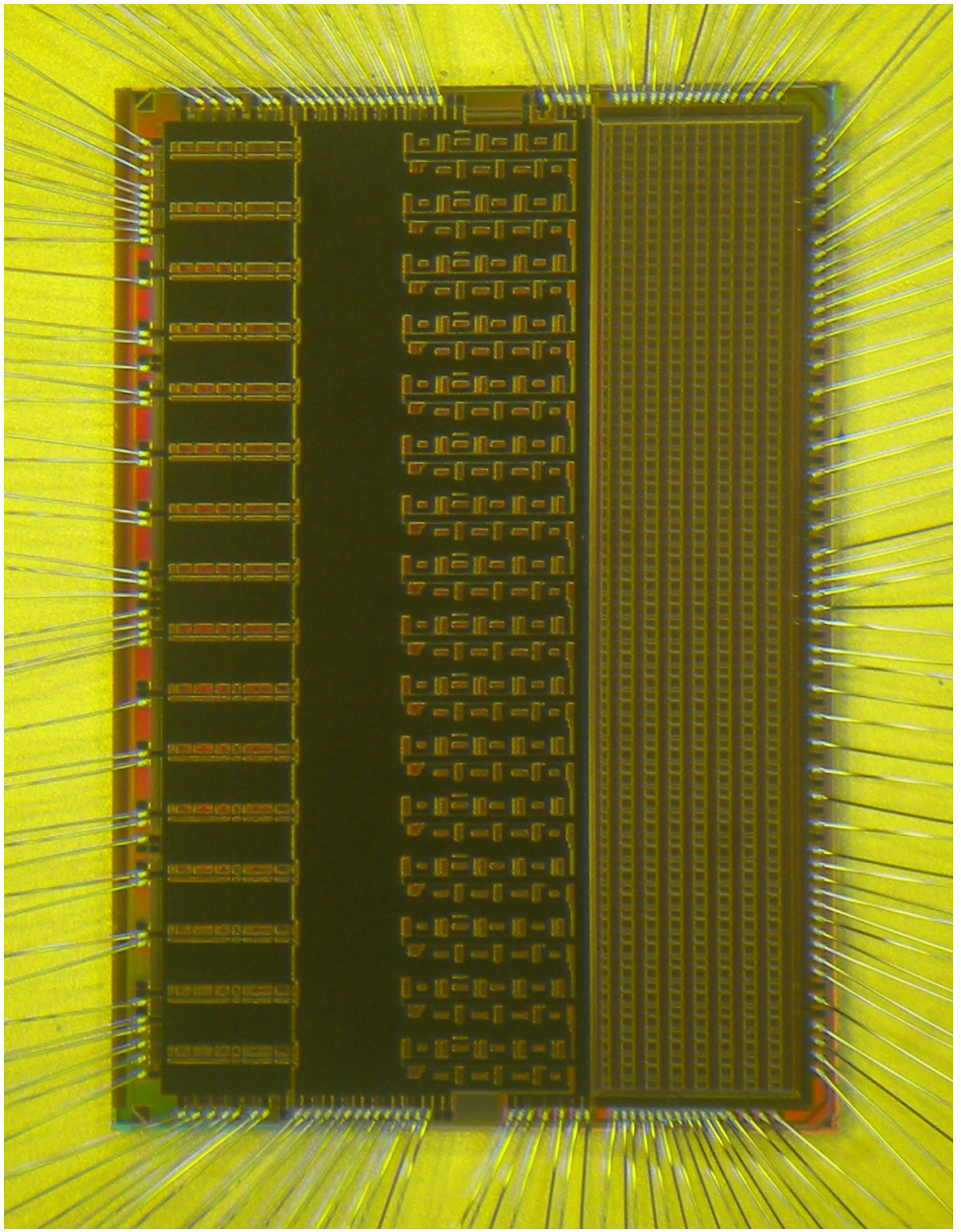
- **Prototype chip developed for the read-out of the Linear Collider TPC.**
- **Based on the present readout of the ALICE TPC (PASA+ALTRO chip with DSP on two separate dies).**
- **16 channels with front-end, ADC and digital signal processor.**
- **Fully differential, 10 bit pipeline ADC**
- **3 mm^2 per channel (active area) in CMOS 0.13 µm.**
- **Key DSP functions:baseline subtraction, signal conditioning, baseline correction and zero-suppression**

Noise 300 electrons: successful integration of preamp and DSP in the same ASIC

Key S-ALTRO features

S-ALTRO key performance	
Gain	12, 15,19, 27 mV/fC
Peaking time	30, 60, 90, 120 ns
Signal polarity	both
Detector capacitance	4-20 pF
Number of bits	10
Sampling Frequency	10-40 MHz
Power (active)	47 mW/ch
Power (sleep)	0.6 mW/ch

S-ALTRO power break down	
PASA	10 mW/ch
ADC (analog)	31.28 mW/ch
ADC (digital)	1.7 mW/ch
DSP	4 mW/ch



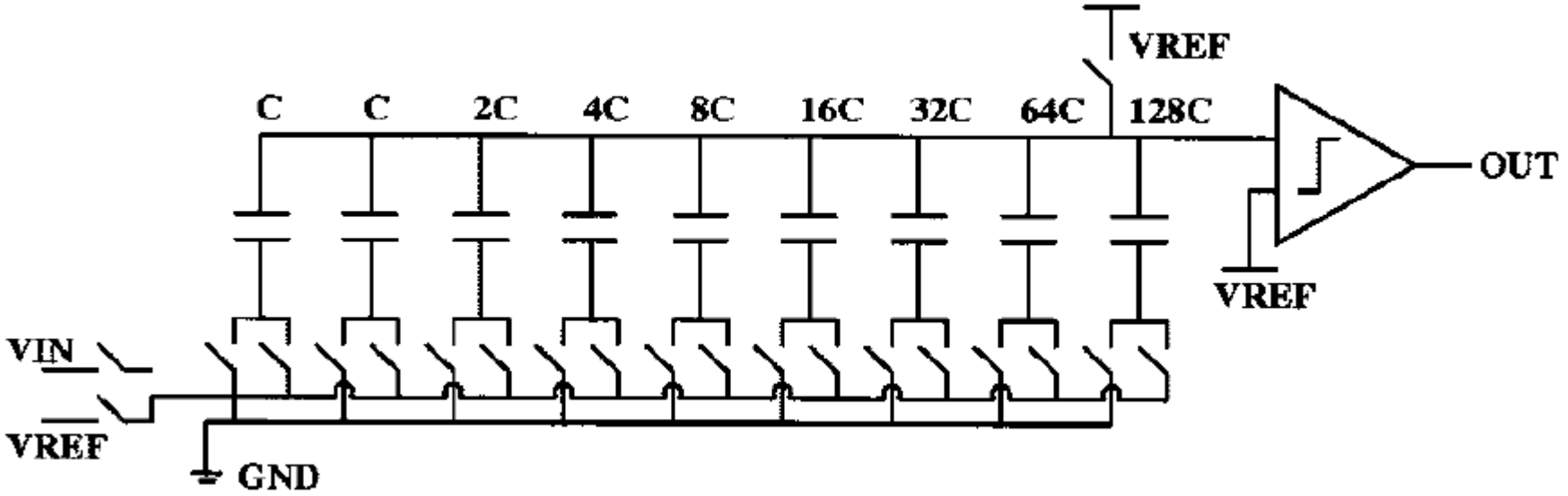
Low power ADC: some examples

Ref	Technology	Architecture	N of bit	Sampling rate (MS/s)	ENOB	Power (mW)	FOM (Fj/step)
1	90 nm	SAR	9	40	8.23	0.82	68
2	130 nm	SAR	10	50	9.11	0.82	30
3	65 nm	SAR	10	100	9.01	1.13	22
4	90 nm	FLASH+SAR	9	100-200	8.44-8.31	0.75/1.33	34.7
5	90 nm	SAR	10	50	9.5	0.32	9

$$FoM = P/(2^{ENOB} F_s)$$

- ADC with 50 MS/s, 9-10 bit resolution and < 1mW of power are now common.
- The renaissance of the SAR ADC.

Traditional SAR ADC (1)



- In the sampling phase the top plate is connected to VREF and the bottom plate to VIN.
- After sampling the top plate is left floating and all the bottom plate are switched to GND. Voltage of the top plate is VREF-VIN.
- The capacitance of the MSB (128C) is switched to VREF. The voltage of the top plate is VREF-VIN+VREF/2. If the voltage is > VREF, the MSB is set to zero and the bottom plate of the MSB capacitors is switched back to GND.
- If VREF-VIN+VREF/2 is smaller than VREF, the bottom plate of the MSB is kept at VREF and the corresponding bit is set to 1.
- The procedure continues with the other bits.

Traditional SAR ADC (2)

- In conventional SAR ADC:
- Capacitors can be switched back and forth between VREF and GND: unnecessary power consumption in the DAC.
- DAC capacitors are usually over-sized with respect to the minimum required by noise boundaries.
- Logic is synchronous with a master clock: 40 MHz clock leads to less that 4 MS/sec.

Performance improvements stem from:

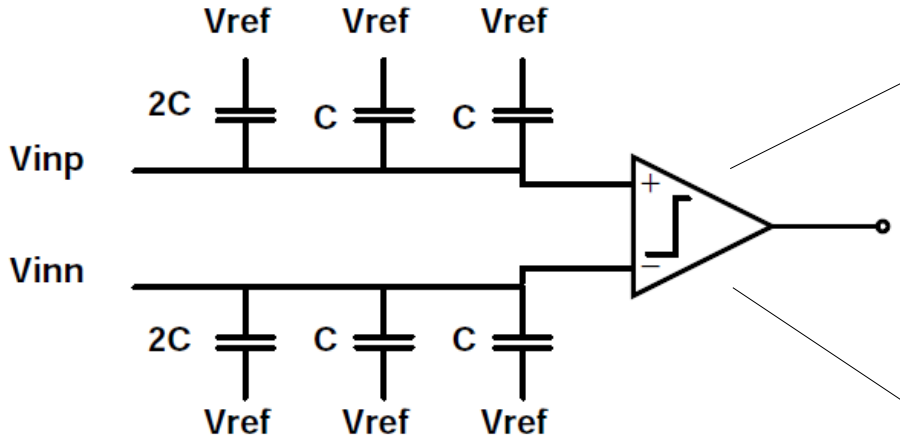
- Reduction of capacitor size
- Modified switching schemes
- Use of asynchronous logic

Modified switching algorithms

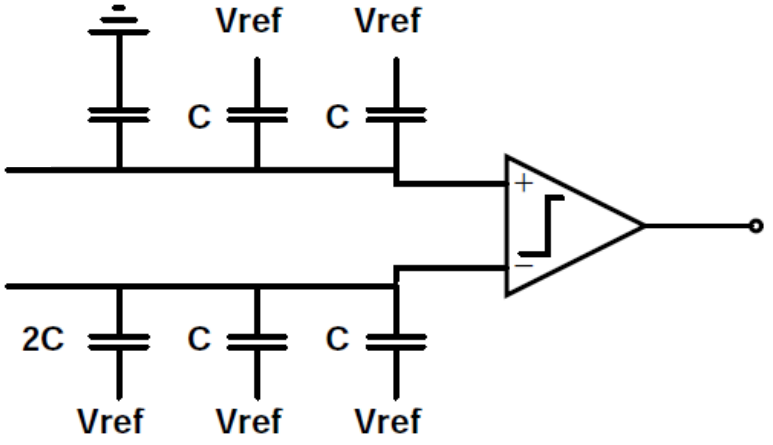
A 10-bit 50-MS/s SAR ADC With a Monotonic Capacitor Switching Procedure

Chun-Cheng Liu, *Student Member, IEEE*, Soon-Jyh Chang, *Member, IEEE*, Guan-Ying Huang, *Student Member, IEEE*, and Ying-Zu Lin, *Student Member, IEEE*

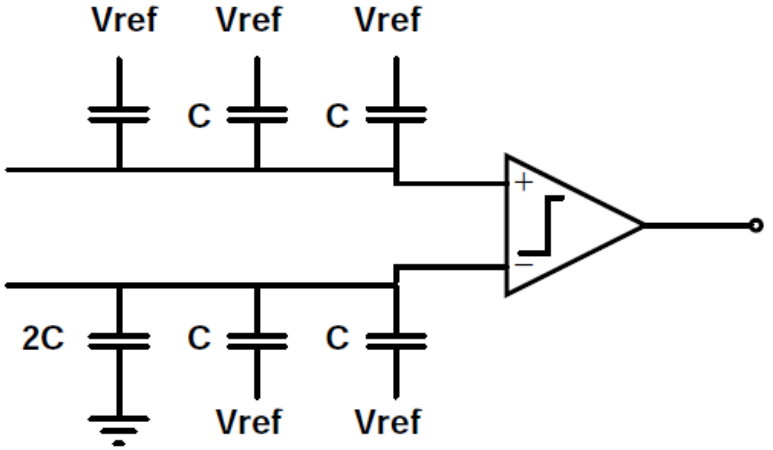
Sampling & first comparison

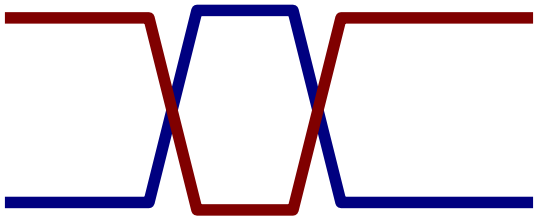


If Vinp > Vinn



If Vinp < Vinn





- **Modern ADC are always fully differential.**
- **A front-end with fully differential outputs is necessary.**
- **Alternative switching schemes can save up to 98% of the DAC power**

Capacitor in SAR ADC

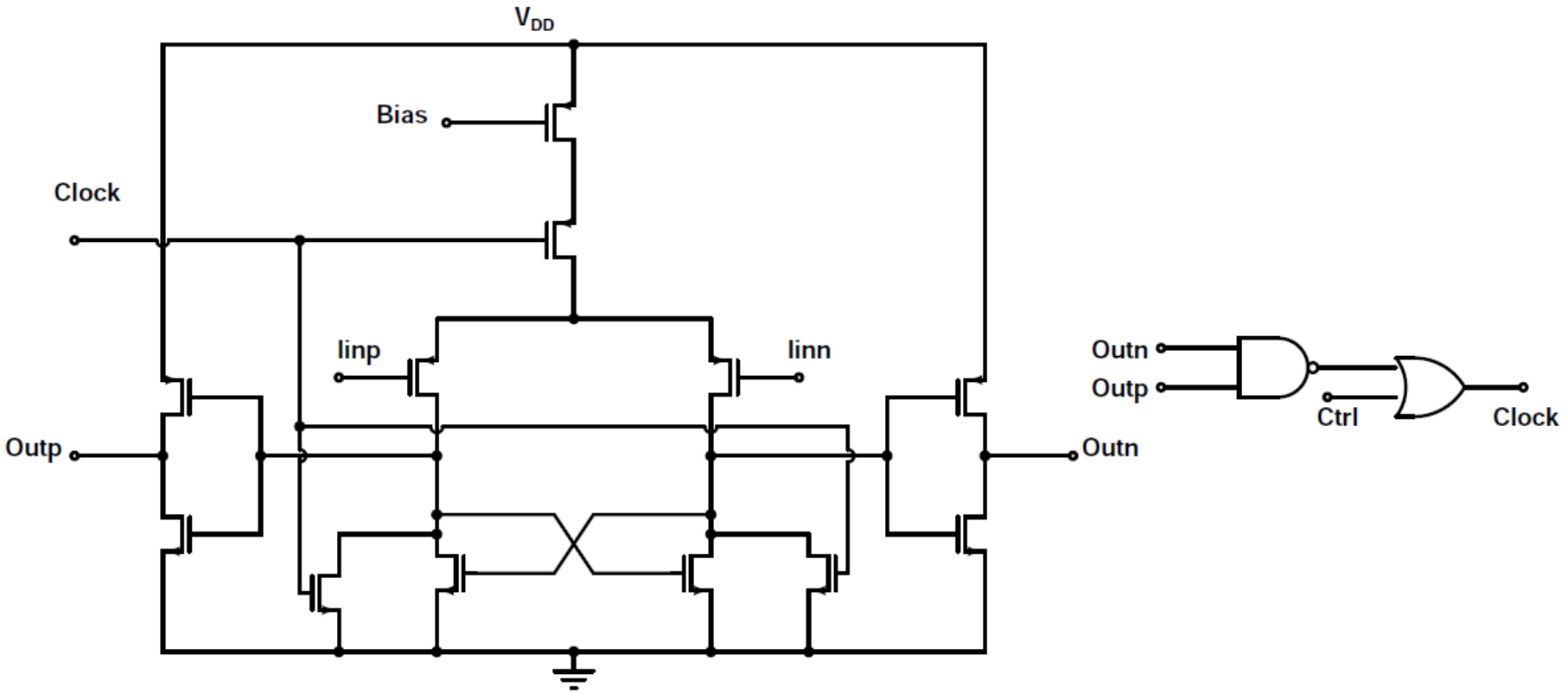
- **Noise limits:**

$$V_{LSB} = \frac{V_{FS}}{2^N} \qquad E_q = \frac{V_{LSB}}{\sqrt{12}} \qquad \frac{kT}{C_{DAC}} = \frac{{V_{FS}}^2}{12 \cdot 2^{2N}}$$

Number of bits	Total DAC capacitance	LSB capacitance
5	$5.09 \cdot 10^{-17}$	$1.59 \cdot 10^{-18}$
6	$2.03 \cdot 10^{-16}$	$3.18 \cdot 10^{-18}$
7	$8.14 \cdot 10^{-16}$	$6.36 \cdot 10^{-18}$
8	$3.26 \cdot 10^{-15}$	$1.27 \cdot 10^{-17}$
9	$1.30 \cdot 10^{-14}$	$2.54 \cdot 10^{-17}$
10	$5.2 \cdot 10^{-14}$	$5.08 \cdot 10^{-17}$
11	$2.08 \cdot 10^{-13}$	$1.02 \cdot 10^{-16}$
12	$8.33 \cdot 10^{-13}$	$2.03 \cdot 10^{-16}$

- DAC capacitance can be very small
- Practical limit comes from matching rather then noise
- LSB capacitance as low as 1 fF already used.

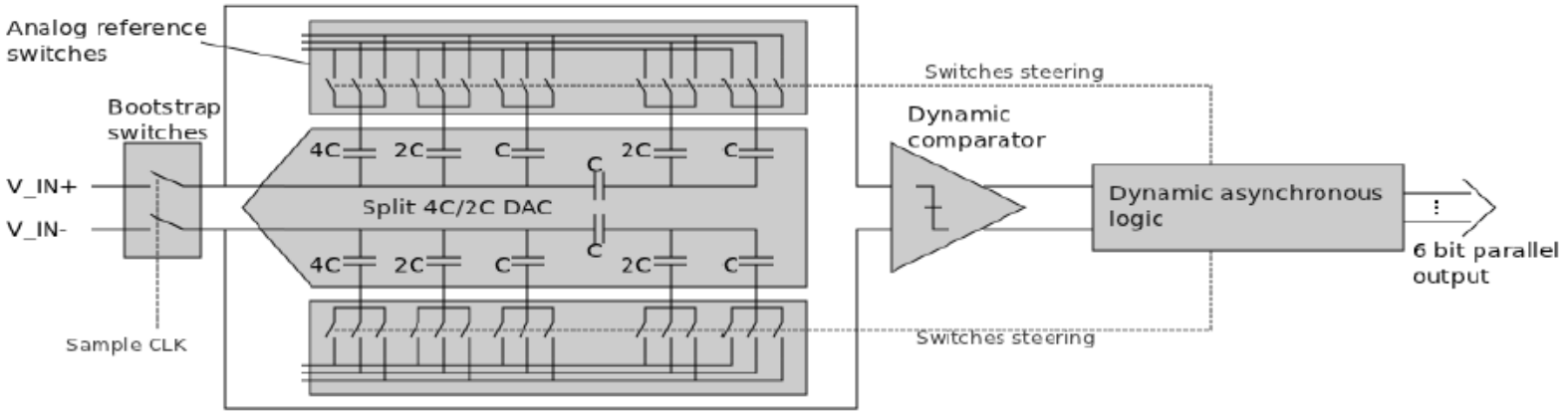
Example of asynchronous logic

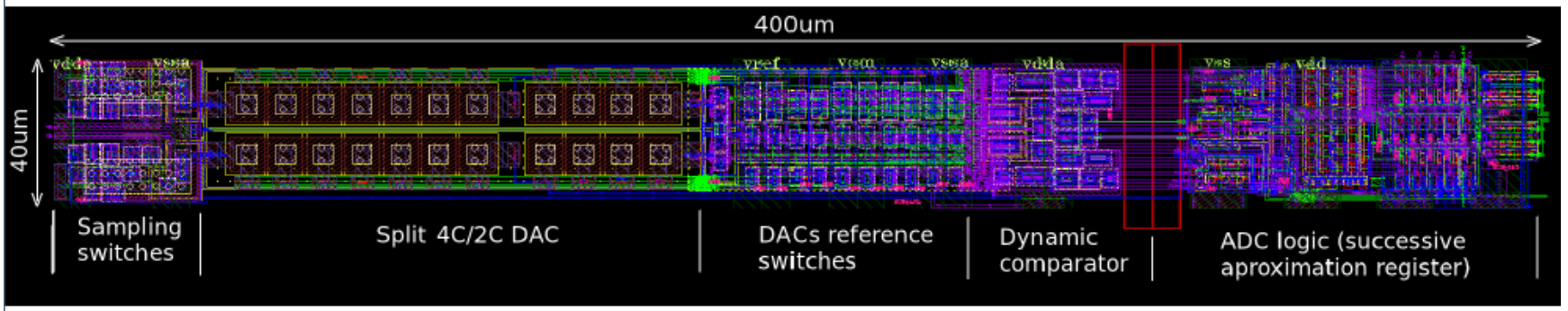


- Clock speed defined by the maximum **toggling frequency** of the **comparator**.
- Asynchronous logic design requires analog-grade simulations....
- In a **plain SAR**, clock frequency above **500 MHz** necessary to achieve **50 MS/s** of conversion speed.
- Higher speed achievable with **hybrid** architectures.

From M. Idizik et al., Multichannel ADC for physics applications
https://indico.cern.ch/conferenceDisplay.py?confId=225551

Design of 6-bit SAR ADC in IBM 130 nm





- Single channel: 40um x 400um (area 0.016 mm^2)
- Custom capacitor p-cell layout done to obtain 40um pitch

Prototypes under tests…
10-bit ADC, PLL, SLVS

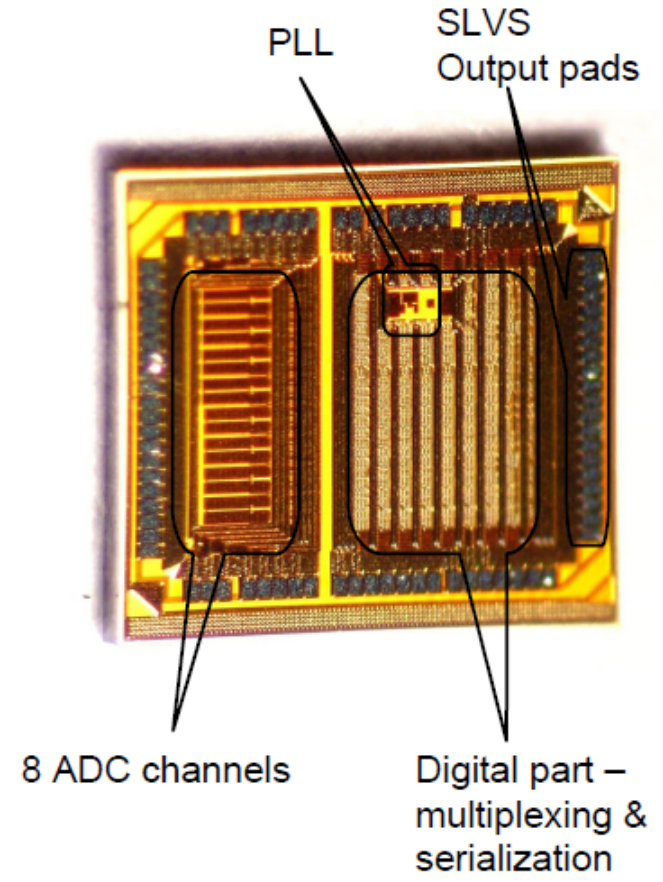
Tecnology:0.13 um CMOS
600 um x 146 um x 10 bit

Prototype of 10-bit ADC

- SAR ADC with segmented DAC
- Scalable frequency (up to ~50 MS/s) and power consumption
- Simulated power consumption 1-2mW at 40MS/s
- 146um pitch

Prototype of PLL

- Type II PLL with 2nd order filter
- Scalable frequency&power
- Automatically switched VCO frequency range 8MHz – 3GHz
- VCO frequency division by 6, 8, 10 or 16
- Simulated power consumption ~1mW at 3GHz



From M. Idizik et al., Multichannel ADC for physics applications
https://indico.cern.ch/conferenceDisplay.py?confId=225551

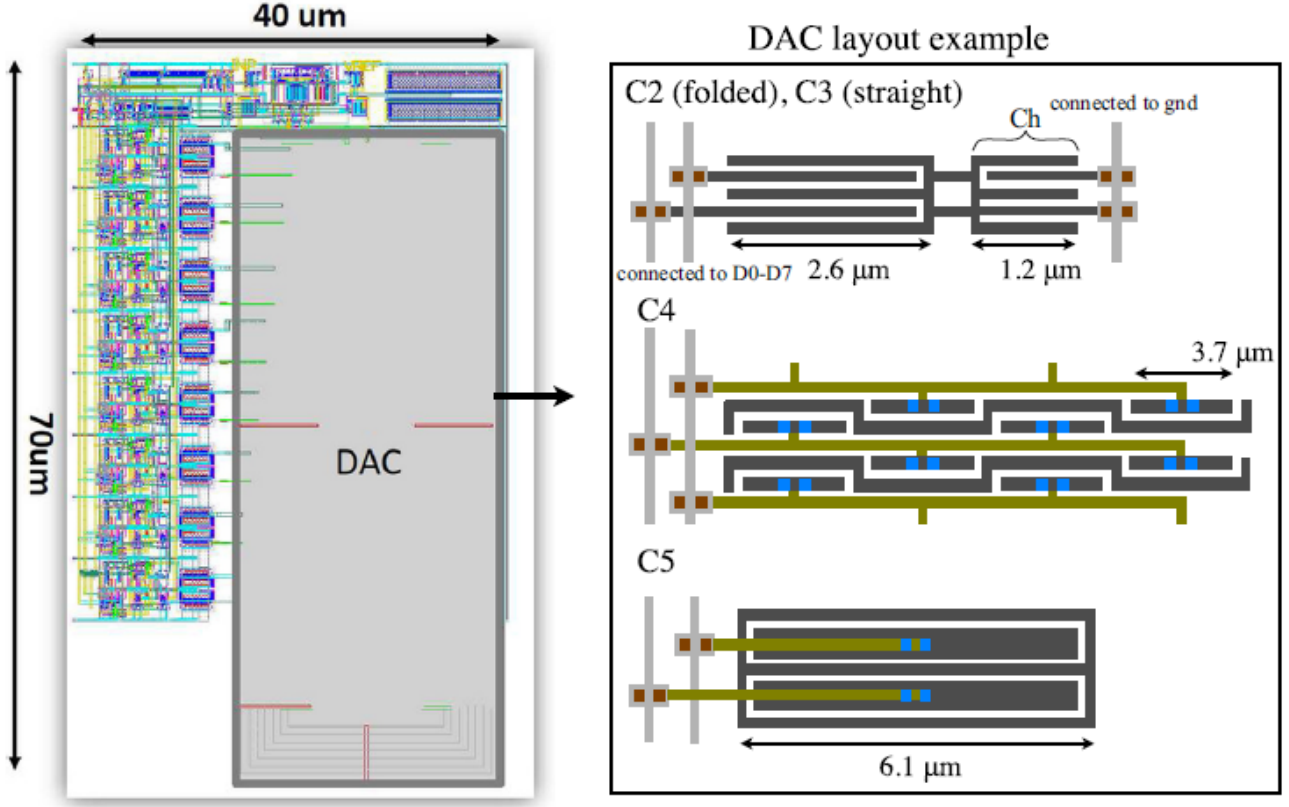
Nuclear Instruments and Methods in Physics Research A ▮ (▮▮▮▮) ▮▮▮–▮▮▮

A 10 MS/s 8-bit charge-redistribution ADC for hybrid pixel applications in 65 m CMOS ☆

Tetsuichi Kishishita*, Tomasz Hemperek, Hans Krüger, Manuel Koch, Leonard Germic, Norbert Wermes

University of Bonn, Physikalisches Institut, Nussallee 12, 53115 Bonn, Germany

70 um x 40 um, 8 bit, 40 uW@10MS/s in 65 nm



A first outlook

- Thanks to the spectacular progress in ADCs, in a 0.13 um technology, full sampling can be feasible at very low power
- For 10 bit resolution and 3 mW of power per channel (excluding the front-end).
- The most complex part of the DSP can be triggered only if there is a suspicion of an event, saving further power.
- Power could be cut futher by going to more aggressive technologies
- In case of power cycling, average power consumption becomes very small

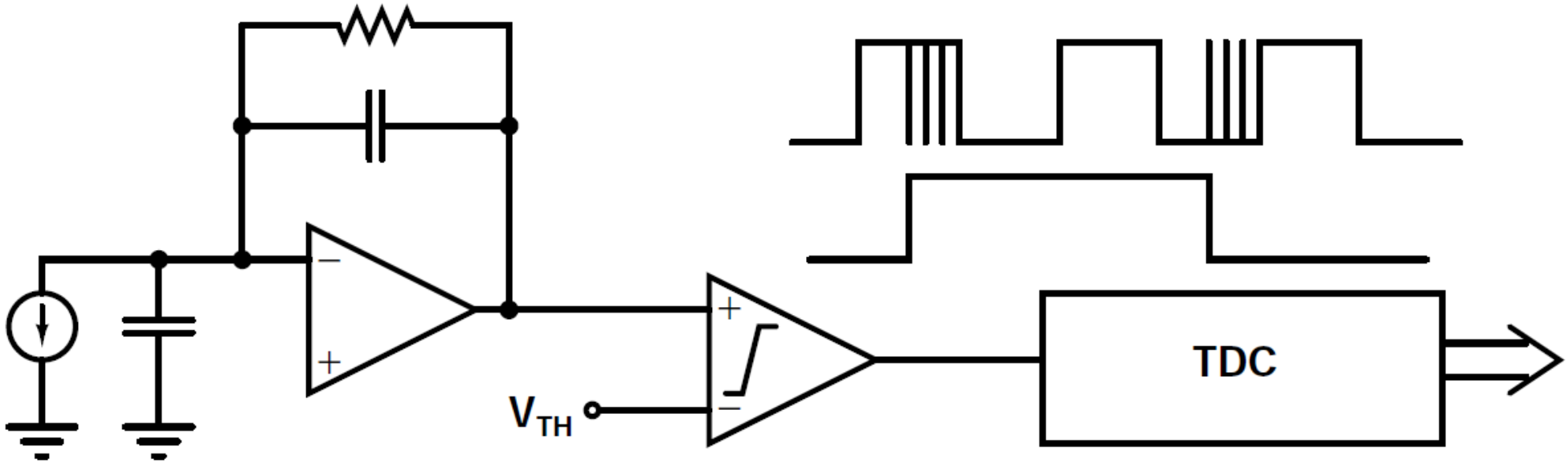
- More front-end chips are likely to be designed in the near future along this line.

What about timing?

Interest is growing around tracking detectors with improved time-tagging capabilities:

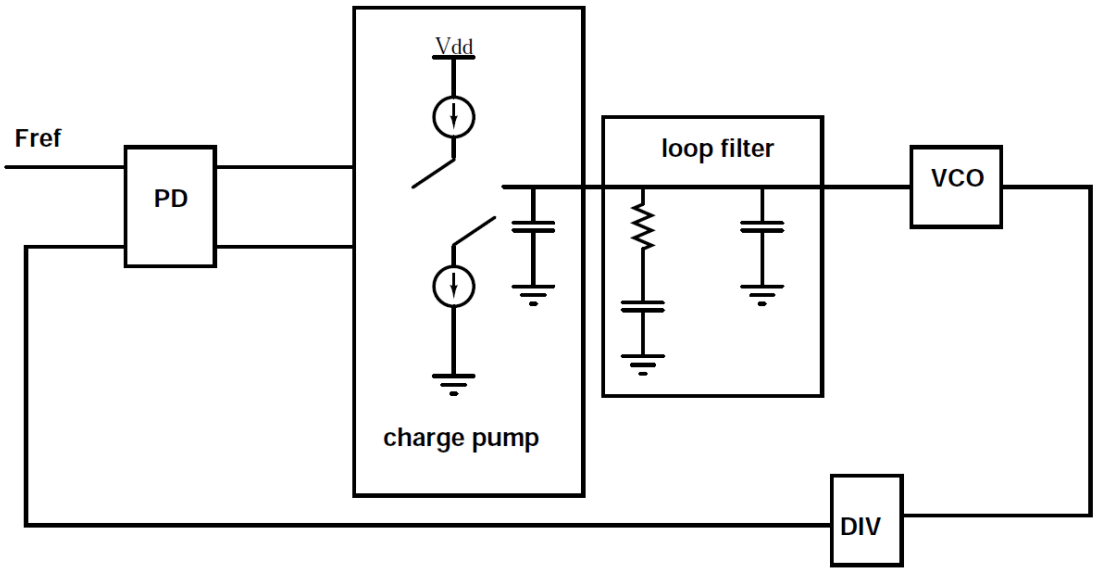
- **Free running detectors with data push architectures or with high pile-up**
  - **Time resolution O(ns).**
  - **Can be derived from a clock: (20 ns clock provides 5.7 ns rms)**
  - **In case of analog readout with waveform sampling, can be improved with interpolation. Time resolution of 5-10% of the peaking time easily achievable.**

- **Specialized tracking detectors with very good time resolution (<100 ps)**
  - **Require dedicated high resolution timing channels.**

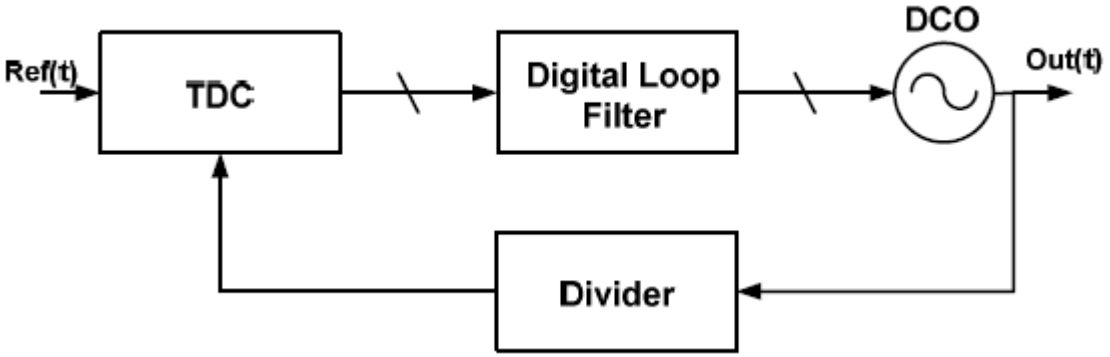


TDC growth

Due to the interest in ALL Digital PLL (ADPLL), TDC left the niche market of instrumentation (HEP, range finding, testing) to become more general purpose components, with an significant increase on the number of published papers in the recent years.



Conventional analog PLL
Needs an analog filter



ALL Digital PLL
Phase difference measured with a TDC

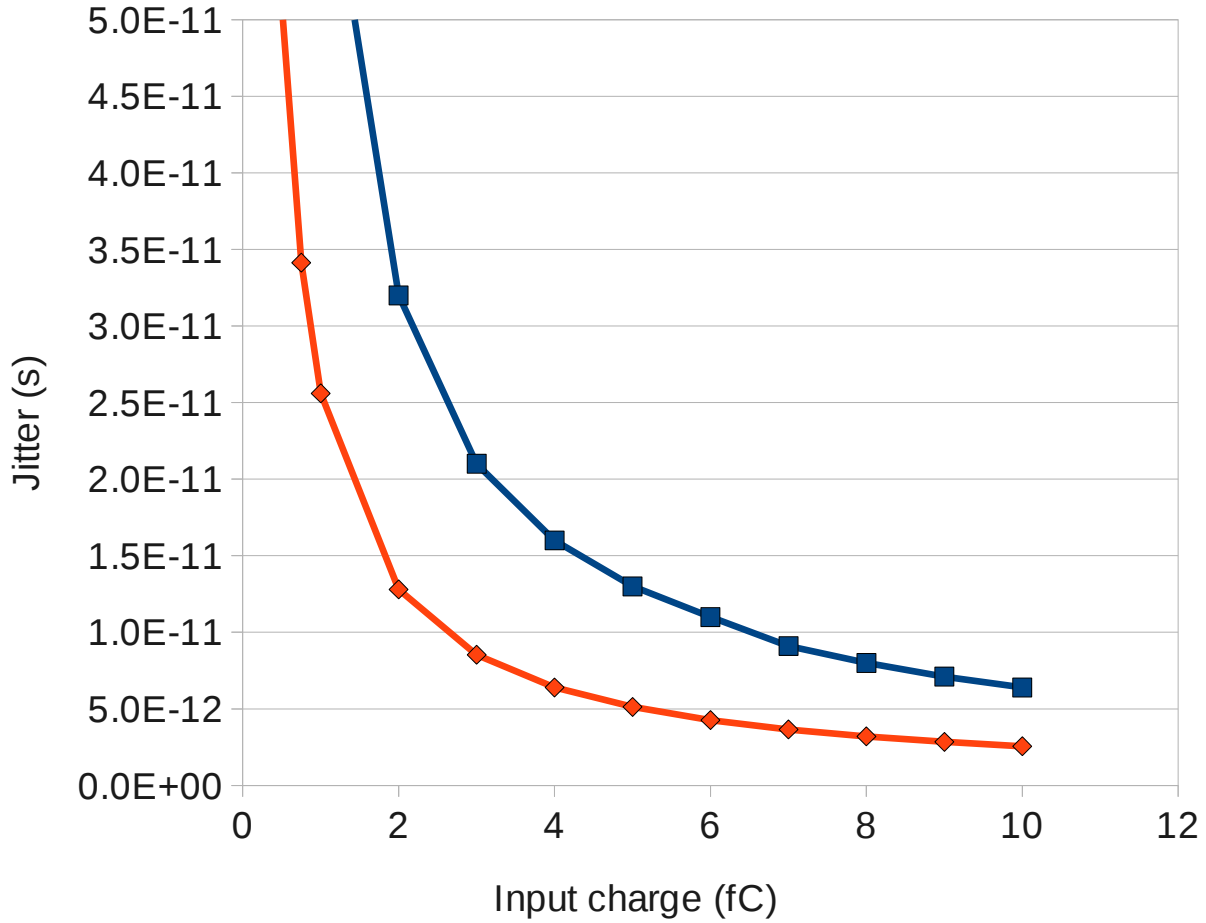
Some recent TDC designs

Ref	Technology	Architecture	Resolution (ps)	Sampling rate (MS/s)	Range (ns)	Power (mW)	Area
1	130 nm	GRO	1	50	12	2.2-21	0.04
2	130 nm	Vernier-ring	8	15	32	7.5	0.26
3	90 nm	Passive inter.	4.7	180	0.6	3.6	0.02
4	90 nm	Delay line	20	26	0.64	6.9	0.01
5	65 nm	2D delay line	4.8	50	< 0.6	1.7	0.02
6	90	Time Amp.	1.25	10	0.64	3	0.6
7	90	Vernier+GRO	3.2	25-100	40	3.6-4.5	0.027

- TDCs are now reaching the sub-ps resolution
- Many different architectures
- Dynamic range low in many high resolution TDC

Limits on timing: jitter

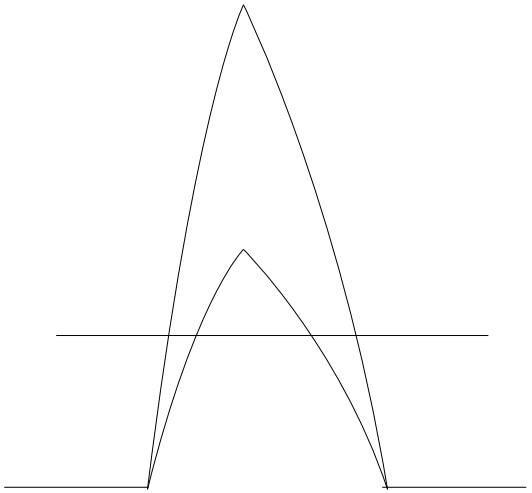
- **For a total signal rise time of 2 ns, a 10 ps resolution can be reached with a noise of 200 electrons and a signal of 6 fC or a signal of 2.5 fC and a noise of 80 electrons.**
- **Peaking time should match detector collection time.**



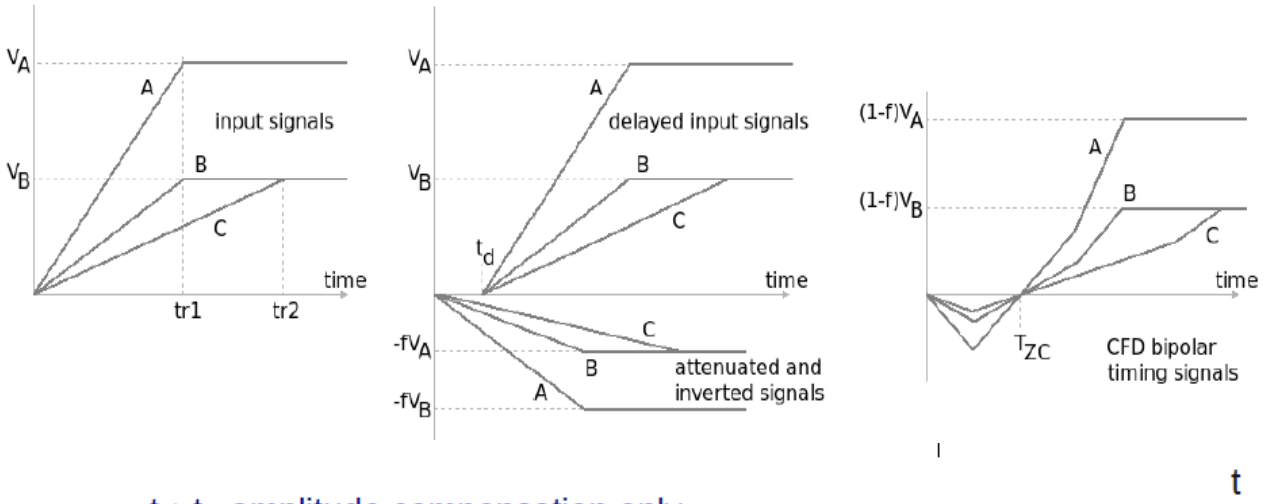
$$\sigma_t = \frac{\sigma_v}{\frac{dV}{dt}}$$

- **Noise limits:**

Some time extraction methods

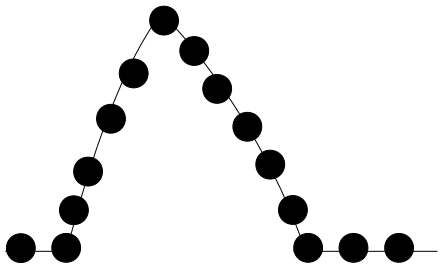


Leading edge timing



$t_d > t_r$, amplitude compensation only

$$fV_0 = \frac{t - t_d}{t_r} V_0 \qquad t_{zc} = f t_r + t_d$$



High speed waveform sampling (>GHz)

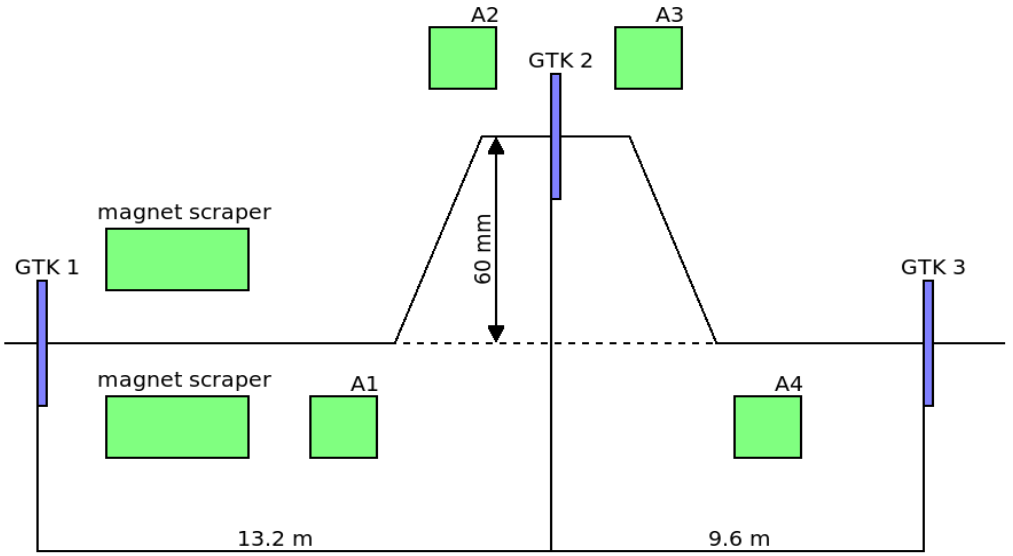
$t_d > t_r$, amplitude and rise time compensation

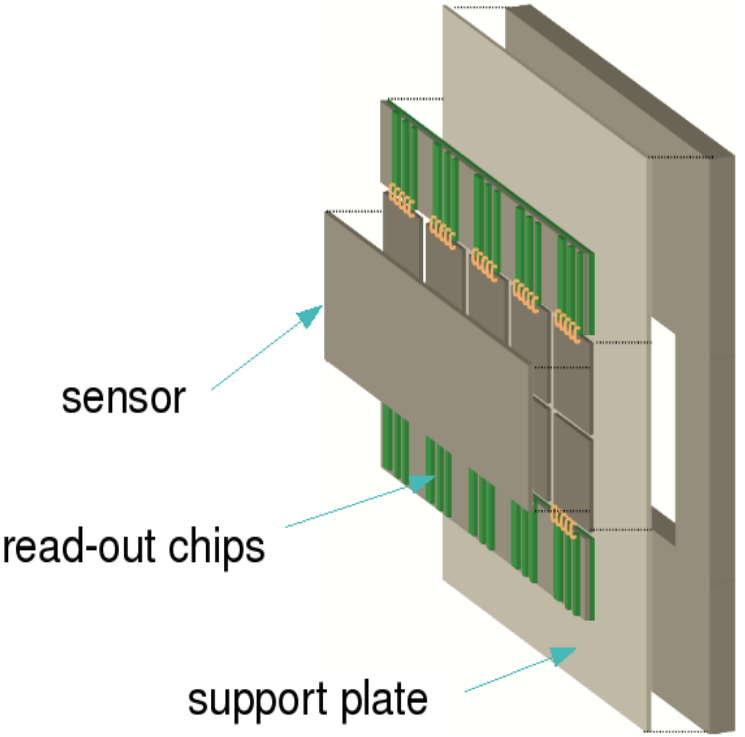
$$f \frac{t}{t_r} V_0 = \frac{t - t_d}{t_r} V_0 \qquad t_{zc} = \frac{t_d}{1 - f}$$

Constant fraction timing

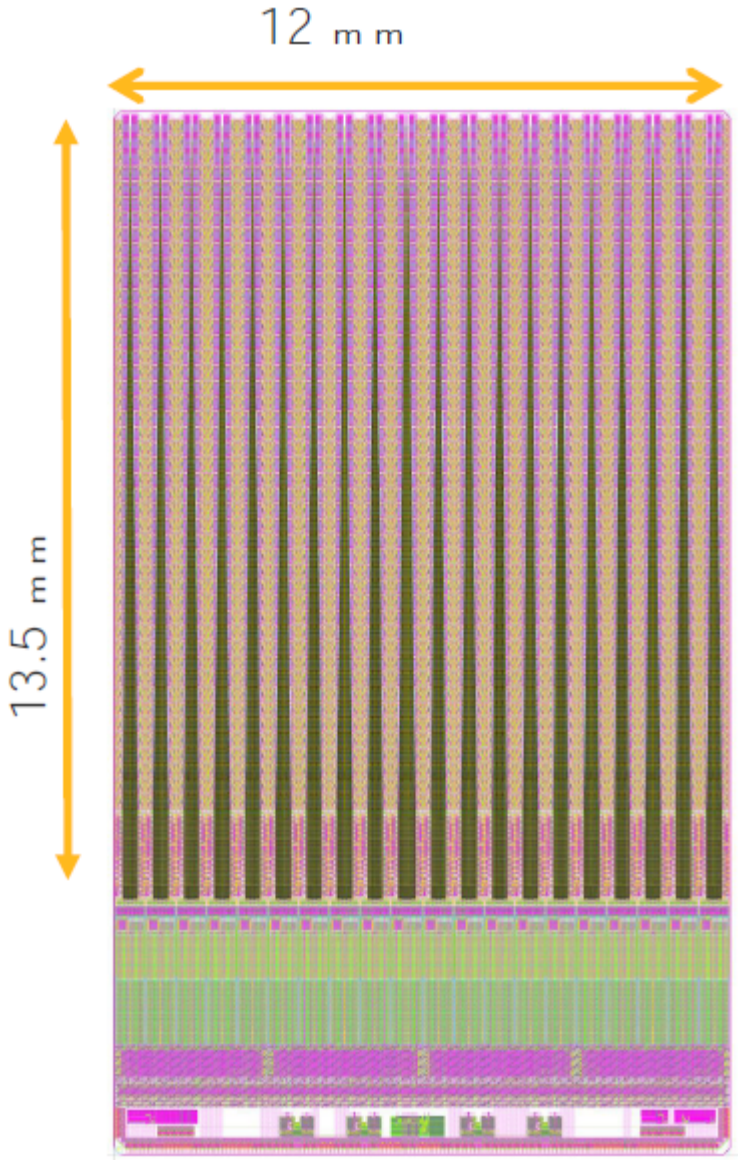
The NA62 Giga-TracKer (GTK)

- State of the art in high granularity, high time resolution trackers.
- Pixel size of 300 um x 300 um targeting 100 ps rms resolution.
- Sensor: standard hybrid pixels 200 um thick.
- Leading edge discriminator + ToT correction chosen as the timing extraction method.





TDCpix



- 1800 pixels organized in a 45 x 40 matrix
- Equivalent of 720 independent TDC channels with 97 ps binning
- TDC based on DLL.
- 4 x 3.2 Gbit/sec serializer
- CMOS 0.13 um

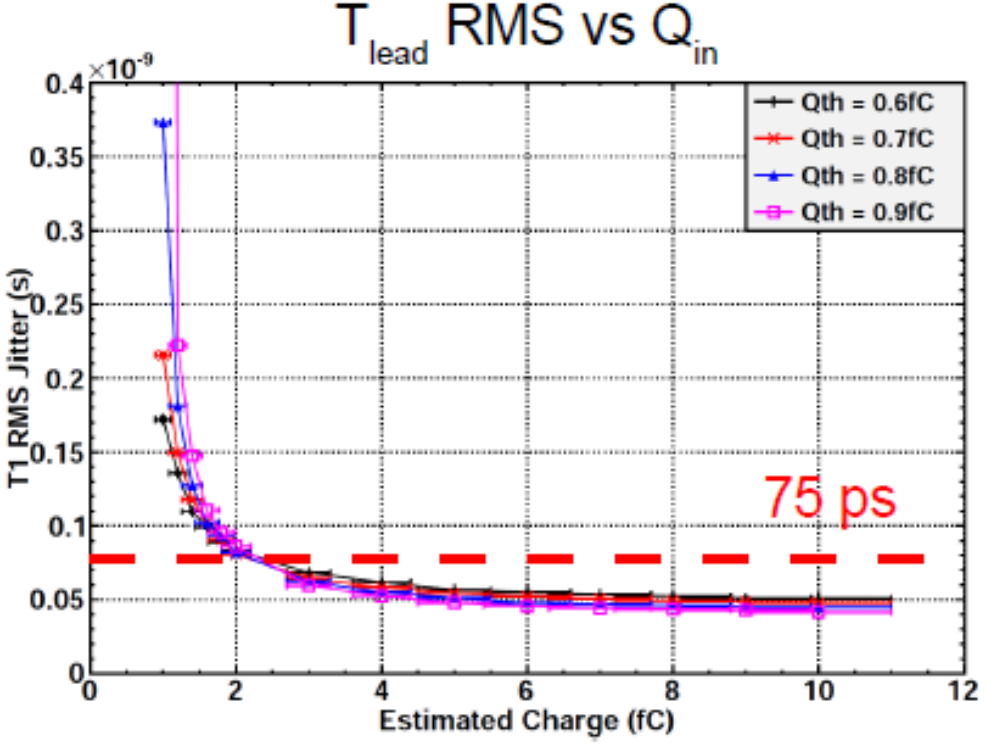
Design submitted to the foundry

A. Kluge et al, The TDCpix readout ASIC: A 75 ps resolution timing front-end for the NA62 Gigatracker hybrid pixel detector.

Nuclear Instr. Meth. A , available online 10 July 2013
http://dx.doi.org/10.1016/j.nima.2013.06.089

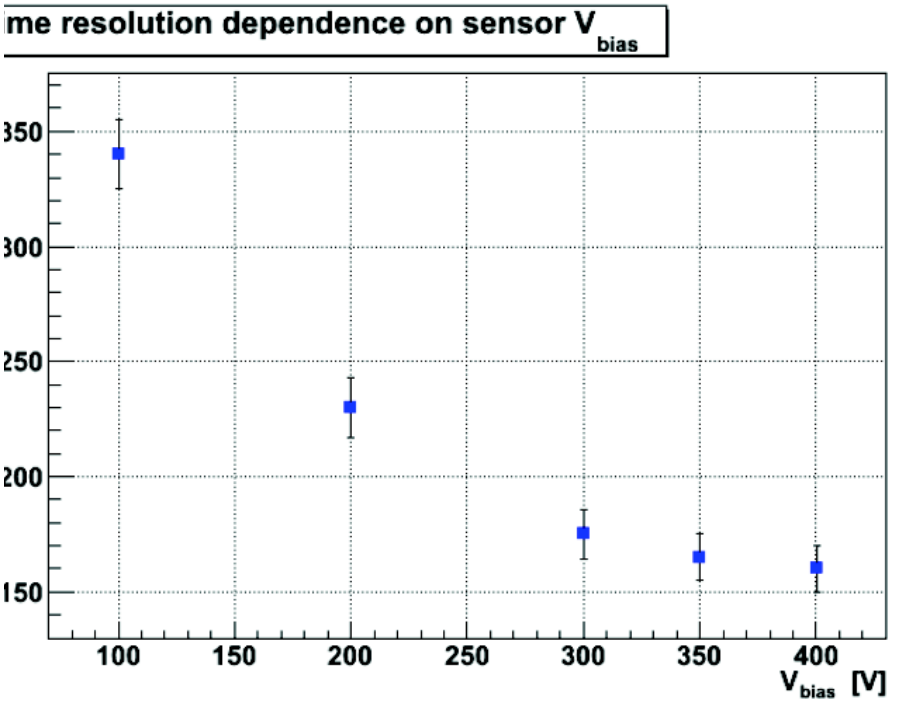
GTK prototype results

Jitter on the leading edge. Laser with 300 V sensor bias



Charge injection with laser
300 V detector bias

Resolution obtained in beam tests as a function of the sensor bias. ToT corrections applied.



Resultion worsening primarily due to distortion of the weighting field at the pixel edges, with an additional contribution from charge straggling.

Same charge, but different signal shapes

Plots courtesy of NA62/GTK project

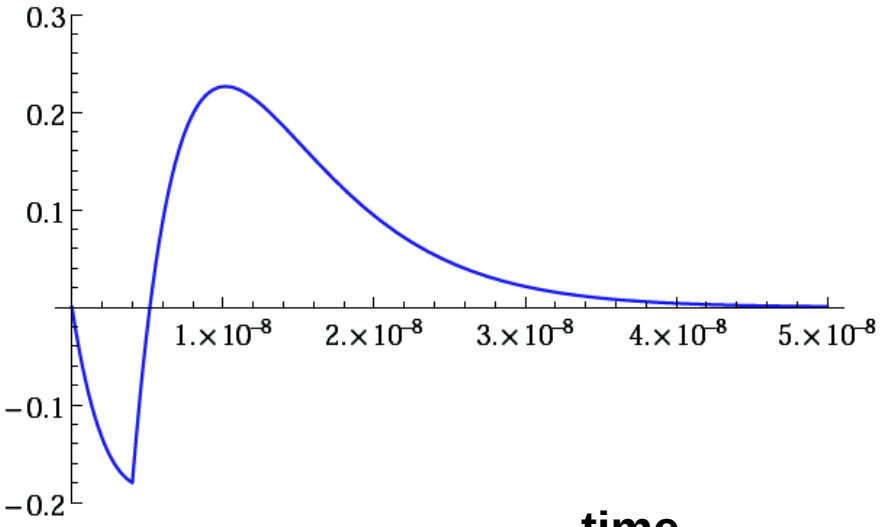
Timing with constant fraction

- Time walk is a **deterministic effect** and in principle it can be corrected for.
- However, signal shape variations imply **change** in the threshold crossing point even for the **same charge**.
- A constant fraction discriminator is immune to rise time variation **only if** the signal has a **linear rising edge**.
- How much is a CFD resistant to shape variations in more realistic cases?

$$\frac{t-t_d}{\tau}e^{-\frac{t-t_d}{\tau}} - f\frac{t}{\tau}e^{-\frac{t}{\tau}}$$

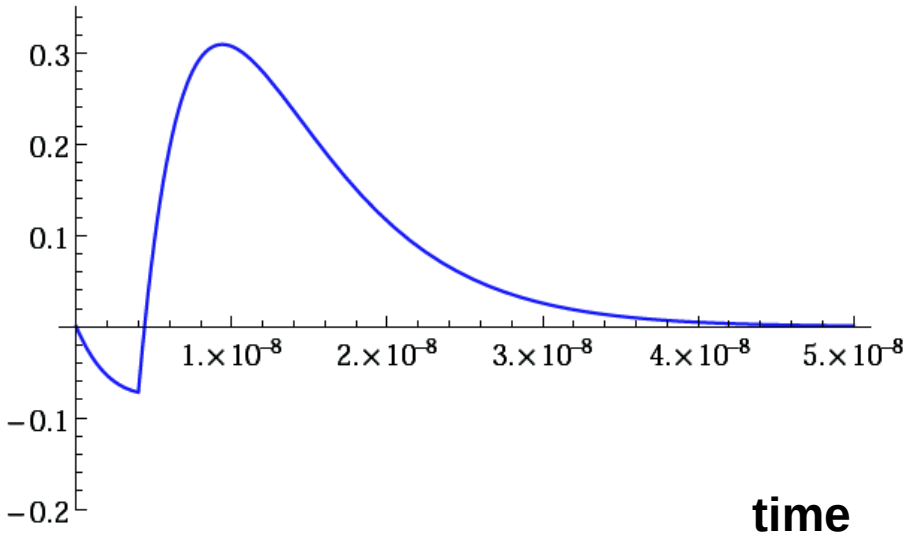
$$t_{zc} = \frac{t_d e^{t_d/\tau}}{e^{t_d/\tau} - f}$$

Amplitude



time

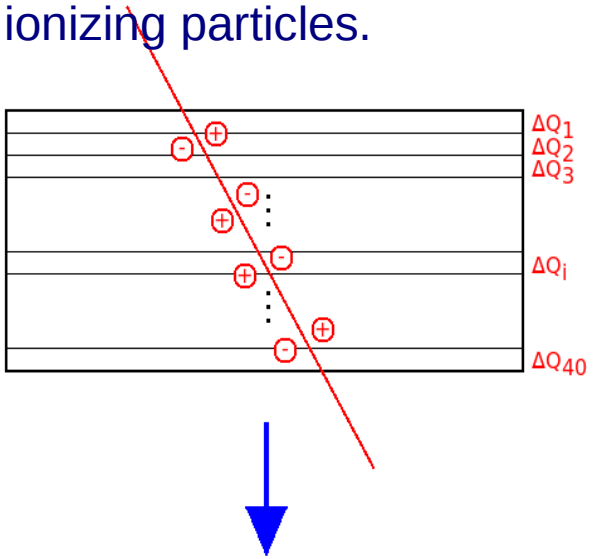
Amplitude



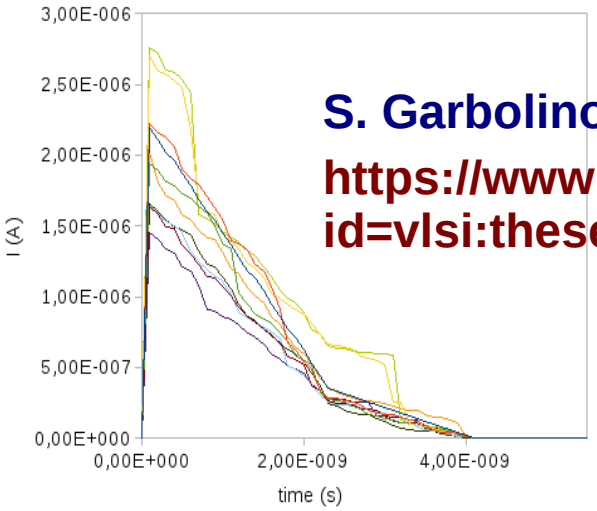
time

CFD simulation studies

Assume silicon sensor 200 um thick and minimum ionizing particles.

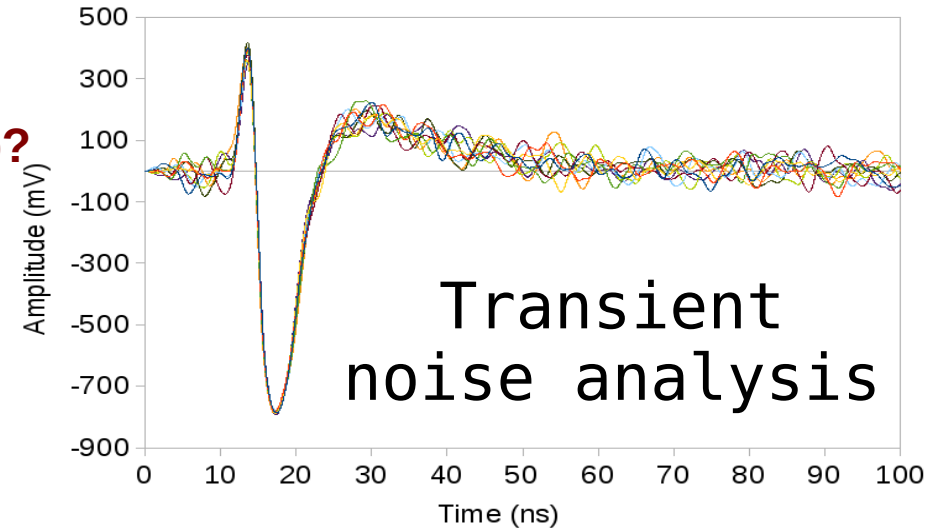


Schematic results			
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)	Time resolution (ps RMS)
Typical mean	40	20	53
$+1.5\sigma$	45	27	48
$+3\sigma$	52	23	59
-1.5σ	38	23	52
-3σ	38	21	67
Layout results			
Process corner	RMS Jitter @ 1MIP (ps)	Error due to signal variations (ps RMS)	Time resolution (ps RMS)
Typical mean	47	27	68
$+1.5\sigma$	50	31	55
$+3\sigma$	59	30	86
-1.5σ	44	27	65
-3σ	45	24	95



S. Garbolino, PhD thesis

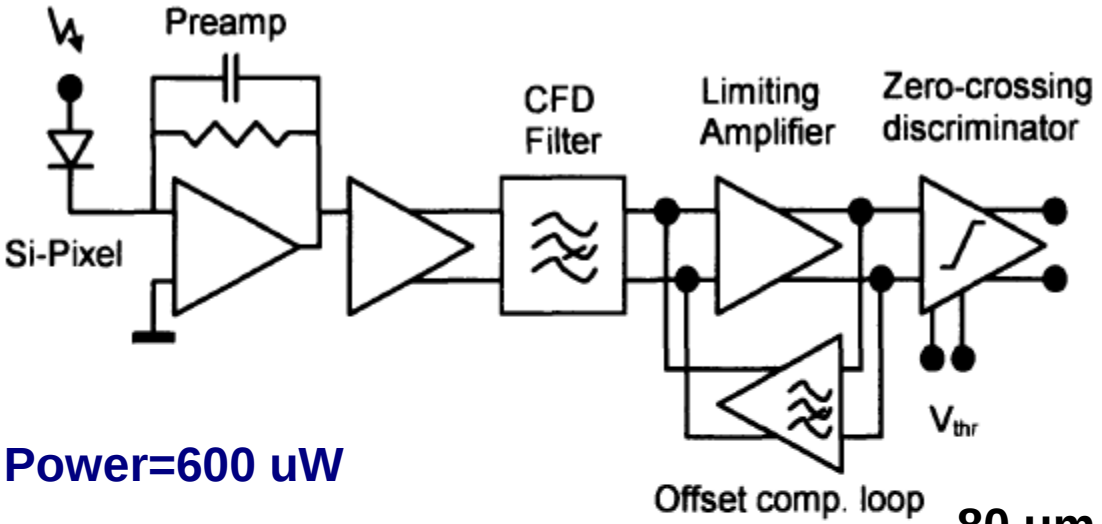
https://www.to.infn.it/doku.php?id=vlsi:theses:archive



Some considerations on CFD

- **Constant Fraction Discriminators can be effectively implemented in DSM technologies with moderate area and power.**

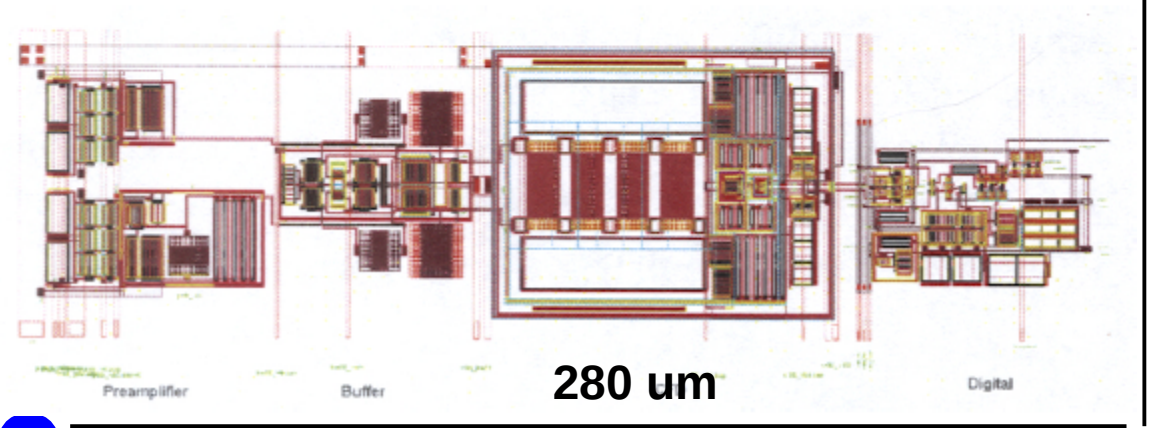
S. Martoiu et al,
IEEE NSS-Mic 2008



Power=600 uW

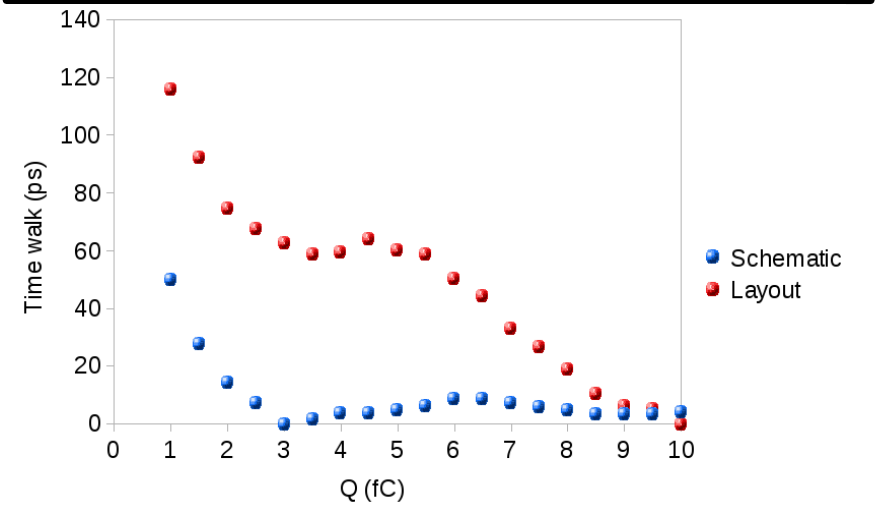
80 um

Fig. 1. Architecture of the front-end circuit.

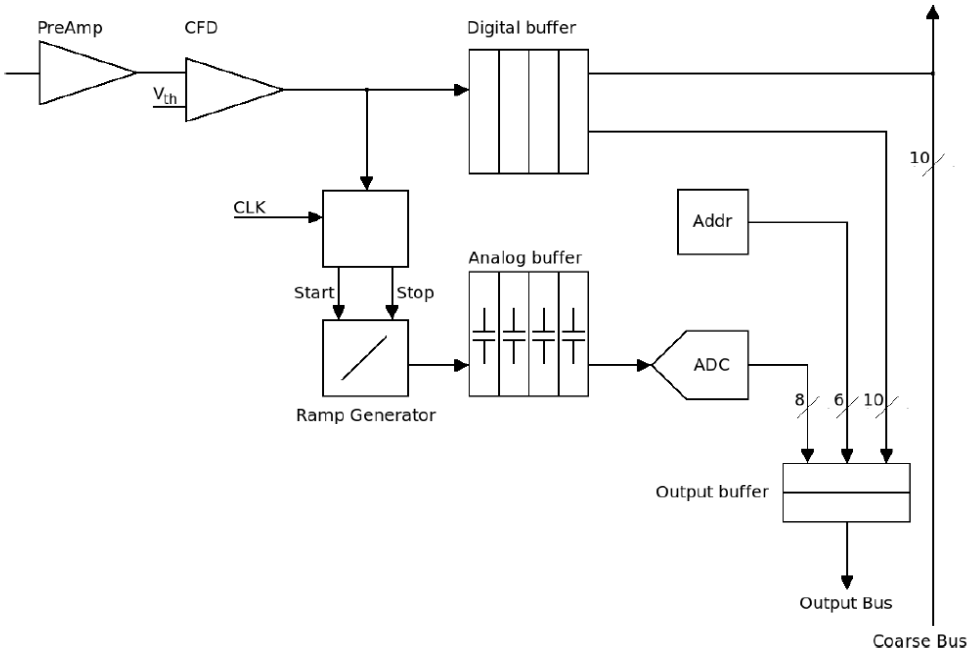


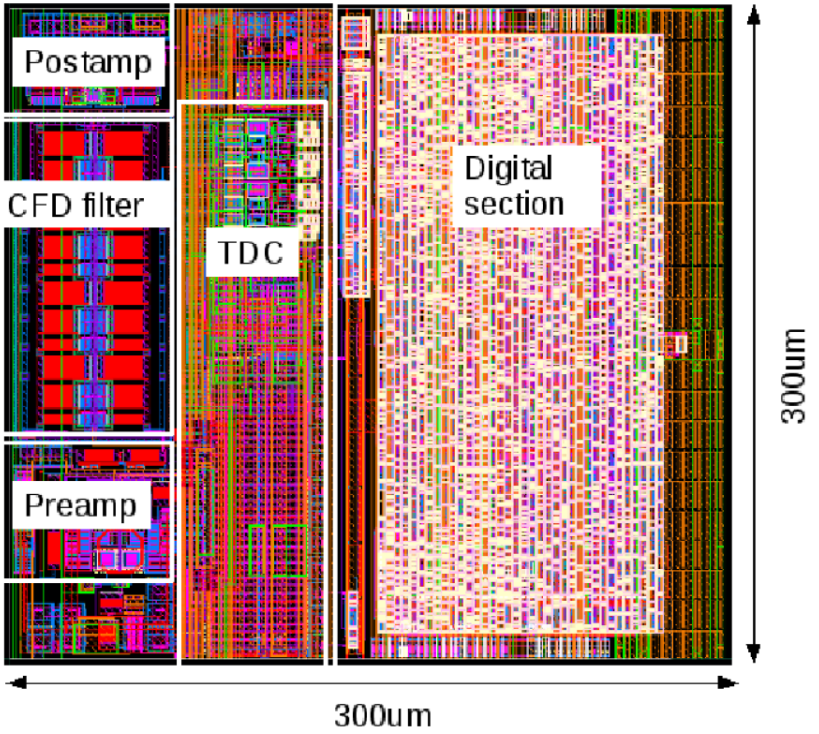
280 um

- **CFD are effective in reducing effects relating to signal shape variations, but they are not the magic toolbox for perfect timing.**
- **CFD rely on linear filtering and performance can be easily corrupted if nominal pulse shape is distorted (layout, substrate noise, etc...)**



Pixel with embedded TDC





- **Preamp. CFD, TDC incorporated on 300 um x 300 um**
- **Power 1mW/ch**
- **250 kHz rate capability**
- **Major issue: preserve the CFD from digital noise aggression**
- **Development triggered by na62**
- **Did not reach maturity on time for an early use in the experiment, but very useful playground for other developments.**

Example of time-based front-end

M. Rolo, Integrated Circuit Design for Time-of-Flight PET with Silicon Photomultiplier.

8th "Trento" Workshop on Advanced Silicon Radiation Detectors, Feb. 2013

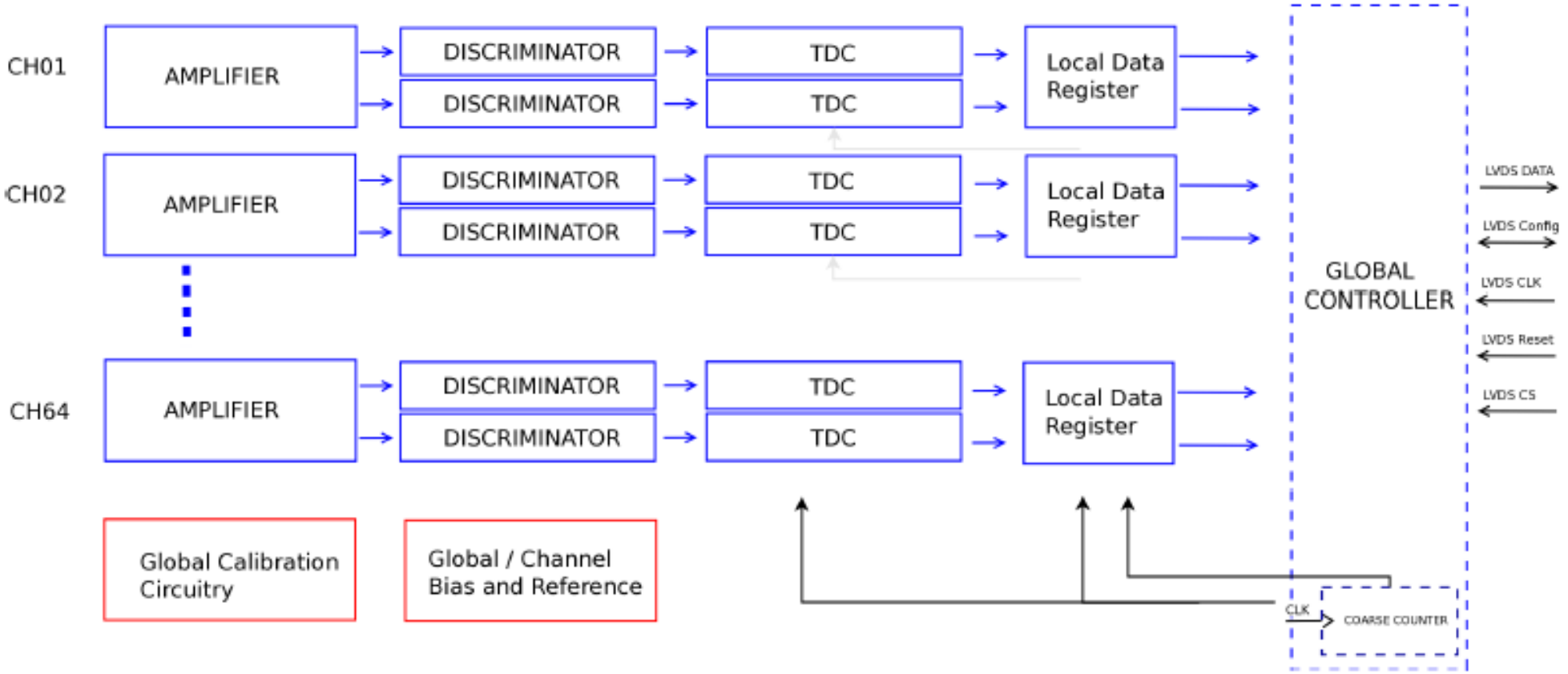
https://indico.cern.ch/contributionDisplay.py?sessionId=7&contribId=38&confId=226647

TOF-PET ASIC specifications

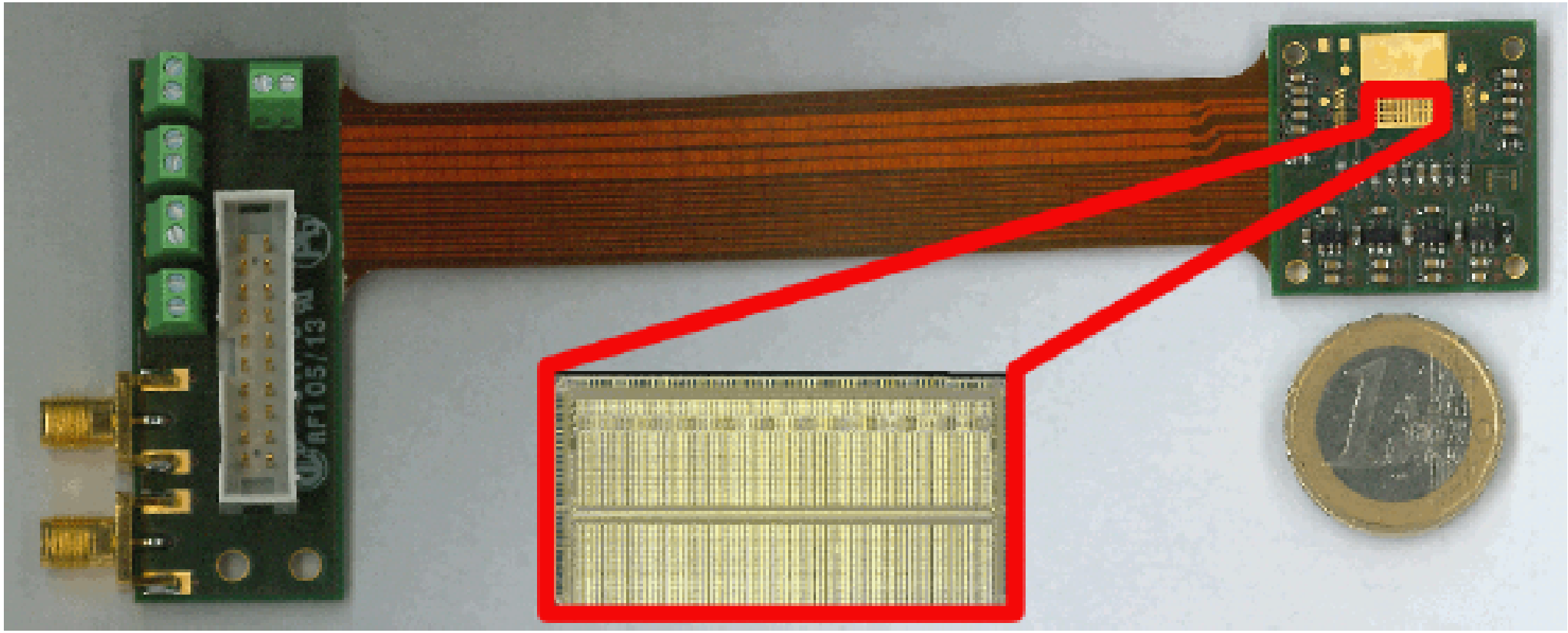
Parameter	Value
Number of channels	64
Clock frequency	80 – 160 MHz
Dynamic range of input charge	**300 pC**
SNR (Q_{in} = 100 fC)	> 20-25 dB
Amplifier noise (in total jitter)	< 25 ps (FWHM)
TDC time binning	**50 ps**
Coarse gain	G_0, $G_0/2$, $G_0/4$
Max. channel hit rate	100 kHz
Max. output data rate	320 Mb/s (640 w/ DDR)
Channel masking	programmable
SiPM fine gain adjustment	**500 mV (5 bits)**
SiPM	up to 320pF term. cap., 2MHz DCR
Calibration BIST	internal gen. pulse, 6-bit prog. amplitude
Power	**< 10 mW per channel**

How these specs impact the choice
of the readout chip architecture?

ASIC architecture

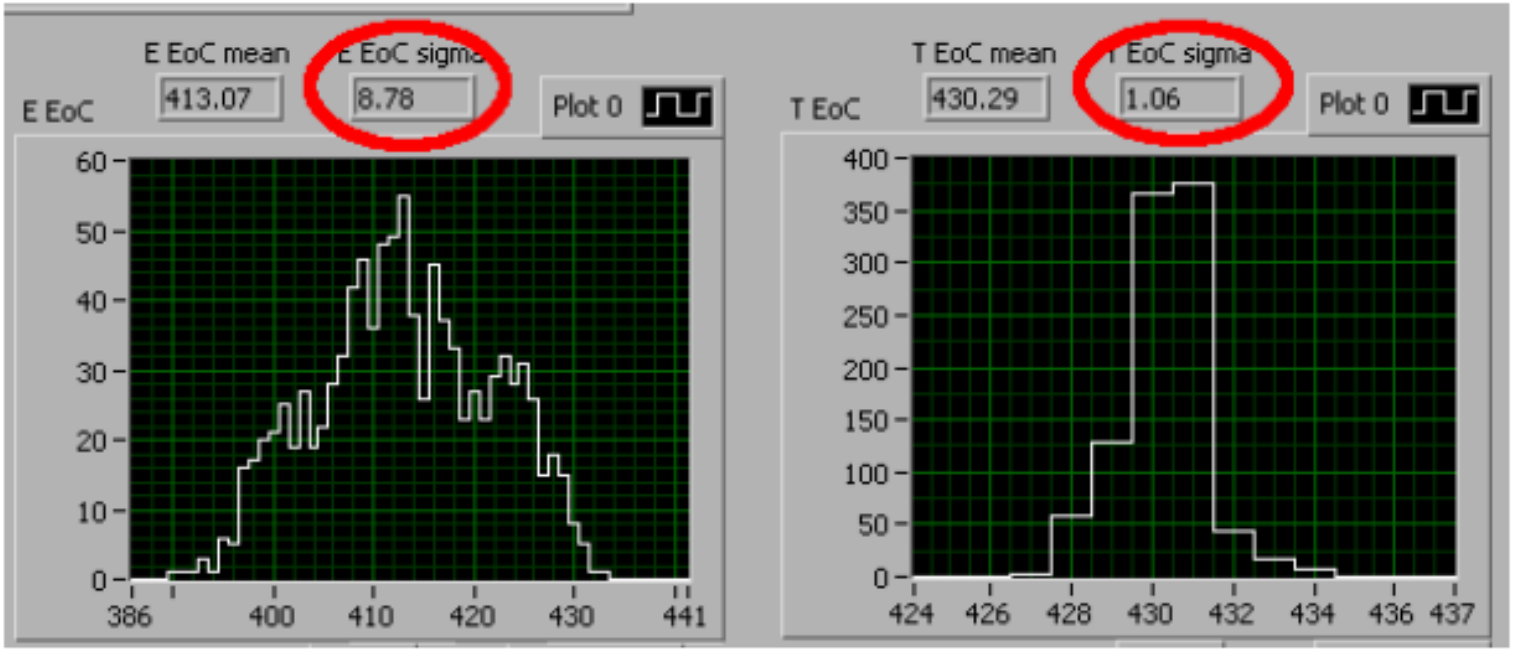


One of the test PCB



Other test PCBs developed at LIP (Lisbon) to accommodate packaged dies.

Some performance example



- **TP jitter + FE jitter + TDC noise ≈ 60 ps FWHM**, using the id of the TDC buffer.

More on fast ADCs

26.4 A 3.1mW 8b 1.2GS/s Single-Channel Asynchronous SAR ADC with Alternate Comparators for Enhanced Speed in 32nm Digital SOI CMOS

Lukas Kull[1,2], Thomas Toifl[1], Martin Schmatz[1], Pier Andrea Francese[1], Christian Menolfi[1], Matthias Braendli[1], Marcel Kossel[1], Thomas Morf[1], Toke Meyer Andersen[1], Yusuf Leblebici[2]

[1]IBM Research, Rüschlikon, Switzerland, [2]EPFL, Lausanne, Switzerland

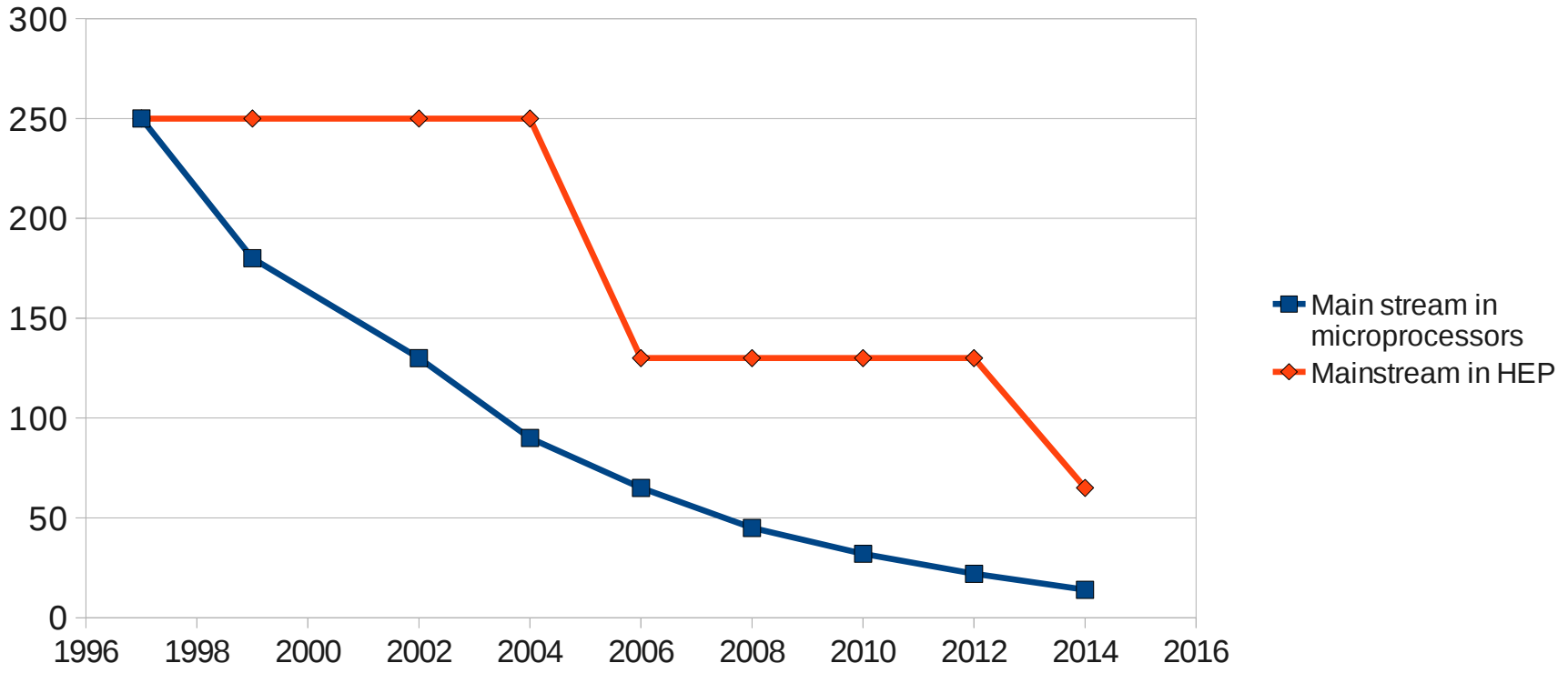
Specifications	[1]	[2]	[3]	[4]	[5]	This work		
Architecture	SAR	Ti-SAR	Ti-SAR	SAR	SAR	SAR		
CMOS Technology (nm)	65	65	65	28	40	32		
Resolution (bits)	8	6	8	8	6	8		
Supply Voltage (V)	1.2	1.2	1.0	1.0	1.0	1.0	1.1	0.9
SNDR near Nyquist (dB)	44.5	31.5	42.75	43.3	30.5	39.3	39.3	38.8
Sampling Speed (GHz)	0.4	1	1	0.75	1.25	1.2	1.3	1.0
Speed per Channel (GHz)	0.4	0.5	0.5	0.75	1.25	1.2	1.3	1.0
Power (mW)	4.0	6.7	3.8	4.5	6.08	3.1	4.2	2.0
FOM (fJ/conf step)	73	210	24	41	178	34	43	28
Area (mm^2)	0.024	0.11	0.013	0.004	0.013	0.0015		
Area for 64GS/s (mm^2)	3.8	7.0	8.3	0.26	0.67	0.080	0.074	0.096

A 9-bit 50MS/s Asynchronous SAR ADC in 28nm CMOS

Tuan-Vu Cao, Snorre Aunet, Trond Ytterdal
Circuits and Systems group, Department of Electronics and Telecommunications
Norwegian University of Science and Technology, Norway
Emails: {vu.tuan.cao, snorre.aunet, trond.ytterdal}@iet.ntnu.no

- Simulations indicate that 9 bit and 50 MS/s are achievable with 45 uW of power!
- Digitization and basic DSP functions at 50 MS/s could be achieved with 150 uW of power per channel (excluding the very front-end part).

Industry vs HEP



- **MPW: 15 mm2 in 28 nm: 156 000 (standard), 189 000 SOI**
- **1 mm2: 15 000 euros**
  http://cmp.imag.fr/products/ic/?p=prices