Commissioning of the Read-Out Driver (ROD) card for the ATLAS IBL detector and upgrade studies for the Pixel Layers 1 and 2

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Outline

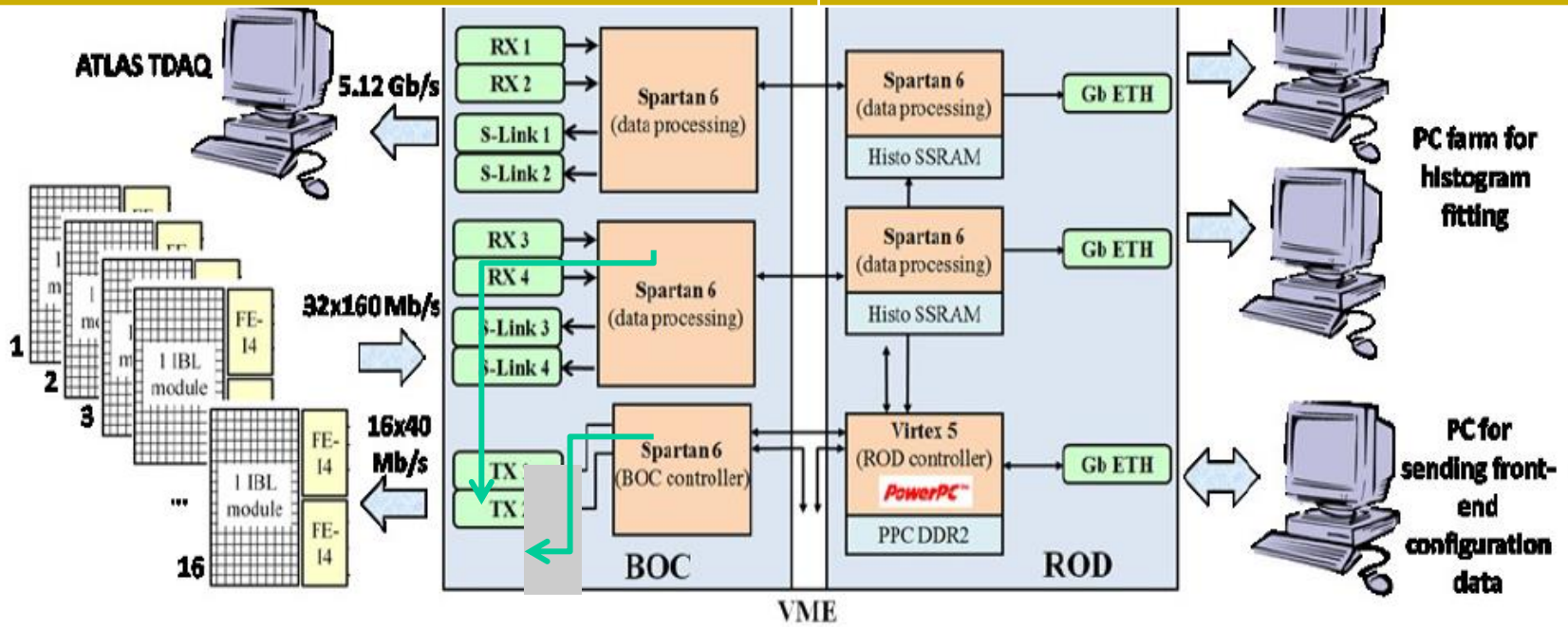
- ROD card status
- Pixel ROD vs IBL ROD
- Ongoing ROD tests
- Plans for IBL ROD production
- Proposals for outer layers of Pixel Detector

Basics

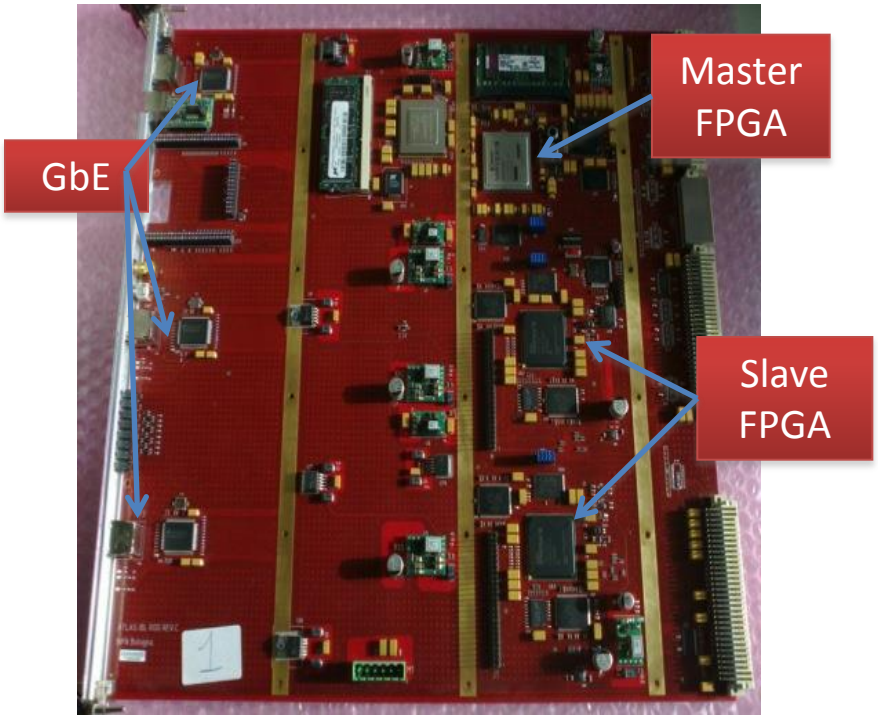
- **IBL ROD started from pixel ROD**
- **VME 9U backward compatible card**
  - Some ways to also connect IBL ROD to pixel BOC
- **IBL ROD extends modularity by a factor of 4**
  - 32 FEI4 chips, 4 SLinks
- **IBL ROD FW started from "Berkeley FW"**
  - Only calibration fits have moved to external PCs (two Gb/s Ethernet ports)
- **All other ROD pixel functions are only being adapted to the new ROD**
- **Extra features were added**
  - Possibility to work Off-crate
  - USB port on the front panel
  - Third Gb/s-Ethernet port to upload microblaze SW or data for testing aims
  - Possibility to exclude the VME and control everything under Gb/s-Ethernet

Read-out System Overview

Number of IBL Staves /ROD-BOC pair	14
# DAQ Modules per ROD-BOC pair	16
# FE-I4s chip per ROD-BOC pair	32
Total # of FE-I4s in IBL	448 (32*14)
Number of Pixels per FE-I4	26880
Total # of read-out channels	~12 M



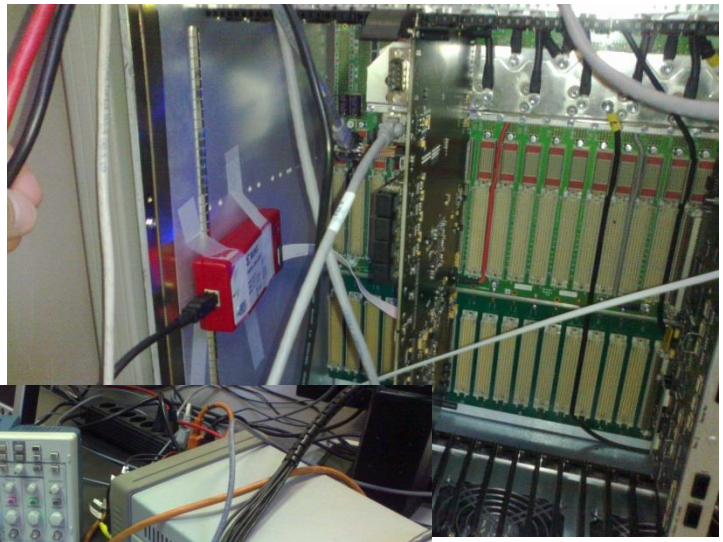
IBL Readout Driver

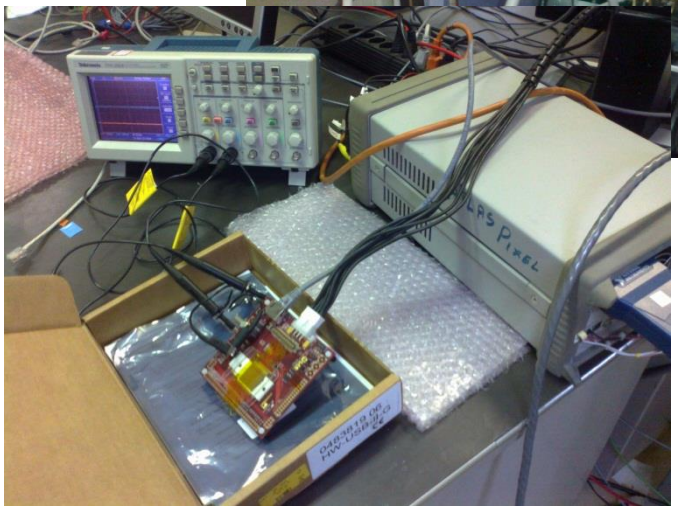


ROD RevC

- Control card
  - Steering of detector
    - Configuration
    - Commands
  - Detector calibration by steering the calibration scans
  - Physics data taking
    - Trigger sending, event building
  - Histogramming for calibration and monitoring
- Master FPGA:
  - Control data generation
  - Run control (calibration scans and data taking)
- Slave FPGAs:
  - Data interface to and from Back of Crate Card
  - Data formatting and event-fragment building, histogramming

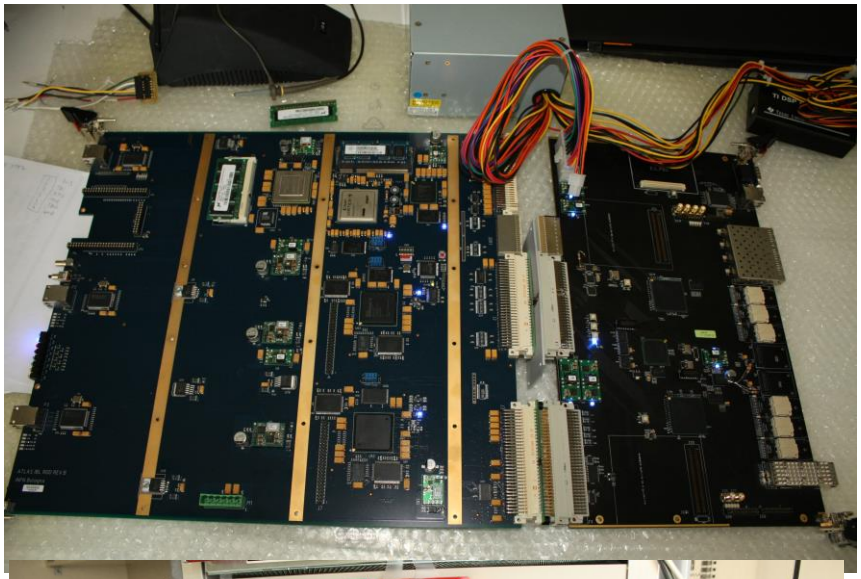
Some pictures

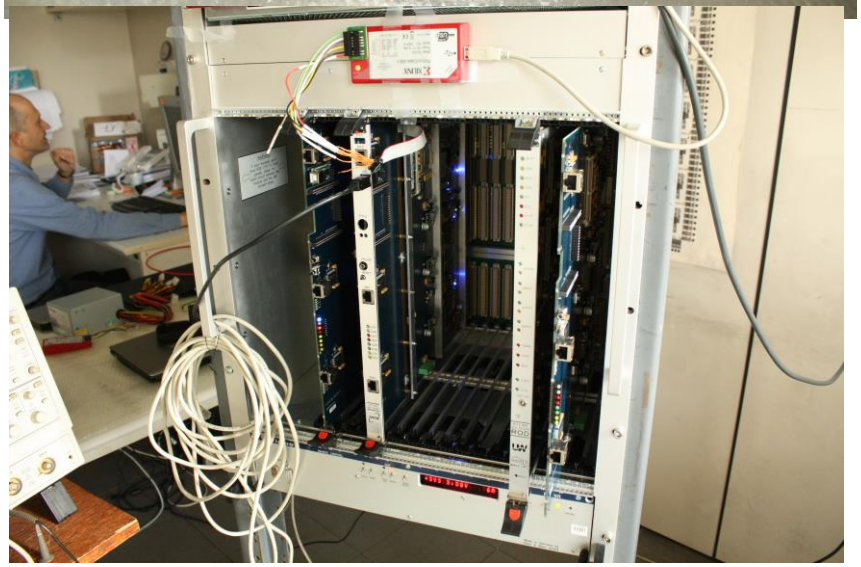




System test in the Pixel-Lab

BOC-ROD off-crate test



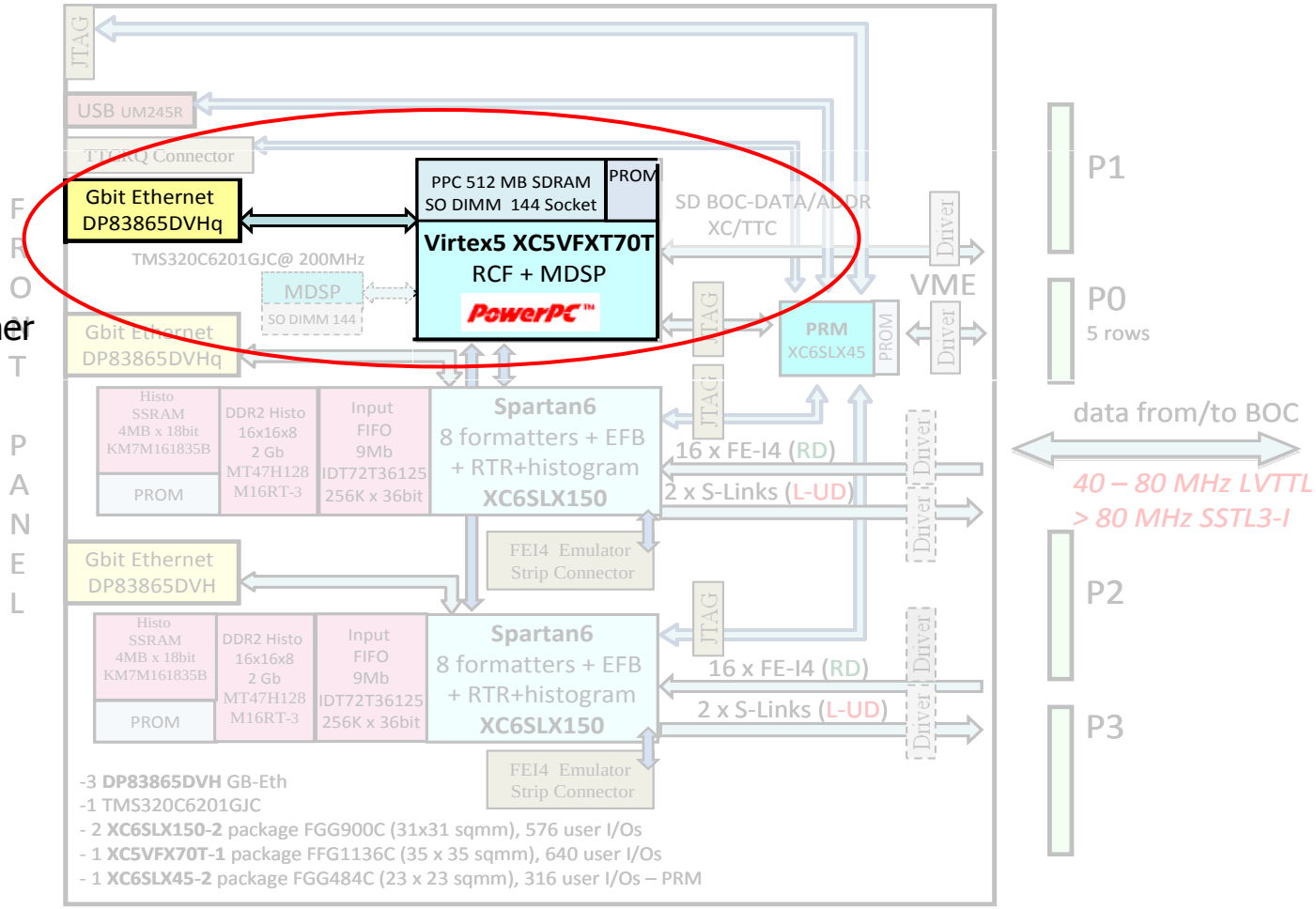


BOC-ROD on-crate test

Firmware wrt “old pixel ROD”

- **Power PC-based system: HW-SW**

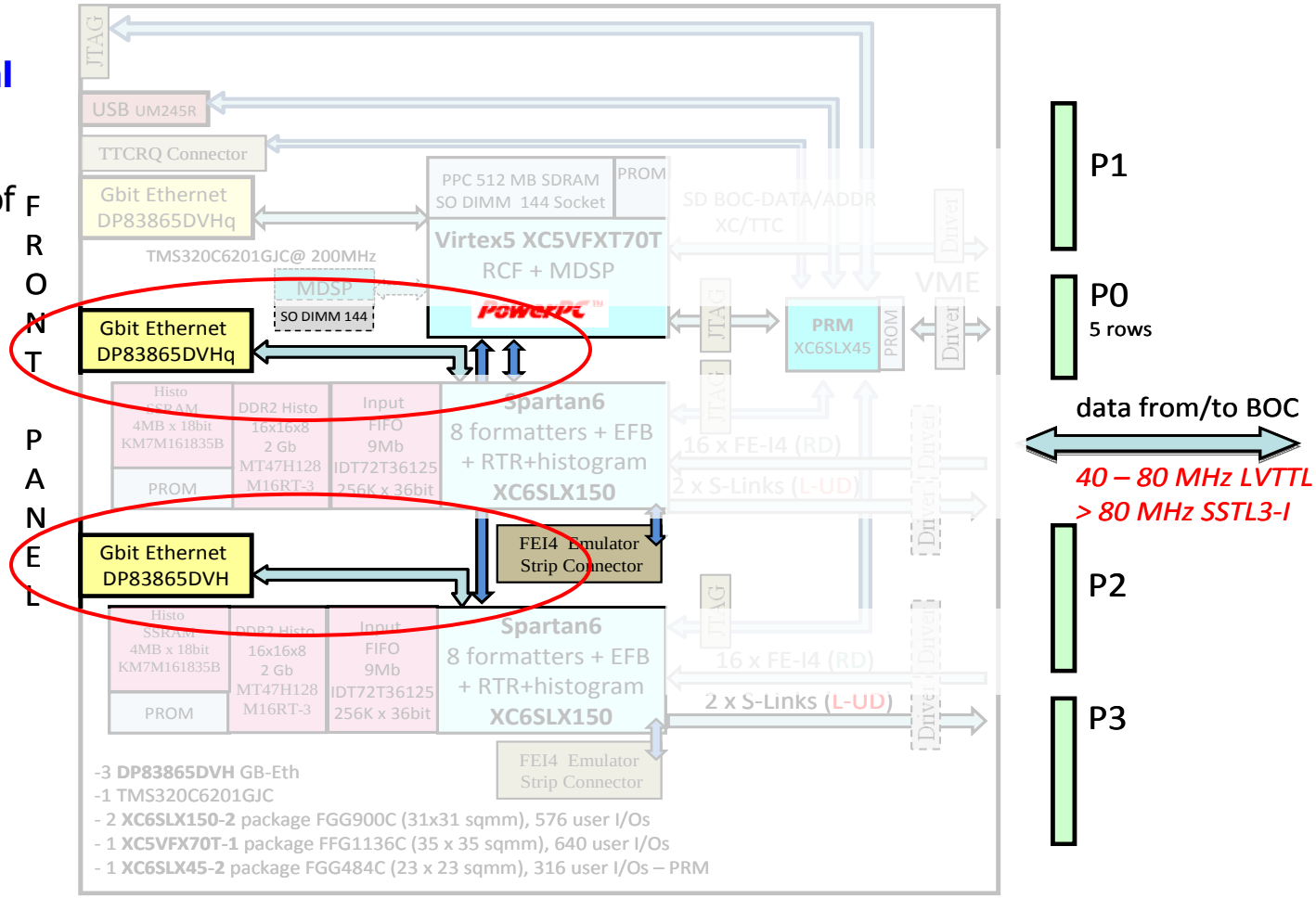
The MDSP C-code of the “old pixel ROD” has been integrated into the Virtex5 PowerPC and simulated together with the VHDL code



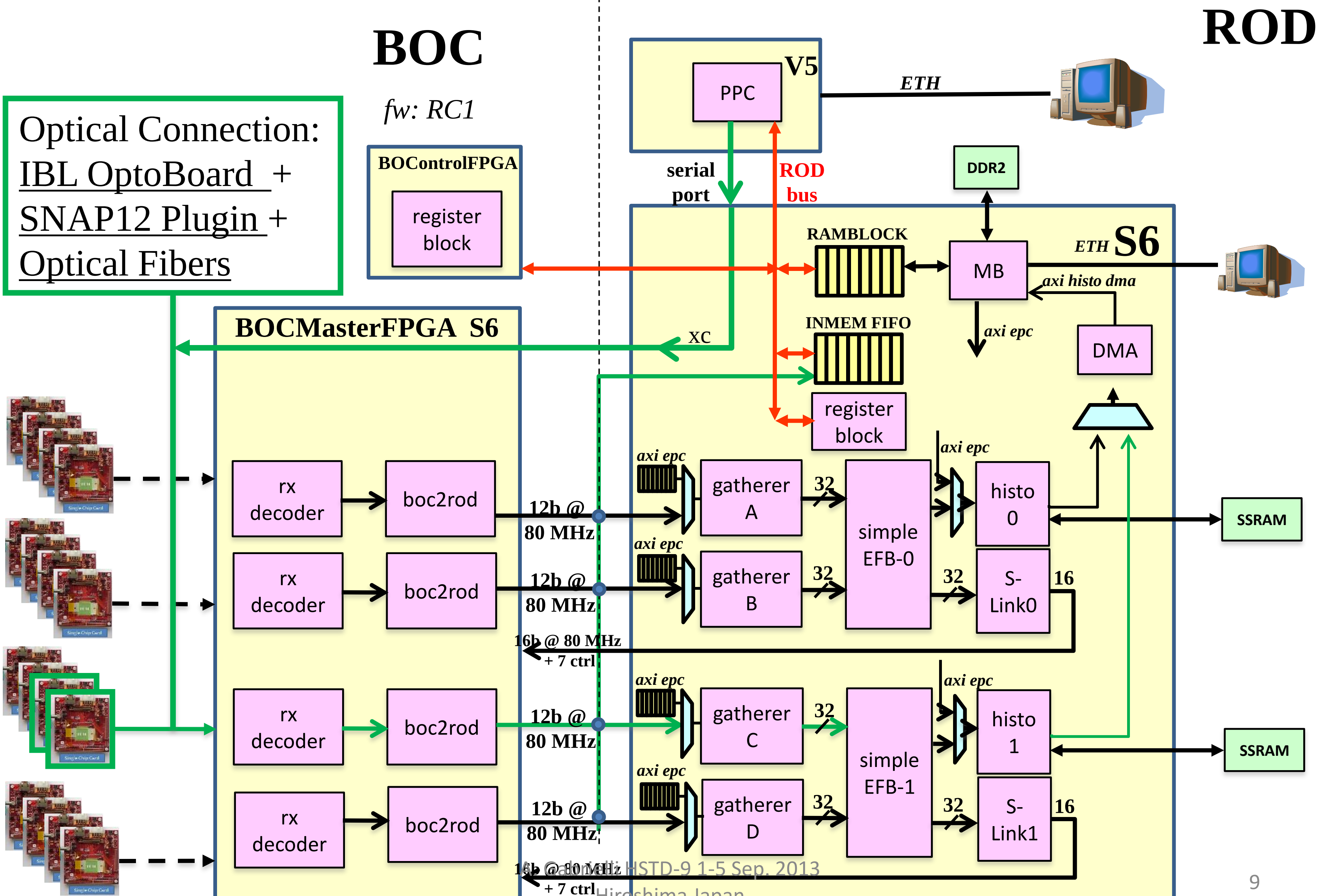
Firmware wrt “old pixel ROD”

- **Histogramming moved to external PC-GPU farm**

The SDSP functionality of the “old pixel ROD” has been moved externally via two Gb/s Ethernet ports



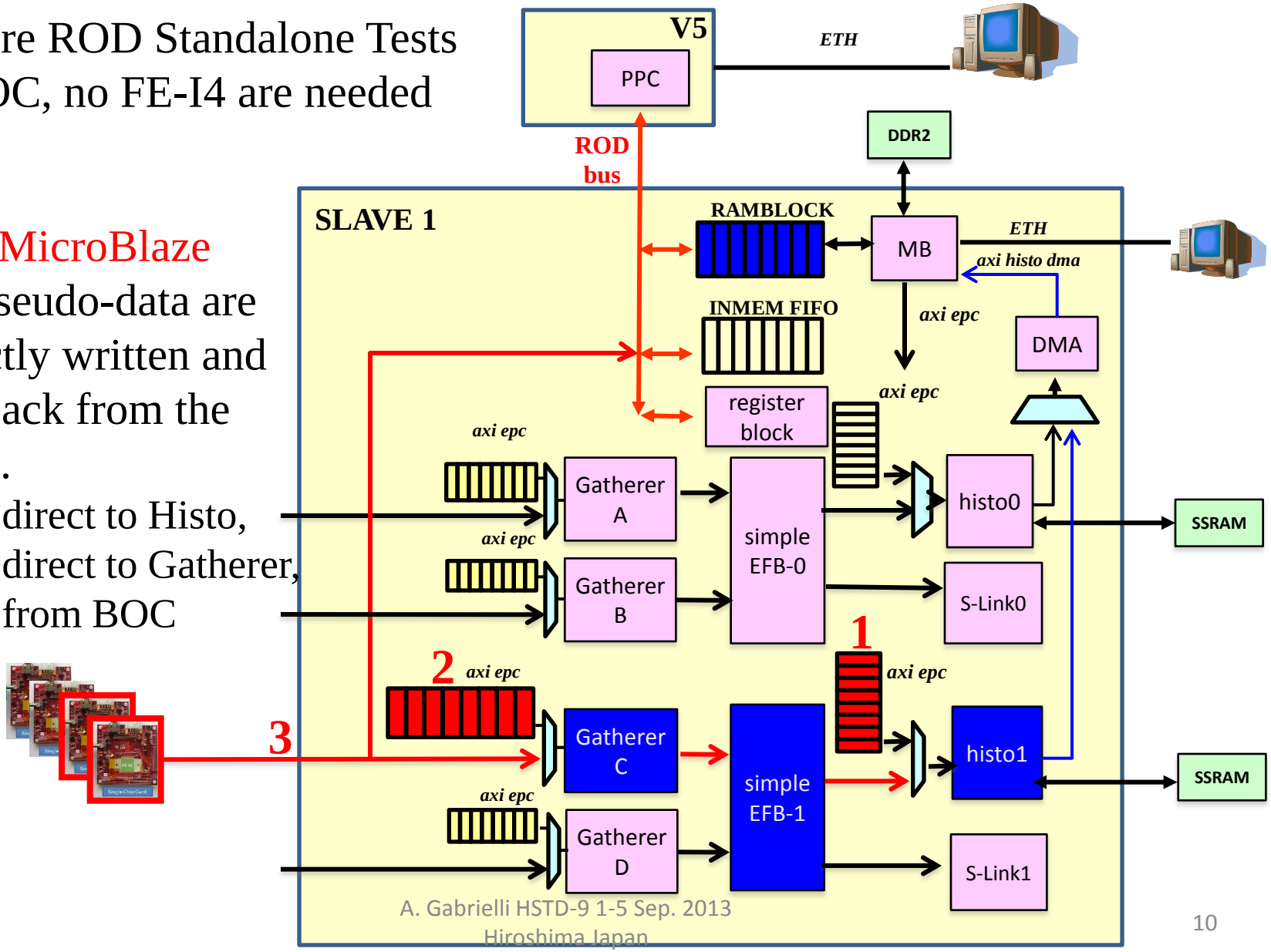
BOC/ROD Firmware overview



FW for the Histogrammer tests

1 and 2 are ROD Standalone Tests
→ no BOC, no FE-I4 are needed

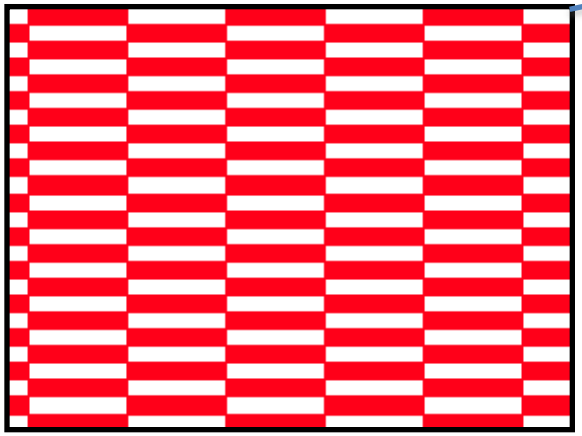
- From MicroBlaze
  The pseudo-data are correctly written and read back from the slaves.
- Step 1 direct to Histo,
- Step 2 direct to Gatherer,
- Step 3 from BOC

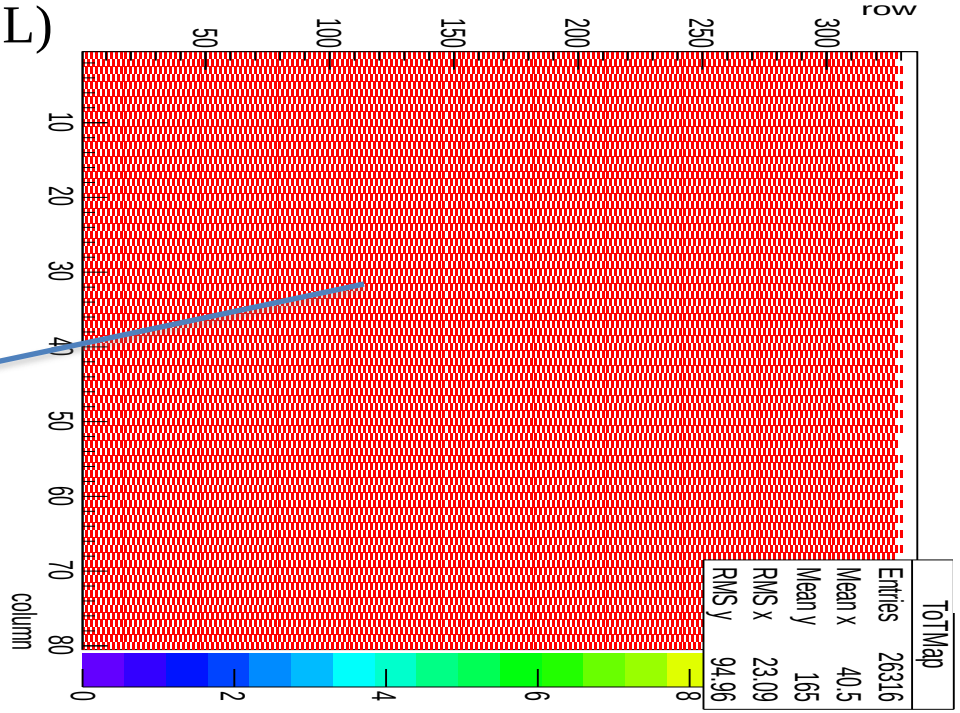


Ongoing ROD tests

Besides all the previous BOC-ROD tests some new HW tests are ongoing

- **FEI4B-ROD** communication: digital scan test with pixel mask
- ToT scan on FEI4_B chip
  (green FEI4_B board from LBL)

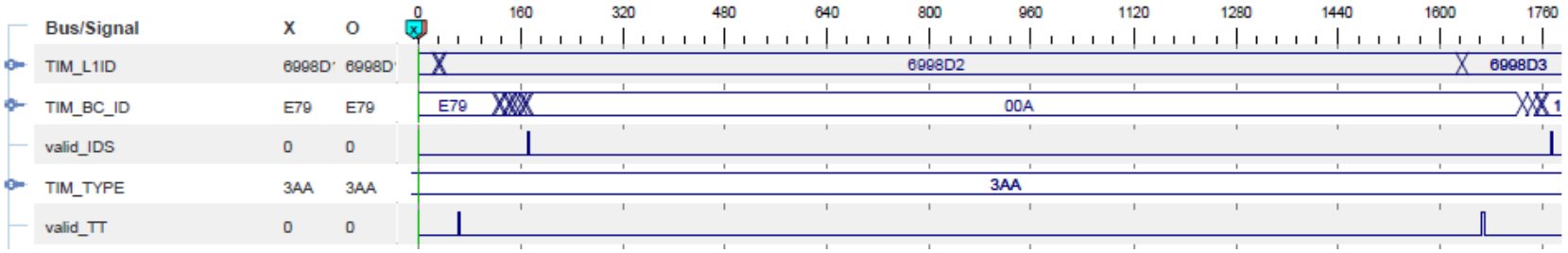




Operation with the TIM

TIM – BOC - ROD communication seems ok!

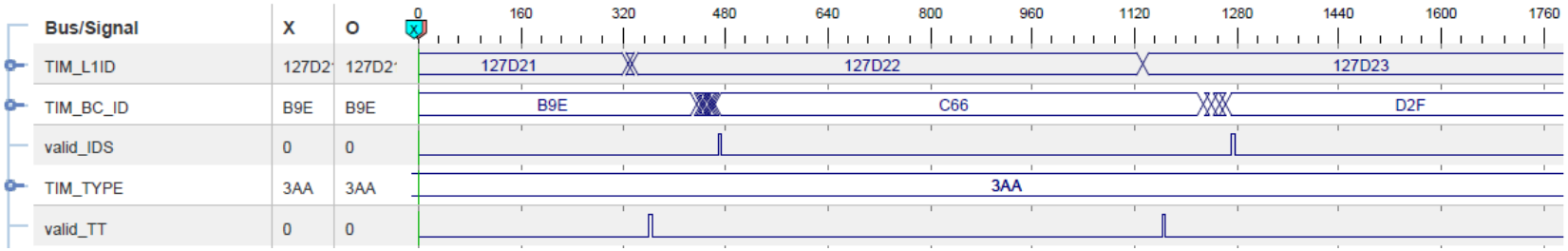
•The TIM board, (TIM 2C) is the same as the one in Bologna, however with different firmware version.



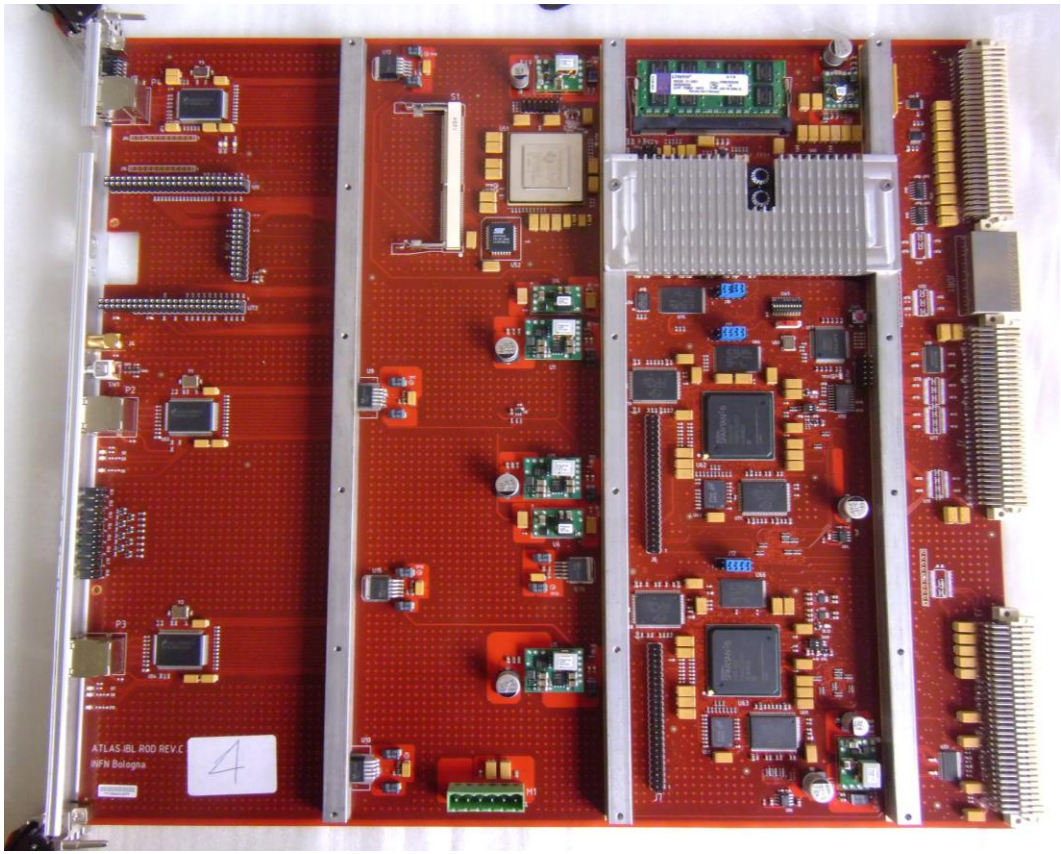
•**LV1_ID** are correctly incremented and received from the ROD. No error seen, no fluctuation of **LV1_ID** has been detected so far.

•Changing the frequency of the trigger we see a coherent change in Chipscope signals.

•**TT also checked**.



IBL ROD (rev C) Bologna 14-layer card



14 Required + spares for IBL

5 Already test-card produced

15 under production

Rev C under test in Bologna and at CERN

- **no issues so far**
- firmware under development by the pixel collaboration
- tests with BOC rev B

Ongoing ROD tests

Besides all the previous BOC-ROD tests some new HW tests are ongoing

ROD firmware upload

- configuration via VME, through *Program-Reset-Manager* **OK**
- FW and SW for embedded processors via VME **OK**

BOC-2-ROD

- clock-phase, I/O terminations **OK**
- Predefined pattern sent to ROD, cross-checked with memory block on Spartan6, tested with Chipscope **OK**
- Cross-check of SSTL3_I signals received from BOC with and w/o terminations (revB vs revC)
  clock phase spectrum enhanced with terminations
  Acceptance window widens

Ongoing ROD tests

Besides all the previous BOC-ROD tests some new HW tests are ongoing

TIM-2-ROD communication

- Serial streams from TIM to ROD have been tested **OK**
- LV1ID counter, Bunch Crossing ID (BCID) and Trigger Type (TT) **OK**

ROD Internal Bus and RAM checks

- PowerPC program fills a RAM block on Virtex5,
  then data sent to Spartan6, cross-checked with Chipscope, **OK**

Communication towards histograms

- **Spartan6-External SSRAM *on-ROD communication* OK at 100 MHz**

ROD IBL production and testing procedures

- **IBL ROD production**
- List of minimal procedures to validate the ROD cards after production
  - Firmware-software upload from VME, JTAG and Gb/s-Ethernet ports
  - ROD-2-BOC dataflow over all I/O lines
  - R/W tests for Virtex5 and Spartan6 external memory modules
  - Dataflow tests on the 3 Gb/s ports
  - TIM card connectivity test

- Test committed-delegated to the ROD manufacturing company
  This is the same we asked for ROD ver B and C cards
  - Electrical test after component supply
  - XRay test for large BGA-packaged components

  - **15 RevC IBL ROD board production started on August 26th 2013**
  - **Boards are expected on the first week of October**
  - **Distribution to CERN might start at the end of October**

Plan for ROD of Layer 2

NEEDS:

26 Boards + spares, same numbers as current Pixel Detector
Still use of IBL boards for ATLAS Pixel Layer 2

Options for ATLAS Layer2 ROD production

- **A everything from the beginning to the end: like for IBL**
- **B** board production, assembly, tests and firmware support components provided via CERN (even partially)
- **C** components, board production and tests done via third party Bologna provides firmware support only

ISSUE: Time schedule of Layer 2 overlaps IBL schedule

Plan for ROD of Layer 1

NEEDS:

38 Boards + spares, same numbers as current Pixel Detector

Too early for a reasonable schedule for Layer 1 but it seems reasonable use IBL boards for Layer1

Options:

- Buy the components for the boards along with those for Layer 2
- Wait after IBL and Layer 2 will be mounted

Conclusion

Big effort from where we started from for …

- ROD design, production, tuning of the cards
- Mechanics, Heat-Sink for Virtex5, board rigidity
- Firmware test
- Firmware development and support
- From 2009, 12 ROD boards have been produced starting from scratch:
  - **2 were the very first prototypes**,
  - the other **10 (5+5) are in hands and working**
- **IBL ROD production is ongoing**

We can propose to repeat the same roadmap for Layer2

Whatever needed for **Layer 1** will be probably postponed after IBL and Layer 2 commissioning; only components might be bought earlier