

Commissioning of the Read-Out Driver (ROD) card for the ATLAS IBL detector and upgrade studies for the Pixel Layers 1 and 2

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During the first shutdown of the LHC collider in 2013/14, the Atlas experiment will be equipped with an innermost silicon layer, called IBL. Read-out electronics have been redesigned in order to accomplish the IBL performances. A new front end ASIC (FE-14) has been designed as well as new off-detector devices. The latter are two 9U-VME cards called Back-Of-Crate and Read-Out Driver (ROD). The ROD is devoted to data processing, configuration and control of the overall read-out electronics. After the first prototyping samples a pre-production batch has been delivered with a finalized layout. Actual production of the ROD cards is scheduled on summer 2013 and commissioning on 2014. This contribution describes the setup, the tests carried out for the commissioning of the IBL ROD cards and, in general, for the acquisition system. In particular, it will be shown how integration tests have been performed by increasing the level of system complexity: slices of the IBL read-out chain have been instrumented and ROD performances are verified in a test bench mimicking a small-size final setup. This contribution will report also an outlook on the possible adoption of the IBL ROD for ATLAS Pixel Layer 1 and 2. The higher luminosity that will be expected for LHC after future upgrades will require more performances for the acquisition system, especially in term of throughput. Estimation of future needs for the electronics of Layer 1 and 2 will be shown and it will be discussed whether the adoption of the IBL ROD card or its upgraded version could be a viable solution.

Primary author: GABRIELLI, Alessandro (Universita e INFN (IT))

Co-authors: FALCHIERI, Davide (Universita e INFN (IT)); BALBI, Gabriele (Universita e INFN (IT)); BINDI, Marcello (University of Bologna); TRAVAGLINI, Riccardo (Universita e INFN (IT))

Presenter: GABRIELLI, Alessandro (Universita e INFN (IT))

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