Trigger-less readout architecture for the upgrade of the LHCb experiment at CERN

Topical Workshop on Electronics for Particle Physics (TWEPP2013)
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Federico Alessio, CERN
on behalf of the LHCb Collaboration
Outline

• Introduction to LHCb and current performance

• Motivations for an upgrade of the LHCb detector
  o Current limitations

• Detector Upgrade

• Readout Architecture Upgrade
  o FE Trigger-less electronics
  o Readout Control and clock
  o DAQ technologies

• Outlook on plans and future running conditions
Current LHCb detector

LHCb proved itself to be the **Forward General-Purpose Detector** at the LHC:

- forward arm spectrometer with unique coverage in pseudorapidity
  - $2 < \eta < 5$, 4% of solid angle
- catching 40% of heavy quark production cross-section
- precision measurements in beauty and charm sectors
  - $\Delta p / p = 0.4\%$ at 5 GeV/c, IP resolution 20 $\mu$m for high-pT tracks, decay time resolution 45 fs for $B_s \rightarrow J/\psi \, \phi$ and $B_s \rightarrow D_s \, \pi$
  - collected 3 fb$^{-1}$ with >90% efficiency (>99% offline/online)
Current LHCb detector

- Particle ID
- Calorimeters
- Muon
- Vertexing
- Tracking
- First-level HW trigger
Current LHCb readout architecture

- **Front-End**
  - First-level HW trigger
  - L0 trigger
  - LHC clock

- **Back-End**
  - Event size ~65 kB
  - Output rate of processed events 5 kHz

- **Processing FARM**
  - ~29000 cores

- **Storage**
  - MON farm

- **Timing & Fast Control System**
  - Max bandwidth ~1.1 MHz

- **Detector**
  - Use of TTCrx
  - ~250 Readout Boards (TELL1)
  - ~1 Tb/s event building network

- **Event building**
  - Event Requests

- **READOUT NETWORK**
  - FE
  - Readout Board
  - SWITCH
  - SWITCH
  - SWITCH
  - SWITCH
  - SWITCH
  - SWITCH
  - SWITCH

Federico Alessio
Upgrading LHCb

The amount of data and the physics yield from data recorded by the current LHCb experiment is limited by its detector, readout technologies and hardware trigger.

While LHC accelerator will keep steadily increasing …

- energy / beam (3.5 → 4 → 6.5 TeV → …)
- luminosity (peak 8x10^{33} → 2x10^{34} cm^{-2}s^{-1} → …)

… LHCb will stay limited in terms of

- data bandwidth: limited to 1.1 MHz / 40 MHz max
- physics yields for hadronic channels at the hardware trigger
- detectors degradation at higher luminosities
Upgrade Strategy

Remove first-level hardware trigger!
→ accept all LHC bunch crossing: trigger-less Front-End electronics

Current

Upgrade

1MHz event rate

40MHz event rate

~1Tb/s

~40 Tb/s

Courtesy K. Wyllie
Implications of upgrade strategy

Removal of first-level hardware trigger implies:

• **read out every LHC bunch crossing**
  o trigger-less Front-End electronics
  o multi-Tb/s readout network

• **fully flexible software trigger**
  o full event information available on processing node to improve trigger decision
  o maximize signal efficiencies at high events rate

• **reach higher luminosities**
  → redesign (incompatible) sub-detectors for a peak luminosity of $20 \times 10^{32}$ cm$^{-2}$s$^{-1}$

• **more data by increasing bandwidth**
  → redesign readout architecture to record 40 MHz events
Upgraded LHCb Detector

- Particle ID
- Replace HPDs + electronics

- New Vertex Detector

- Calorimeters
  - Reduce PMT gain + new electronics

- New Tracking stations

- Muon new electronics

→ See Poster Session and backup slides for details
Upgraded LHCb readout architecture

HW trigger kept as a handle to allow staging

For full details see Electronics Architecture of the LHCb Upgrade LHCb-PUB-2011-0011
Compress (zero-suppress) data already at the FE
  • reduce # of links from ~80000 to ~12500 (~20 MCHF to ~3.1 MCHF)
  • data driven readout (asynchronous) + variable latencies!

Efficiently usage of link bandwidth for data
  • pack data on data link continuously with elastic buffer
  • extensive use of GBT (robust FEC or WideBus mode)
    ✓ evaluate choices based on complexity vs robustness
Efficient data packing mechanism

Average event size

Link bandwidth

Average event size = link bandwidth

Buffer depth

Header is the unique identifier for each event in frame
✓ Compulsory (tag for each LHC crossing)
✓ Programmable in its content (must contain length of frame and BXID)
✓ Used by readout board to decode and separate frames
Fast & Slow Control to FE

Separate links between controls and data

- A lot of data to collect
- Controls can be fanned-out (especially fast control and clock)

Compact links merging Timing, Fast and Clock (TFC) and Slow Control (ECS).

- Extensive use of GBT as Master GBT to drive Data GBT (especially for clock)
- Extensive use of GBT-SCA for FE configuration and monitoring
Detector links

**Generic Link:**
GBT + Versatile Link + commercial components

**Duplex Master Control Link (2,500):** Fast & Slow Control + Clock

**Simplex Data Link (12,500):** Data

Ken Wyllie, CERN
FPGAs in FE?

Main advantage $\rightarrow$ re-programmability
- tune algorithms
- scale system

Good past experience with flash FPGAs (ACTEL/MICROSEMI)
Irradiation program (OT) with full TDC code, 320MHz from internal PLL

Reconfig fails  PLL lock error

$\rightarrow$ See W. Wink in Poster Session
From timing and clock point of view, need to ensure constant:

- LATENCY: Alignment with BXID
- FINE PHASE: Alignment with best sampling point

Master GBT used as current TTCrx at FE
- Must maintain constant phase and latency
- Local adjustment at FE

Resynchronization mechanisms must be envisaged:
- To recover from desynch as fast as possible
- Possibly automated in firmware
Back-End: new LHCb TELL40

**Classical approach:** ~0.5 Tb/s data aggregator board with 10 GbE to FARM

- 24 inputs @ 4.8 Gb
- GBT format
- 12 outputs/inputs @ 10Gb ethernet

96 inputs @ 4.8 Gb → processing in FPGA → 48 x 10G ethernet ports

→ See JP Cachemiche in xTCA Working Group
TELL40 AMC

Ready now.
ATCA40 = 4 x TELL40

Under test.
Common firmware development

Common firmware across various sub-systems
→ user code changes the flavors of the board

Common software to control the board
→ based on current LHCb ECS

Minimize:
→ Unconformities
→ Manpower
Sub-detector user code logic

Readout board must support asynchronous readout!
→ Alignment block to realign all inputs and create an event packet
Mini-DAQ system

A small readout slice on the table
→ Full AMC40 card + Credit-Card size PC + interface to FARM + all flavors of firmware in one card

Used as a common test bench for
• developing code
• test logic
• optimize resources
• test beams

Common simulation framework based on Mini-DAQ under development

→ FE electronics will be validated both in simulation and with the Mini-DAQ to enforce specs compatibilities
Mini-DAQ is here
LHCb readout slice

Same ATCA board used in different flavors:
same generic hardware, different firmware

replicate for as much as needed (scalable)
Counting rooms in the surface

- Max of ~300 m from FE to Readout Boards (TELL40)
- Can use cheapest commercial links (compact network)
- Easiest operation (accessibility)
- Tests with proto FE and TELL40 show that his works well with excellent margins

→ See R. Schwemmer in Poster Session
Classical DAQ event-builder

Diagram showing a network setup for TELL40s Force10 Switches, with 40GbE and 10GbE connections, and sub-farms with Z9000 (16x 40GbE + 64x 10GbE) and Force10 Switch/Router.
Alternative proposal: bi-directional event-builder network
Alternative proposal: readout board for bi-directional network

PCIe Gen3 NIC cards (PCIe40), with FPGAs and ~150 Mb/s throughput to host PC

- Technologically-independent, i.e. take advantage of latest technology
  - host PC acts as FARM PC already: open choice for interface technology as late as possible and very compact network
- Cost effective as removes one optical interconnect (to the processing FARM)
- Put everything in a box, keep distances short, reduce costs for interconnects and network switches
- Commercially available

Proposal currently under investigation
LHCb upgrade plan

- Upgrade TDRs
- Tendering & Serial production
- Quality control & acceptance tests
- Installation & commissioning upgrade (18 months to plan!)

2014 - 2022
- LHC LSI
- LHC Run II
- LHC LSII
- LHC Run III
- LHC LSIII

Technical reviews & technology choices (ongoing now!)

for high-lumi LHC $L_{\text{peak}} > 5 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
An upgrade plan of the LHCb experiment has been laid out

- Aim at collecting 10x more data and 20x more hadronic events

LHCb upgrade is **technologically challenging** and time wise tight

- Trigger-less, ~40 Tb/s network, minimize number of components
- Optimize costs and manpower: be smarter …
- R&D, specs, evaluation, validation are ongoing.

**CERN endorsed the LHCb Upgrade by fully approving it!**
(this time we showed off our muscles)

We have exciting times ahead in 2014 and beyond!
(and not just because of the World Cup…)

Grazie per l’attenzione!
Backup
LHCb data taking plan

- **LHCb startup**
- **LHCb collected ~3 fb^{-1}**
- **LHCb to collect 5-7 fb^{-1}**
- **Upgrade!**

**2010**

- **LHC Run I**
  - $E = 7(2010-2011) \& 8(2012) \text{ TeV (pp)}$ @ 50 ns
  - $E = 2.76 \text{ TeV (Pb}^+\text{Pb}^-)$
  - $E = 5 \text{ TeV (pPb}^+)$

**2011**

- **LHC Run II**
  - $E = 13 \text{ TeV (pp)}$ @ 25 ns
  - $L_{\text{peak}} = 2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
  - $E = 2.76 \text{ TeV (Pb}^+\text{Pb}^-)$

**2012**

- **LHC Long Shutdown I**
  - LHC splices repair + consolidation

**2013**

- **LHC Run II**
  - $E = 13 \text{ TeV (pp)}$ @ 25 ns
  - $L_{\text{peak}} = 2 \times 10^{34} \text{cm}^{-2}\text{s}^{-1}$
  - $E = 2.76 \text{ TeV (Pb}^+\text{Pb}^-)$

**2014**

- **LHC Long Shutdown I**
  - LHC splices repair + consolidation

**2015**

**2016**

**2017**

**2018**

TWEPP2013, 23-27 September 2013, Perugia, Italy

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LHCb has **excellent performance**:

- **luminosity leveling** at constant $4 \times 10^{32} \text{ cm}^{-2}\text{s}^{-1}$ with a constant $\sim 1.5$ interactions per LHC crossing
  - ✔️ $> 2\times$ designed values!
- $>3$ fb$^{-1}$ data recorded with overall efficiency $\sim 93\%$
- $>99\%$ detector channels working and operational
- $>99\%$ of online data good for offline analysis
- $>96\%$ efficiency for long tracks in track reconstruction
- $>90\%$ ParticleID efficiencies
Running Conditions 2010-2012

#Colliding bunch pairs
Visible crossing rate
<Pileup>
\[\text{MHz}\]\(10^{30}\text{ cm}^{-2}\text{s}^{-1}\)

Inst. luminosity

LHCb Design

Exploratory

Sept 2010   Apr 2011   Apr 2012

Courtesy R. Jacobsson
LHCb Control Room

2010 - 2012

• 2010: Operated with two non-expert shifters plus a VELO closing manager
• 2011 – 2012: Operated with two non-expert shifters
  ➔ Experiment highly automated and computer voice assisted for information, warnings/alarms and instructions
LHCb is continuously generating excellent physics results:

$$BR(B_s \to \mu^+\mu^-) = 2.9^{+1.1}_{-1.0} \times 10^{-9} \ (4.0\sigma)$$

**B**$^+$ $\rightarrow$ **K**$^+$ $\mu^+\mu^-$ resonance

**B**$^+$ $\rightarrow$ **K**$^-$ resonance

**B**$^0_s$ mixing

CP Violation in decays of **B**$^0_s$ mesons

+ >100 papers and high quality results
LHCB physics prospects

Expect to collect a total of \(\sim 8 \text{ fb}^{-1}\) of data up to 2018 and 50 \text{ fb}^{-1}\) of data after 2018 \(\rightarrow\) moving towards precision of theory

<table>
<thead>
<tr>
<th>Type</th>
<th>Observable</th>
<th>Current precision</th>
<th>LHCb 2018</th>
<th>Upgrade (50 fb(^{-1}))</th>
<th>Theory uncertainty</th>
</tr>
</thead>
<tbody>
<tr>
<td>(B_s^0) mixing</td>
<td>(2\beta_s (B_s^0 \rightarrow J/\psi \phi))</td>
<td>0.10 [9]</td>
<td>0.025</td>
<td>0.008</td>
<td>(\sim 0.003)</td>
</tr>
<tr>
<td></td>
<td>(2\beta_s (B_s^0 \rightarrow J/\psi f_0(980)))</td>
<td>0.17 [10]</td>
<td>0.045</td>
<td>0.014</td>
<td>(\sim 0.01)</td>
</tr>
<tr>
<td></td>
<td>(A_{b_s}(B_s^0))</td>
<td>(6.4 \times 10^{-3}) [18]</td>
<td>0.6 \times 10^{-3}</td>
<td>0.2 \times 10^{-3}</td>
<td>0.03 \times 10^{-3}</td>
</tr>
<tr>
<td>Gluonic penguin</td>
<td>(2\beta_s^{\text{eff}}(B_s^0 \rightarrow \phi \phi))</td>
<td>–</td>
<td>0.17</td>
<td>0.03</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>(2\beta_s^{\text{eff}}(B_s^0 \rightarrow K^*0 \bar{K}^*0))</td>
<td>–</td>
<td>0.13</td>
<td>0.02</td>
<td>(&lt; 0.02)</td>
</tr>
<tr>
<td></td>
<td>(2\beta_s^{\text{eff}}(B_s^0 \rightarrow \phi K_s^0))</td>
<td>0.17 [18]</td>
<td>0.30</td>
<td>0.05</td>
<td>0.02</td>
</tr>
<tr>
<td>Right-handed currents</td>
<td>(2\beta_s^{\text{eff}}(B_s^0 \rightarrow \phi \gamma))</td>
<td>–</td>
<td>0.09</td>
<td>0.02</td>
<td>(&lt; 0.01)</td>
</tr>
<tr>
<td></td>
<td>(\tau^{\text{eff}}(B_s^0 \rightarrow \phi \gamma/\tau_{B_s^0}))</td>
<td>–</td>
<td>5%</td>
<td>1%</td>
<td>0.2%</td>
</tr>
<tr>
<td>Electroweak penguin</td>
<td>(S_3(B^0 \rightarrow K^{*0} \mu^+ \mu^-; 1 &lt; q^2 &lt; 6 \text{ GeV}^2/\text{c}^4))</td>
<td>0.08 [14]</td>
<td>0.025</td>
<td>0.008</td>
<td>0.02</td>
</tr>
<tr>
<td></td>
<td>(s_0 A_{FB}(B^0 \rightarrow K^{*0} \mu^+ \mu^-))</td>
<td>25% [14]</td>
<td>6%</td>
<td>2%</td>
<td>7%</td>
</tr>
<tr>
<td></td>
<td>(A_1(K \mu^+ \mu^-; 1 &lt; q^2 &lt; 6 \text{ GeV}^2/\text{c}^4))</td>
<td>0.25 [15]</td>
<td>0.08</td>
<td>0.025</td>
<td>(\sim 0.02)</td>
</tr>
<tr>
<td></td>
<td>(B(B^+ \rightarrow \pi^+ \mu^+ \mu^-)/B(B^+ \rightarrow K^+ \mu^+ \mu^-))</td>
<td>25% [16]</td>
<td>8%</td>
<td>2.5%</td>
<td>(\sim 10%)</td>
</tr>
<tr>
<td>Higgs penguin</td>
<td>(B(B_s^0 \rightarrow \mu^+ \mu^-))</td>
<td>(1.5 \times 10^{-9}) [2]</td>
<td>(0.5 \times 10^{-9})</td>
<td>(0.15 \times 10^{-9})</td>
<td>(0.3 \times 10^{-9})</td>
</tr>
<tr>
<td></td>
<td>(B(B^0 \rightarrow \mu^+ \mu^-)/B(B_s^0 \rightarrow \mu^+ \mu^-))</td>
<td>(\sim 100%)</td>
<td>(\sim 35%)</td>
<td>(\sim 5%)</td>
<td></td>
</tr>
<tr>
<td>Unitarity triangle</td>
<td>(\gamma (B \rightarrow D^{(<em>)} K^{(</em>)}))</td>
<td>(\sim 10-12^\circ) [19, 20]</td>
<td>4(^\circ)</td>
<td>0.9(^\circ)</td>
<td>negligible</td>
</tr>
<tr>
<td></td>
<td>(\gamma (B_s^0 \rightarrow D_s K))</td>
<td>(11^\circ)</td>
<td>(2.0^\circ)</td>
<td>negligible</td>
<td></td>
</tr>
<tr>
<td></td>
<td>(\beta (B^0 \rightarrow J/\psi K_s^0))</td>
<td>0.8(^\circ) [18]</td>
<td>0.6(^\circ)</td>
<td>0.2(^\circ)</td>
<td>negligible</td>
</tr>
<tr>
<td>Charm</td>
<td>(A_{\Gamma})</td>
<td>(2.3 \times 10^{-3}) [18]</td>
<td>(0.40 \times 10^{-3})</td>
<td>(0.07 \times 10^{-3})</td>
<td>–</td>
</tr>
<tr>
<td>CP violation</td>
<td>(\Delta A_{CP})</td>
<td>(2.1 \times 10^{-3}) [5]</td>
<td>(0.65 \times 10^{-3})</td>
<td>(0.12 \times 10^{-3})</td>
<td>–</td>
</tr>
</tbody>
</table>
First-level hardware trigger is limited at higher luminosities for hadronic channels:

- almost a factor 2 between di-muon events and fully hadronic decays
- due to trigger criteria based on $p_T$ and $E_T$ to reduce trigger rate to the bandwidth limited to 1.1 MHz

At higher luminosities → harsher cuts on $p_T$ and $E_T$

- waste luminosity while not retaining amount of data
- increases complexity of track reconstruction
  - higher computational times in processing farm
- ageing and fast degradation of sub-detectors
  - designed to operate 5 yr at $2 \times 10^{32} \text{cm}^{-2}\text{s}^{-1}$
Physics motivations  
(to remove the limitations)

Beyond Flavour Physics: exploration studies \(\rightarrow\) precision studies

- \(BR(B_s \rightarrow \mu^+\mu^-)\) down to \(\sim 10\%\) of SM
- CKM \(\gamma\) angle to \(<1^\circ\)
- \(2\beta_s\) to precision \(<20\%\) of SM value
- charm CPV search below \(10^{-4}\)

but also
- search for lepton-flavour violating tau decays
- low mass Majorana neutrinos
- electroweak physics
- long-lived new particles
- QCD
- …

For an exhaustive list see *LHCb Upgrade Framework TDR, CERN/LHCC-2012-007*
Is it feasible?

YES! We already tried in 2012: took some data at $10^{33}$ (5x designed values)

<table>
<thead>
<tr>
<th>Date</th>
<th>Fill</th>
<th>Energy</th>
<th>ATLAS Physics</th>
<th>ALICE Physics</th>
<th>CMS Physics</th>
<th>LHCb Upgrade</th>
</tr>
</thead>
<tbody>
<tr>
<td>04-Dec-2012</td>
<td>3374</td>
<td>4000 GeV</td>
<td>5460.0</td>
<td>6.595</td>
<td>5604.2</td>
<td>999.1</td>
</tr>
<tr>
<td>B S/N almost independent of pileup</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
| D S/N shows some degradation vs pileup.
Upgrade strategy

Straightforward idea: remove the first-level hardware trigger
Must optimize:

- **Cost vs performance**
  - Minimum requirement to maintain current performance in harsher conditions
  - Re-use existing infrastructure/electronics where needed/possible

- **Manpower**

- **Time**
  - Develop common solution where possible
    - especially in readout architecture
    - e.g. common specs, common readout board…
Current LHCb Vertex Detector

Current Vertex Detector (VELO) is at the heart of LHCb tracking, triggering and vertexing

- Excellent performance, reliable, cluster efficiency >99.5%, best hit resolution down to <4μm
- Movable device! ~50mm to ~5mm close to LHC beams when in collisions (autonomously…)

Si-strips measuring r and φ
New LHCb Vertex Detector

Future VELO must maintain same performance, but in harsher conditions

- Low material budget, cope with > radiation damage, deal with > multiplicities
- Trigger-less readout ASICs and provide fast and efficient reconstruction at HW level

→ Recent technology reviews favored the choice of a

**Si-pixel detector with microchannel cooling**
New LHCb Vertex Detector

• Pixel Silicon detector modules cooled down with fluid (bi-phase CO₂) which passes under the chips in etched microchannels (ΔT = 4-7 °C between fluid and sensor)

• Getting closer to beam (agreed with LHC!) to improve IP resolution!
VeloPix

- Uses ToT for pulse height from TimePix
  - 130 nm CMOS, rad-hard, low-power
- High occupancy in sensors closer to beam
  - factor 10 between innermost and outermost
- Very high data throughput
  - Single chip output ~13 Gb/s
  - Total VELO ~2.5 Tb/s!
- Busy events takes longer to compress
  - Up to 12 μs latency
  - Asynchronous data driven readout! (i.e. events are out-of-order)
Matrix = 64 x 64 super-pixels

Digital Super Pixel core
160um x 220um

Data packet
- BCID 12b
- SP address 12b
- N. of hits 4b
- Payload 8b – 128b

# tracks per 25ns

Hottest chip: 12.2 Gbit/s of data
Current LHCb Tracking system

Present Tracking System will be upgraded:

- VELO + TT (Si-strip) + DIPOLE (no change) + IT (2% inner area, Si) / OT (Straw Tubes)

Current pattern-recognition based on current tracking system would not be efficient in upgraded scenario

- Too high occupancy in central region
- R&D for different solutions
  → for downstream and upstream tracking

Sidenote: R&D in increasing Dipole field (x1.8 Bdl)

Courtesy JC. Wang
New Upstream Tracking Stations

R&D upstream:

- Replace current TT with UT (*Upstream Tracker*), also based on Si-strips
  - reduced thickness
  - finer granularity
  - improved coverage (innermost cut-out at 34 mm)
  - much less material budget (<5% $X_0$)
New UT + New VELO

- Better $p_T$ resolution
- Drastic reduction in ghost rate
- Large gain in reconstruction time!

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Si-strip FE ASIC

ASIC in 130nm CMOS
rad-hard
low power

SAR ADC

Processing & compression

Output links

X 128

shaper 5pF – 45pF

Small spillover 25ns after peak

32cm

6

X 128

6

SAR ADC

Processing & compression

Output links

shaper 5pF – 45pF
SAR ADC

Under test, expected power < 0.5 mW
New Downstream Tracking Stations

R&D downstream:

- Various options still on the table
  - all aimed at reducing the occupancy in the inner region

  - Enlarged, thinner and lighter IT
    → Based on Si-strip
  - New OT straw tubes in central region

  Replace central region with Central Tracker (Sci-Fi detector)
  → Based on Scintillating fibers and SiliconPM

Baseline option!
New LHCb Sci-Fi detector

Build a completely new detector based on Scintillating Thin Fibers

- Blue-emitting multi clad fibers, laid down as a mat
- 2.5m long, 250 um diameter (2.8 ns decay time)
- 12 layers of modules in different layout (x-u-v-x)
- read out with SiPM (at -50C): new trigger-less FE
Sci-Fi SiPMs

Signal shape!
Gain variations?
Clustering to reduce noise
Outer Tracker new electronics

Re-use existing front-end

TDC (ASIC) mapped to
• flash FPGA
• SRAM FPGA
OT TDC in FPGA?

32 bins, 0.78 ns

OK in radiation…….?
Present Ring-Imaging Cherenkov (RICH) detector will be upgraded:

- Current RICH1 (aerogel $C_4F_{10}$) + RICH2 (CF$_4$

**Main changes:**

Remove aerogel radiator

- to compensate for increased occupancy

Remove Hybrid-PhotoDetectors (HPD) with Multi-AnodePMTs

- Hamamatsu R11265 with 80% active area

Front-End electronics will be redeveloped

**R&D:**

Add new detector TORCH

- 1-10 GeV/c
RICH MAPMTs

Non-uniform occupancy scalable links

Adjustable gains in FE MAROC3 or CLARO
Present Calorimeters detectors will be kept:

- ECAL (Shashlik 25 $X_0$ Pb + scintillator)
- HCAL (TileCal Fe + scintillator)

→ PreShower / ScintillatingPadDetector (PS/SPD) will be removed

Main changes:

- PMT gain will be reduced by a factor 5
  - to reduce ageing due to higher luminosities
- Front-End electronics will be redeveloped
  - to be compatible with the reduced gain (R&D)
  - to be compatible with trigger-less readout
Current LHCb:
Remove deadtime by clipping signals

Upgrade:
Reduce gain of PMT (to increase lifetime)
⇒ remove clipping: it decreases signal
⇒ reduce noise by removing $R_{term}$

Active termination in ICECAL ASIC

Switched integrators: no deadtime used successfully in LHCb PS/SPD calo
Calorimeters electronics

ICECAL ASIC in 0.35mm

Digital in flash-FPGA
Upgraded Muon Detectors

Present Muon detector will be kept:

- 4 layers (M2-M5) of Multi-Wire Proportional Chambers (MWPC)

→ first layer of Muon Detector (M1 – used in first-level trigger, with GEMs) will be removed

Main changes:

Front-End electronics will be redeveloped

- to be compatible with trigger-less readout

R&D:

Replace inner part of M2 (closest to IP) with GEMs detectors

- to have higher-granularity
Muon electronics

No M1
M2 to M5 \(\to\) up to 140 ODE
Hit/ L0 link: NZS1 bit/ ch @ 40 MHz
TDC link: ZS 4 bits/ ch @ 40 MHz

L0 (\(\mu\)) Trigger on 4 TELL40s (4 AMC)

Hit/L0mu: 280 GBT links
NZS @ 40 MHz
TDC: 280 GBT links
ZS @ 40 MHz

4 TELL40s (4 AMC)
Trigger-less FE zero-suppression

Channels 0.............3
A-D conversion (6 bits)

Threshold

<table>
<thead>
<tr>
<th>Add 7b</th>
<th>Data 6b</th>
</tr>
</thead>
<tbody>
<tr>
<td>54</td>
<td>A</td>
</tr>
<tr>
<td>55</td>
<td>B</td>
</tr>
<tr>
<td>56</td>
<td>C</td>
</tr>
<tr>
<td>57</td>
<td>D</td>
</tr>
</tbody>
</table>

128 x 6 = 768 bits
(7+6) x 4 = 52 bits
(7+ n) bits

Break-even point
60 hits = 780 bits

TWEPP2013, 23-27 September 2013, Perugia, Italy
Federico Alessio 65
The S-TFC system at a glance

**S-ODIN** responsible for controlling upgraded readout system
- Distributing timing and synchronous commands
- Manages the dispatching of events to the EFF
- Rate regulates the system
- Support old TTC system: *hybrid system!*

**SOL40** responsible for interfacing FE+TELL40 slice to S-ODIN
- Fan-out TFC information to TELL40
- Fan-in THROTTLE information from TELL40
- Distributes TFC information to FE
- Distributes ECS configuration data to FE
- Receives ECS monitoring data from FE
S-TFC concept reminder

- LHC Interface
- LLT
- S-ODIN
- Master FPGA (STRATIX IV/V GX)
- Clock Fanout
- S-ODIN Logic
- Programmable Switch layer (Partitioning)
- Switch Logic
- Built-in GX Transceivers layer
- #links = #LHCb sub-systems
- ECS
- FARM
- TFC, Throttle
- ECS to FE
- TFC+ECS Interface
- Master FPGA (STRATIX IV/V GX)
- FAN-OUT/FAN-IN Logic
- ECS to FE encoding Logic
- optional S-ODIN Logic
- FE electronics
- TELL40s
- LLT
- FE electronics
- TELL40s
How to decode TFC in FE chips?

Use of \textit{TFC+ECS GBTs} in FE is 100\% common to everybody!!

\begin{itemize}
  \item dashed lines indicate the detector specific interface parts
  \item please pay particular care in the clock transmission: the TFC clock must be used by FE to transmit data, i.e. low jitter!
    \begin{itemize}
      \item Kapton cable, crate, copper between FE ASICs and GBTX
    \end{itemize}
\end{itemize}
The TFC+ECS GBT protocol to FE

- **GBT word**: 120 bits

<table>
<thead>
<tr>
<th>HEADER</th>
<th>IC</th>
<th>EC</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>FEC</th>
</tr>
</thead>
</table>

4 bits (Idle: 0110, Data: 0101) --> 2x2 bits

1 e-link @ 80 Mb/s for GBT internal use only

- **1 e-link @ 80 Mb/s to GBT-SCA**

16 e-links @ 80 Mb/s to 16 GBT-SCAs for ECS

- **24 e-links @ 80 Mb/s for TFC**

- **2x16 bits**

- **SCAs**

- **SCA**

→ **TFC protocol has direct implications in the way in which GBT should be used everywhere**
  - 24 e-links @ 80 Mb/s dedicated to TFC word:
    - Use 80 MHz phase shifter clock to sample TFC parallel word
  - TFC bits are packed in GBT frame so that they all come out on the same clock edge
    - We can repeat the TFC bits also on consecutive 80 MHz clock edge if needed

→ **Leftover 17 e-links dedicated to GBT-SCAs for ECS configuring and monitoring (see later)**
Now, what about the ECS part?

Each pair of bit from ECS field inside GBT can go to a GBT-SCA
- One GBT-SCA is needed to configure the *Data GBTs* (EC one for example?)
- The rest can go to either FE ASICs or DCS objects (temperature, pressure) via other GBT-SCAs
  - GBT-SCA chip has already everything for us: interfaces, e-links ports ..
    → No reason to go for something different!
  - However, «silicon for SCA will come later than silicon for GBTX»…
    → We need something while we wait for it!

---

**GBT word: 120 bits**

<table>
<thead>
<tr>
<th>HEADER</th>
<th>IC</th>
<th>EC</th>
<th>D4</th>
<th>D3</th>
<th>D2</th>
<th>D1</th>
<th>D0</th>
<th>FEC</th>
</tr>
</thead>
<tbody>
<tr>
<td>4 bits</td>
<td>2x2 bits</td>
<td>16 bits</td>
<td>16 bits</td>
<td>16 bits</td>
<td>16 bits</td>
<td>16 bits</td>
<td>2x16 bits</td>
<td></td>
</tr>
</tbody>
</table>

- 1 e-link @ 80 Mb/s for GBT internal use only
- 16 e-link @ 80 Mb/s to GBT-SCA
- 16 GBT-SCAs for ECS

---

**SCAs**

- 24 e-links @ 80 Mb/s for TFC
- 16 e-link @ 80 Mb/s to SCA

---

**SCAs**

- 1 e-link @ 80 Mb/s to GBT-SCA

---

**HEADER**

- Idle: 0110
- Data: 0101

---

**GBT word**

- 24 e-links @ 80 Mb/s for TFC
- 16 GBT-SCAs for ECS
SOL40 encoding block to FE!

Memory Map with internal addressing scheme for GBT-SCA chips + FE chips addressing, e-link addressing and bus type: content of memory loaded from ECS

Protocol drivers build GBT-SCA packets with addressing scheme and bus type for associated GBT-SCA user busses to selected FE chip

→ Basically each block will build one of the GBT-SCA supported protocols
DAQ IP core

Ethernet 10G (xN) Setup
Long distance transmission

Short fiber

400m OM4 fiber
Future LHC DAQs in numbers

<table>
<thead>
<tr>
<th></th>
<th>Event-size [kB]</th>
<th>Rate [kHz]</th>
<th>Bandwidth [Gb/s]</th>
<th>Year [CE]</th>
</tr>
</thead>
<tbody>
<tr>
<td>ALICE</td>
<td>20000</td>
<td>50</td>
<td>8000</td>
<td>2019</td>
</tr>
<tr>
<td>ATLAS</td>
<td>4000</td>
<td>200</td>
<td>6400</td>
<td>2022</td>
</tr>
<tr>
<td>CMS</td>
<td>2000</td>
<td>200</td>
<td>3200</td>
<td>2022</td>
</tr>
<tr>
<td>LHCb</td>
<td>100</td>
<td>40000</td>
<td>32000</td>
<td>2019</td>
</tr>
</tbody>
</table>

- Some overlapping trends across experiments, at least conceptually
  - custom-made Readout Boards with fast optical links and big&powerful FPGAs
    - ideally with fast interface to PCs (PCIe Gen3 or future…)
    - ideally with some co-processing (Xeon, GPUs…)
  - commercial network technologies following market trends in terms of BW & costs
    - distributed vs data-center-like network.
    - network technologies: Ethernet vs InfiniBand.

*Courtesy N. Neufeld*
Try to keep the good things about our current DAQ:

✓ Simple single-stage dataflow
✓ Smallest possible number of hardware components
✓ Scalability

Try to put in the good things we know of:

✓ Minimize number of expensive “core” network ports
✓ Use the most efficient technology for a given connection
  • Try to be open for interconnect technology and keep distances short
✓ Exploit the economy of scale → try to do what everybody does (but smarter 😊)
Evolution of Network Interface Cards

- PCIe Gen3 available
- Chelsio T5 (40 GbE and Intel 40 GbE expected)
- EDR (100 Gb/s) HCA expected
- 100 GbE NIC expected
- PCIe Gen4 expected

- Ethernet
- InfiniBand x4
- PCIe x8

- Courtesy N. Neufeld
• Minimal variant – no external memories / no transmitters for GBT

• Power from 75W up to 450W (if needed! using GPU standard)

• PEX8733 can be replaced by PCIe x 16 softcore
Alternative option: DAQ with PCIe40

Again, same generic hardware with different firmware (PCle40)

Very compact event-building network: host PC acts as event-builder node
- basically, “infinite” buffer-space
- streamlined readout