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Trigger-less readout architecture for the upgrade of the LHCb experiment at CERN

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The LHCb experiment has proposed an upgrade of its detector in order to collect data at ten times its initial design luminosity. The current readout architecture will be upgraded by removing the existing first-level hardware trigger whose efficiency is limited for hadronic channels at high luminosity. The new readout system will record every LHC bunch crossing and send data to a trigger selection process performed entirely by software running in a computing farm. Therefore, the new readout system must cope with higher sub-detector occupancies, higher rate and higher network load. In this paper, we describe the architecture, functionalities and technological challenges of such an upgraded system.

Summary

The LHCb experiment is planning a major upgrade during the LHC Long Shutdown 2 in order to increase the amount of recorded data by a magnitude factor of 10. Some sub-detector technologies will perform adequately in the upgrade environment, whilst others will be replaced. However, the upgrade requires the complete replacement of all Front-End electronics and data acquisition (DAQ).

A fully trigger-less 40 MHz readout architecture has been envisaged as the baseline for the upgrade of the LHCb readout architecture. The architecture aims at removing entirely the first-level hardware trigger in order to record every bunch crossing in the LHC and make every event available to the high-level software trigger. Such choice presents major challenges and technological solutions which are outlined in this paper.

In particular, we will focus our attention on the implementation of trigger-less Front-End electronics. The sub-detector electronics will run without the aid of a first-level trigger, recording and transmitting every LHC bunch crossing. Moreover, the Front-End electronics will profit from the development of a generic radiation-tolerant data link. We will present plans for the implementation of the Front-End electronics with this link and the implications of this choice on the entire readout architecture. Investigations are ongoing to evaluate the use of Field Programmable Gate Arrays (FPGAs) in FE environments, and these will be summarized.

New technologies for the readout and DAQ system are also envisaged. A common electronics board will be used as the backbone of the readout architecture. This board is based on Advanced Telecommunications Computing Architecture (ATCA) technologies, dense optical links and powerful FPGAs which allow for a highly integrated and cost-effective system. This board will take the role of a module to read data from sub-detector, but, thanks to its flexibility, will also take the role of specific control boards to supervise the entire readout system.

A new fast readout control system is being developed to transmit fast commands, timing information and clock to the entire readout electronics. This system will act as the supervisor of the entire readout system by distributing fast commands via optical links. Furthermore, this system will be interfaced to the global LHCb Experimental Control System and transmit configuration data to the Front-End electronics. The data bandwidth provided by the generic link allows the sharing of hardware resources for both fast and slow commands. The implementations and implications of such a solution are described in this paper.

Finally, new solutions and technologies for event building networks will also be presented as the new LHCb DAQ network will need to cope with a multi-Tb/s dataflow.

To conclude, we will outline plans for the development of the system over the next years and the technological challenges which will need to be faced during this period.

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