Hardware and Firmware developments for the upgrade of the ATLAS Level-1 Central Trigger Processor

TWEPP 2013, Perugia, 25. September

System overview:
- Trigger/DAQ System Architecture
- Level-1 Trigger: current system
- CTP Architecture
- CTP: Upgrade motivations

Central Trigger Processor Core+ (CTPCORE+)
- Demonstrator
  - Hardware Tests – Proof of Concept
  - Firmware Design
- CTPCORE+ Hardware
  - Board Design
  - Status

Summary and Outlook
Trigger/DAQ System Architecture

Level-1 Trigger (LVL1):
- Custom electronics, FPGAs

Level-2 Trigger (LVL2), Event Filter (EF):
- COTS computers, networks & custom software

Front-end Electronics:
- Custom, rad-hard ASICs

Pipeline Memories

Level-1 Accept (L1A)

Derandomizers

Readout Drivers (RODS)

Readout Buffers (ROBS)

Event Builder

Full-event buffers and Processor sub-farms

Data Recording

20 MHz

75 kHz

~5 kHz

~600 Hz

Event Filter

Level-2 Trigger (2.5 us)
Level-1 Trigger: Post-LS1 System

- Uses reduced granularity information from calorimeter and muon trigger detectors
- Trigger decision based on object multiplicities at different thresholds
- Synchronous, pipelined processing system operating at the bunch crossing (BC) rate of 40 MHz
- Generates Level-1 Accept (L1A) and sends it via Timing, Trigger and Control (TTC) distribution to detector front-ends to initiate readout
- Identifies regions-of-interest (RoI) to seed the Level-2 (LVL2) Trigger
- Maximum round-trip latency: 2.5 us
  - Data stored in on-detector pipelines
- Maximum trigger rate: 100 kHz
- Custom built electronics (FPGAs)
CTP Architecture

Composed of 9U VME boards:

- **CTPMI - Machine interface**
  - Receive timing signals from LHC

- **CTPIN - Input module**
  - Receive trigger input signals
  - Synchronize and align signals

- **CTPMON - Monitoring module**
  - Bunch-per-bunch monitoring

- **CTPCORE - Core module**
  - Form Level-1 Accept (L1A)
  - Send summary information to LVL2 & DAQ

- **CTPOUT - Output module**
  - Send trigger to detector FE via the TTC system
  - Receive calibration requests

- **CTP Backplane**
  - Common (timing), trigger inputs and calibration requests
CTP: Upgrade motivations

• Primary motivation
  – Increase the number of trigger inputs:
    – PIT: 160 -> 320
    – Topological processor (L1Topo) signals: 0 -> 192
    – Increase the number of trigger items (combinations): 256 -> 512

• Additional features
  – Partitioning of L1A generation for detector commissioning
    – 1 primary partition + 2 secondary for concurrent running
  – Option to connect trigger inputs through optical links (2018)

• Requires complete redesign of CTPCORE (=> CTPCORE+), CTPOUT (CTPOUT+) modules and COM backplane
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  - Readout & Monitoring FPGA
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Summary and Outlook
CTPCORE+ - Hardware

- **GPS time (CTRP)**
- **Monitoring PC**
- **DAQ S-LINK**
- **LVL2 S-LINK**
- **Spare SFPs**
- **Optical Outputs (loopback tests)**
- **96 Electrical Inputs (LVDS) from L1Topo**
- **Optical Trigger Inputs for Phase-1**

**Readout/Monitoring FPGA (XC7VX485T)**
- **VME I/F (XC6SLX45)**
- **1GbE PHY**
- **SFP**
- **Mini POD Tx**
- **Mini POD Rx**
- **PIT, ITM, TAP, TAV (16 x 6.4 Gbd)**
- **12 x 6.4 Gbd**
- **3 x 32 bit @ 40/80 MHz**
- **12 x 6.4 Gbd**
- **BC, ORB, ECR, 3 x BSY L1Ap**
- **2 x L1As**
- **RAM1**
- **RAM2**
- **RAM**
- **VMEbus**
- **Trigger & Timing Signals (COM Backplane)**
- **PIT Bus Backplane 160 bit @ 80 MHz (DDR)**

Marco Ghibaudi, 25. September 2013
New CTPCORE+ module has been designed, in production
Trigger Path FPGA

- Virtex-7 FPGAs (XC7VX485T, BGA1157)
  - 300k LUTs (6-input), 600k flip-flops, 1030 RAM blocks (36 kbit)
  - 600 I/O pins, 20 multi-gigabit transceivers (MGTs)
- Trigger path implemented in one FPGA to minimize latency
- Trigger input signals
  - 160 PIT bus lines at 80 MHz (320 triggers at 40MHz)
  - 96 LVDS inputs for low-latency connection to L1Topo from the front panel (DDR)
  - Option to connect trigger inputs through 12 serial optical links
- Functions:
  - Generates L1A signal and associated trigger type for three trigger partitions
  - Receives busy signals for each partition from COM+ backplane to veto triggers
  - Sends full information about trigger decision to readout & monitoring FPGA (>2300 bit/BC > 90 Gbit/s)
  - Playback and diagnostics memory (DDR3 SODIMM memory)
Readout & Monitoring FPGA

- Same type as trigger path FPGA (XC7VX485T)
- Implements non-latency critical functionality
- Receives detailed information from trigger path FPGA via 16 serial links running at 6.4 Gbps
- Readout functionality
  - Send trigger summary information for the primary partition to LVL2 and DAQ via S-LINK for every L1A
  - Add precise timestamp to each event (GPS reference)
- Monitoring functionality
  - 2048 integrating counters for trigger rate monitoring
  - 256 per-bunch monitoring counters
    - Histogram of selected trigger bit versus BCID
    - Requires ~50% of the on-chip block RAM resources
    - Event monitoring
  - Optional GbE communication path to overcome VME bandwidth limitation
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**Demonstrator**
- Hardware Tests – Proof of Concept
  - Chip-to-chip communication test
  - Power Consumption
  - Firmware Design

Summary and Conclusion
Demonstrator

- Based on 2 commercial Xilinx evaluation boards (VC707)
  - Same Virtex7 FPGAs (XC7VX485T) as used on CTPCORE+ board, different package
  - 2 FMC connectors exporting 16 MGTs
  - Ethernet Interface
  - 1GB DDR3 Ram Memory

- Used for:
  - Hardware proof-of-concept
  - Firmware prototyping without waiting for CTPCORE+ board

- Examples of tests conducted
  - Chip to chip connectivity test
  - Power consumption measurements
  - Validation of F/W modules
Chip-to-Chip communication

- On CTPCORE+ board, FPGA Trigger and FPGA Readout are connected through 16 MGTs (diff. pairs, fast links). Chip-to-chip connections on PCB traces, target speed 6.4Gbps.

  - To estimate the BER, we set up a test environment
  - The same type of test can be done on CTPCORE+ board

Results of long-run test:
~ 6 hours -> 0 Errors.
Power consumption

- Both VC707 and CTPCORE+ boards use DC/DC controllers with PMBus interface
- PMBus is an open-standard power-management protocol, similar to I2C. It can be used for:
  - Configuring and monitoring power supply unit parameters (voltage and current in/out levels).
- For crosschecking vendors power consumption estimation tools results. In our case for checking the values generated by Xilinx Power Estimation (XPE) tool.

Advanced configuration capabilities: E.g. Rail 1 has a 1.75 V output and it’s powered off 10 ms before Rail 4.

Result: XPE predictions are coherent with measurements
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- **Firmware Design**
  - New components

Summary and Outlook
DDDR3 Memory

- DDR3 Memory Controller for monitoring trigger information and running playback tests
  - Modified Xilinx IPCore for DDR3 memory controller (clocking scheme etc.)

- Tested at 1.6Gbps (bandwidth ~100 Gbps)

- Use of memory:
  - Snapshot memory
  - Playback memory

- Scheduling of the memory accesses for handling different types of requests
  - Store trigger information in the memory (snapshot memory)
  - Load and store test patterns (playback memory)
  - Programming and retrieval of memory content through VME/Ipbus
Control and Monitoring Interface

- Ethernet based control protocol
  - Control and monitoring achieved through Ipbus
  - IPbus provides a mechanism to access FPGA registers through Ethernet/UDP. Used by CMS
  - Used in the Demonstrator to emulate VME (no VME bus on VC707). It will be replaced by VME on CTPCORE+
  - Adaptation of IPbus 1.4 firmware to work with Virtex7 FPGA architecture
  - Supports standard operations (Read, Read Burst, Write, Write Burst)
  - Developed model (MAC-layer emulated, full IPbus stack) to speed up simulation
Chip to Chip communication protocol – 1/2

• Extended the Xilinx Aurora 64b66b proprietary protocol for implementing multiple channels (each channel 4 MGTs)

• Configurable baud-rate (6.4 Gbps, 8Gbps, 10Gbps)
Chip to Chip communication protocol – 2/2

- Designed glue logic for overcoming internal clocking limitations of Xilinx MGTs;
  - Scalable multiple channels architecture
  - Same design can be used on CTPCORE+
  - Based on packet dispatching and sequence restoring for in-order reception

<table>
<thead>
<tr>
<th>System</th>
<th>Num. MGTs</th>
<th>MGT Baudrate</th>
<th>Throughput (64b66b coding)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Demonstrator</td>
<td>3*4</td>
<td>10 Gbps</td>
<td>116 Gbps</td>
</tr>
<tr>
<td>CTPCORE+</td>
<td>4*4</td>
<td>6.4 Gbps</td>
<td>99.3 Gbps</td>
</tr>
</tbody>
</table>

Diagram: BC Data Generator or Triggering Logic → Packet Dispatcher (RR) → FIFO Tx Ch.0, FIFO Tx Ch.1, FIFO Tx Ch.2, FIFO Tx Ch.3 → Packet Sequence Recomposer → FIFO Rx Ch.0, FIFO Rx Ch.1, FIFO Rx Ch.2, FIFO Rx Ch.3
Firmware validation

- Integration of the newly developed firmware modules in a system that mimics CTPCORE+ configuration
- IPbus is used for controlling the configuration and monitoring demonstrator system
- Concurrent memory accesses supported during playback test
- Domain crossing needs to be carefully handled
  - IPBus (32.5 Mhz), Ethernet (125Mhz), Core Logic (40MHz), MGTs (160 MHz)

Datapaths

- Config. via IPbus
- Internal data storage
- Playback mode
- RAM access IPbus
- RAM access MGT
- MGT to MGT

![Datapath Diagram](image)
Summary and outlook

• Summary
  - CTPCORE+ board designed. First prototypes in production, PCB delayed
  - Firmware for DDR3 Memory, Ethernet + IPbus and MGTs new hardware components:
    - Designed and tested on the demonstrator
    - Easy to integrate on CTPCORE+

• Outlook
  - CTPCORE+ board testing, system integration
  - Port existing firmware on the new architecture, integrating it with new components
  - Extend software to support new features of CTPCORE+
  - Commissioning in ATLAS in 2014
Questions?