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Hardware, firmware and software developments for the upgrade of the ATLAS Level-1 Central Trigger Processor

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The Central Trigger Processor (CTP) is the final stage of the ATLAS first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 100 kHz. An upgrade of the CTP is currently underway to significantly increase the number of trigger inputs and trigger combinations, allowing additional flexibility for the trigger menu.

We present the hardware and FPGA firmware of the newly designed core module (CTPCORE+) module of the CTP, as well as results from a system used for early firmware and software prototyping based on commercial FPGA evaluation boards. First test result from the CTPCORE+ module will also be shown.

Summary

The Central Trigger Processor (CTP) is the final stage of the ATLAS first level trigger system which reduces the collision rate of 40 MHz to a Level-1 event rate of 100 kHz. The CTP makes the trigger decision based on a list of programmable selection criteria using trigger inputs from the calorimeter and muon trigger subsystems as well as from other sources.

The CTP is entirely based on custom-built electronics modules housed in a single 9U VME64x chassis. The functionality of the CTP is largely implemented in FPGAs. However, due to the increasing luminosity of the LHC expected after the first long shutdown and the growing demands placed on the ATLAS Level-1 trigger system, the current CTP has reached its design limits.

Therefore an upgrade of the CTP is currently underway to significantly increase the number of trigger inputs to the CTP from 160 to 512, by operating the internal backplane at twice its design speed. In addition, the newly designed core module (CTPCORE+) of the CTP provides direct inputs for the potentially latency-critical signals from the Level-1 Topological Trigger Processor (L1Topo), which will also be deployed during the shutdown. With the CTPCORE+ module the number of trigger combinations that can be individually masked and pre-scaled will also increase from 256 to 512, allowing additional flexibility for the trigger menu. The timing backplane of the CTP and the output modules (CTPOUT+) will also be replaced in order to provide support for additional independent trigger partitions for calibration runs and detector commissioning. Finally, the upgraded CTPCORE+ will provide support for receiving trigger input signals over high-speed optical links for future trigger system upgrades (latency permitting).

We present the hardware and FPGA firmware of the newly designed CTPCORE+ module, as well as results from a system used for early firmware and software prototyping based on commercial FPGA evaluation boards. First test result from the final CTPCORE+ module will also be shown. The upgraded CTP will be deployed in the ATLAS experiment during 2014.

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