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The Charge Pump PLL Clock Generator Designed for the 1.56 ns Bin Size Time-to-Digital Converter Pixel Array of Timepix3 Readout Chip

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Timepix3 is a newly developed pixel readout chip which is expected to be operated in a wide range of gaseous and silicon detectors. It is made of 256 x 256 pixels organized in a square pixel-array with 55um pitch. Oscillators running at 640MHz are distributed across the pixel-array and allow for a highly accurate measurement of the arrival time of a hit. This paper concentrates on a low-jitter PLL that is located in the chip periphery. This PLL provides a control voltage which regulates the actual frequency of the individual oscillators, allowing for compensation of process, voltage and temperature variations.

Summary

The Timepix3 predecessor, labeled Timepix, originated from the successful Medipix2 ASIC developed at CERN. It was operated as active anode in various gaseous detectors with gas electron multipliers (GEMs) and MICROMMEGAS for gas amplification. Such charge collection on the bare pixels of a especially developed ASIC is one of the readout concepts pursued for a TPC operated at a future linear collider. However, this application demands for several improvements now implemented in the recent Timepix3 ASIC.

The Timepix3 readout chip was designed by a collaboration of CERN, NIKHEF and the University of Bonn. It features an active surface of 1.4 x 1.4 cm2. Each pixel contains an analog front end: a charge sensitive amplifier, a discriminator and a 4-bit digital-to-analog converter for threshold adjustment. Signals of positive and negative polarity can be processed. The digital part of the pixel includes a 10-bit time-over-threshold counter, a 14-bit coarse time-stamping register and a 4-bit fine time-stamping counter. Each pixel can be programmed to work on one of three different modes: Event counting & Integral ToT, Only ToA and ToA & ToT.

In order to avoid distributing a very high-speed clock signal into the pixel-array and to save the pixel area, eight pixels (called super pixel) share a high-speed voltage control oscillator (VCO) that is based on a small area RC ring-oscillator. A PLL circuit with an embedded replica of the ring-oscillator is located in the periphery of the chip. By distributing the control voltage rather than the clock signal to the pixel-array, all pixel-level ring-oscillators are forced to oscillate at 640MHz. This approach allows to stabilize the oscillation frequency by an external PLL, and hence to reduce the effect of fluctuations with respect to process parameter variations and temperature changes.

The developed PLL consists of a phase frequency detector (PFD), a charge pump, a third-order passive loop filter, a VCO and a digital divider. The PFD detects the phase and frequency differences between the reference and the feedback clock signal. These differences are converted into a control voltage by the charge pump and the loop filter. Once frequency and phase of the input reference are the same as those of the feedback clock signal, the voltage from the loop filter is used to control the pixel-level ring-oscillators for yielding a constant frequency of 640 MHz.

In August of 2011, a prototype called GOSSIPO4.1 has been designed and fabricated for verification of the basic Timepix3. It includes eight-pixel structures (i.e. super pixel) sharing one fast oscillator with a PLL control. The functionality of the PLL has been verified on this chip. The PLL generates a clock frequency of 640 MHz with a power consumption of 5 mW, at a supply voltage of 1.5 V. Measurements have shown the TIE jitter performance to be below 24 ps RMS at an additional 320 MHz output. The same PLL structure has

been implemented in Timepix3, which was submit in May of 2013. The results of the Timepix3 PLL will be reported in this workshop.

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