The Read-Out Driver (ROD) card for the ATLAS experiment: commissioning for the IBL detector and upgrade studies for the Pixel Layers 1 and 2

R.Travaglini

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Session B2 : Systems, Planning, installation, commissioning and running experience
Atlas Pixel Detector Overview

**innermost detector:** tracking and vertexing

**3 barrel layers** - b-layer closer the beam pipe (\( <r> = 5\text{cm} \))

80 millions pixel in total (50 \(\mu\text{m} \times 400\ \mu\text{m} \))

**front-end chip:** FE-I3 (2880 channels x chip)

basic unit: module (sensitive region coupled with 16 FE-I3)

1774 modules in total

one Module Control Chip (MCC) x module

different readout schemes:

b-layer: 2 link @ 80 Mb/s (160 Mb/s)

layer 1: 1 link @ 80 Mb/s

layer 2: 1 link @ 40 Mb/s

Each **off-detector readout unit** handles up to 160 MB/s

(2 link @ full speed) (1 S-Link)
Pixel Detector Upgrade: Inner Barrel Layer (IBL)

Major Goals:

- strengthen the **tracking capability** by increasing both redundancy and precision;
- **preserve the performances** of the Pixel Detector for effects due to the increased luminosity expected after LHC upgrades (greater pile-up and radiation doses).

Installation during LHC long shutdown 1 (ends in June 2014)
A new front-end ASIC, called FE-I4 has been designed to face the larger occupancy as well as to manage the increased bandwidth expected for IBL.

New off-detector electronics have been foreseen as well, in order to overcome limitations in the current system: two 9U-VME cards: Back-of-Crate (BOC) and Read-Out Driver (ROD) respectively implementing optical I/O interface and data processing.

Each card pair processes data received from 32 FE-I4 data links for a total I/O bandwidth of 5.12 Gb/s.

BOC-ROD Output through 4 S-Links per pair to drive the data out.

Faster calibration link by using Gb Ethernet instead of the VME bus for data transfer.
The ROD-BOC

14 pairs to be installed in total (+1 for Diamond detector)
the ReadOut Driver (ROD) card

Control:
- commands to FE-I4 (configuration, triggers)
- configure BOC

Data taking:
- gathering of front-end output
- event building

Detector calibration and monitoring:
- Scan performing
- histogramming

rev C - February ’13 - 5 cards - pre-production

rev A - Sept. ’11
- 3 cards
- 1st proto

rev B - February ’12
- 5 cards
- distributed at labs
ROD - Hardware

14 layers PCB - 9U VME

Control, debug and interface with Calibration Farm/PC:
- 3 Gbit Ethernet Connectors:
  - 1 receiving config. from PC
  - 2 sending histos to PC farm
- 1 USB mezzanine
- 1 TTCrq mezzanine

Main Firmware components:
- 1 Spartan6 (Xil.) Prog. Res. Man.
- 1 Virtex5 (Xil.) Master: operation control (PowerPC)
- 2 Spartan6 (Xil.) Slaves: data processing (MicroBlaze)

Other components:
- 4 SSRAM (2 per Sp6)
- 1 Flash (Atmel) for the Vtx5
- 3 DDR2 (1 per each Sp6 + 1 Vtx5)

Interface with BOC (FE-I4&ROS):
- P0/P2/P3 connectors 40-80Mhz
ROD commissioning strategy

Many test stands have been assembled; different functionalities have been verified as well as distinct parts of firmwares are developed based on local setups.

6 labs with different setups:
CERN, Bologna, Wuppertal, Mannheim, Genova, Gottingen
### ROD commissioning

<table>
<thead>
<tr>
<th>Test</th>
<th>Status</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power supply</td>
<td>DONE</td>
<td>25.7 W with current fw</td>
</tr>
<tr>
<td>Temperature</td>
<td>DONE</td>
<td>V5 &lt; 42 C ; SP6 &lt; 50 C</td>
</tr>
<tr>
<td>Clock distribution</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>Interface with TIM</td>
<td>almost done</td>
<td></td>
</tr>
<tr>
<td>Interface with DDR2 and FLASH mem</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>VME</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>On-board and to BOC slow control Bus</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>BOC -&gt; ROD</td>
<td>DONE</td>
<td>96 lines (SSTL3 @ 80 MHz)</td>
</tr>
<tr>
<td>ROD -&gt; BOC</td>
<td>ongoing</td>
<td>tested with full speed but not with S-Link protocol</td>
</tr>
<tr>
<td>Interface with SRAM</td>
<td>almost done</td>
<td>stand alone @ 200 MHz (36 bit)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>full fw @ 140 MHz (32 bit)</td>
</tr>
<tr>
<td>Ethernet</td>
<td>DONE</td>
<td>3 gigabit links</td>
</tr>
<tr>
<td>V5 fw and sw upload from VME</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>SP6 fw upload from VME</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td>SP6 sw upload from ETH</td>
<td>DONE</td>
<td></td>
</tr>
<tr>
<td><strong>Integration with FE-I4</strong></td>
<td>well advanced</td>
<td>see next slides</td>
</tr>
</tbody>
</table>

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The Read-Out Driver (ROD) card for the ATLAS experiment

R.Travaglini
Example test #1: BOC-ROD transmission

Data are sent @ **80 Mb/s on the 96 bit-wide bus (SSTL3 logic)**

Different phases of the sampling clocks

2 hour running per phase

**good uniformity**: same sampling windows for all 5 rev C cards

<table>
<thead>
<tr>
<th>Phase (degrees)</th>
<th>Device</th>
<th>Status</th>
<th>Problems</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>SP6A</td>
<td>FAIL</td>
<td>Multiple errors on every bus</td>
</tr>
<tr>
<td></td>
<td>SP6B</td>
<td>FAIL</td>
<td>Multiple errors on every bus</td>
</tr>
<tr>
<td>90</td>
<td>SP6A</td>
<td>FAIL</td>
<td>One error in 2 hours of test</td>
</tr>
<tr>
<td></td>
<td>SP6B</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td>180</td>
<td>SP6A</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SP6B</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td>270</td>
<td>SP6A</td>
<td>OK</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SP6B</td>
<td>OK</td>
<td></td>
</tr>
</tbody>
</table>
Example tests #2: Integration with FE-I4 (1)

- Firmware layout well advanced
- Most of features to handle 32 FE-I4 are in place
- Tests with 2 chips are usual
- Setup with 8 chip (half a stave) is on going

![Diagram of BOC and ROD systems with connections and component labels]
Example tests #2: Integration with FE-I4 (2)

fw: sp6fmt

fw: rodMaster

Gatherer'

SLAVE B

ROD bus

ETH

V5

PPC

Ramblock

INMEM FIFO

register block

Simple EFB-0

Simple EFB-1

Histo0

Histo1

S-Link0

S-Link1

SSRAM

DDR2

DMA

axi epc

axi epc

axi epc

axi epc

axi histo dma

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Example tests #2: Integration with FE-I4 (3)

CHIP #0
1/4 PixelMask
Cal Pulse Length = 5 BC
First Mask Stage

CHIP #1
1/4 PixelMask
Cal Pulse Length = 6 BC
First Mask Stage
Example #3: Interface with SRAM for Histogramming

★ Custom fw solutions are developed in order to enhance the calibration scan

★ High frequency interface with SRAMs is on study:
  - a 140 MHz clock interface has been successfully integrated in the latest fw release
  - a 200 MHz clock interface has been successfully tested stand-alone

Clock distribution

optimize termination (SSO problem)
ROD ready for production for IBL

We defined a list of minimal procedures to validate the ROD cards after production:

- Firmware-software upload from VME, JTAG and Gb/s-Ethernet ports
- ROD-2-BOC (and BOC-2-ROD) dataflow over all I/O lines
- R/W tests for Virtex5 and Spartan6 external memory modules
- Dataflow tests on the 3 Gb/s ports
- TIM card connectivity test

Test committed-delegated to the ROD manufacturer company (the same we asked for ROD ver B and C cards):

- Electrical test after component supply
- RX test for large BGA-packaged components

15 RevC IBL ROD board production started on August 26th 2013
Boards are expected on the first week of October
Distribution to CERN might start at the end of October
Overview reminder

innermost detector: tracking and vertexing
3 barrel layers - b-layer closer the beam pipe
(\(<r>=5\text{cm}\))
80 millions pixel in total (50 \text{um} \times 400 \text{um})

front-end chip: FE-I3 (2880 channels x chip)
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layer 2: 1 link @ 40 Mb/s

Each off-detector readout unit handles up to 160 MB/s
(2 link @ full speed)
(1 S-Link)
With the **restart of LHC** we expect a **higher luminosity**, which will increase even more in the next years.

**The link occupancy for the Pixel readout link will suffer from bandwidth limitations.**
(reminder: link bandwidth is a function of both occupancy and trigger rate)
Module and link occupancy have been extrapolated using the experience gained from the last year(s).

Suffering for **Layer2** could be observed already in the last run period.
**Possible Action:** Increase link bandwidth to 80 Mb/s

**Layer 1** will experience at $\sim 2 \times 10^{34}$ luminosity
Layer 1 is already read out at 80 Mb/s
**Possible Action:** Double the links per module and upgrade the bandwidth to 2x 80 Mb/s, (requires installing additional fibres now)
Adopting ROD for layer 1 and 2

Therefore, **using the presented IBL ROD and BOC cards is a viable solution** also for the Pixel upgrade to overcome the bandwidth limitations.

Firmware of the ROD needs modification to handle the Pixel module data.

**No Atlas official plan** at the time being but **discussion** well advanced.

We can **propose** to repeat the **same roadmap for Layer 2**
(caveat:
   new boards production should start soon; to be installed mid next year)

Whatever needed for Layer 1 will be probably postponed after IBL and Layer 2 commissioning; only components might be bought earlier

**Further benefits:**

No major further development is needed as the ROD and BOC are there for the IBL anyhow

Firmware adaptation to Pixel needs

**This will uniform our readout system:**

Common spares for the 4-Layers Pixel
Summary and conclusions

- The **ROD card** for the readout of the **Atlas IBL** pixel has been presented.

- **Tests** on the pre-production batch have been discussed and selected results shown.

- The **final production** has been launched (15 cards).

- **Bandwidth limitation** of existing Pixel **layers 1 and 2** have been analyzed.

- The **benefits** of adoption of the **IBL ROD** even for layer 1 and 2 have been pointed out.
Additional Material
IBL ReadOut system summary

<table>
<thead>
<tr>
<th>Number of IBL Staves / ROD-BOC pair</th>
<th>14</th>
</tr>
</thead>
<tbody>
<tr>
<td># DAQ Modules per ROD-BOC pair</td>
<td>16</td>
</tr>
<tr>
<td># FE-I4s chip per ROD-BOC pair</td>
<td>32</td>
</tr>
<tr>
<td>Total # of FE-I4s in IBL</td>
<td>448 (32*14)</td>
</tr>
<tr>
<td>Number of Pixels per FE-I4</td>
<td>26880</td>
</tr>
<tr>
<td>Total # of read-out channels</td>
<td>~12 M</td>
</tr>
</tbody>
</table>
Readout Scheme Overview

VME readout crate
16 card pairs (ROD/BOC)

S-Link

ROS

Optical BPM

Optical 8b/10b

Optical BPM

Optical 8b/10b

Optoboard
(housed in Optobox)

Optoboard
(housed in Optobox)

Detector Module
Detector Module
Detector Module
Detector Module
Detector Module
Detector Module
Detector Module

Halfstave

Halfstave

Counting Room

80m

ID end-plate

5-7m

Detector Volume

Electrical

Electrical

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ATLAS IBL Readout Structure

16 modules
2 optoboards

IBL stave
IBL optobox on ID endplate

2 FE-IC
DORIC
VDC

Optical BPM
Optical 8b10b
Electrical

IBL optobox on ID endplate

2 optoboards

TIM
BOC
RX
TX
S-Link
ROD
Event building
Control and steering

Control and steering

Ethernet

The Read-Out Driver (ROD) card for the ATLAS experiment

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## Production & Installation Schedule

<table>
<thead>
<tr>
<th>Installation items</th>
<th>Expected time</th>
<th>comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Card production</td>
<td>From July 2013</td>
<td>Prototypes ready in revC</td>
</tr>
<tr>
<td>System testing</td>
<td>June 2013 -</td>
<td>Set-up phase ongoing</td>
</tr>
<tr>
<td>IBL full test</td>
<td>November 2013</td>
<td>Have all the readout and services ready in SR1</td>
</tr>
<tr>
<td><strong>Installation of off-detector parts for readout and power</strong></td>
<td>Jan/Feb 2014</td>
<td>Whenever they can be taken from final SR1 tests</td>
</tr>
<tr>
<td>Cabling of detector in pit</td>
<td>Mar 2014</td>
<td>After IBL installation</td>
</tr>
<tr>
<td>Commissioning tests and sign-off for closure</td>
<td>April-June 2014</td>
<td>Sequence of warm/cold test</td>
</tr>
<tr>
<td>Ready for closure</td>
<td>End June 2014</td>
<td></td>
</tr>
</tbody>
</table>
**IBL Back of Crate Card**

- Timing interface
  - Receive clock from TIM
  - Distribute the clock to detector components and ROD
- Optical interface to/from detector and readout buffers
  - SNAP12 plugins (Tx / Rx)
  - S-Link plugins (QSFP)
- Data en-/decoding for detector communication
  - BPM encoding towards the detector
  - 8b/10b decoding for the detector data to hand over to the ROD
- Monitoring functionalities for detector data