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The Read-Out Driver (ROD) card for the ATLAS experiment: commissioning for the IBL detector and upgrade studies for the Pixel Layers 1 and 2

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The upgrade of the ATLAS experiment at LHC foresees the insertion of an innermost silicon layer, called Insertable B-layer (IBL). IBL read-out system will be equipped with new electronics. The Readout-Driver card (ROD) is a VME board devoted to data processing, configuration and control. A pre-production batch has been delivered in order to perform tests with instrumented slices of the overall acquisition chain, aiming to finalize strategies for system commissioning. In this contribution both setups and results will be described, as well as preliminary studies on changes in order to adopt the ROD for the ATLAS Pixel Layers 1 and 2.

Summary

During the first long shutdown of the LHC collider in 2013/14, the Atlas experiment will be equipped with an innermost silicon layer, called IBL. Read-out electronics have been redesigned in order to accomplish the IBL performances. A new front end ASIC (FE-I4) has been designed as well as new off-detector devices. The latter are two 9U-VME cards called Back-Of-Crate and Read-Out Driver (ROD). The ROD is devoted to data processing, configuration and control of the overall read-out electronics; the number of total boards to be installed on the experiment is . The design is based on modern FPGA Xilinx devices: one Virtex-5 with embedded PowerPC for enhanced control purposes and two Spartan-6 gathering the front-end output, building the events and processing data in dedicated calibration runs. After the first prototyping samples a pre-production batch has been delivered with a finalized layout.
In this contribution it will be described strategies, setups and tests developed for the goal of commissioning the ROD cards into the IBL acquisition system.
In particular, it will be shown how integration tests have been performed by increasing the level of system complexity: slices of the IBL read-out chain are being instrumented and ROD performances are verified in a test bench mimicking a small-size final setup.
In parallel, the firmware is developed and certified under work-cases similar to the ones expected during the IBL data taking. Major achievements from the tests performed with the overall acquisition chain will be emphasized, since their accomplishment is crucial for the successful commissioning of the system.
This contribution will report also an outlook on the possibile adoption of the IBL ROD for ATLAS Pixel Layer 1 and 2. The higher luminosity that will be foreseen into LHC after future upgrades will require more performances for the acquisition system, especially in term of throughput. Estimation of future requisites for the electronics of Layer 1 and 2 will be show and last, it will be discussed whether the adoption of the IBL ROD or an upgraded version could be a viable solution.

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