A 65-nm-CMOS-process-based 10-Gbps VCSEL driver

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Outlines

- 65-nm CMOS for high energy particle physics
  - Our first try on 65-nm process.

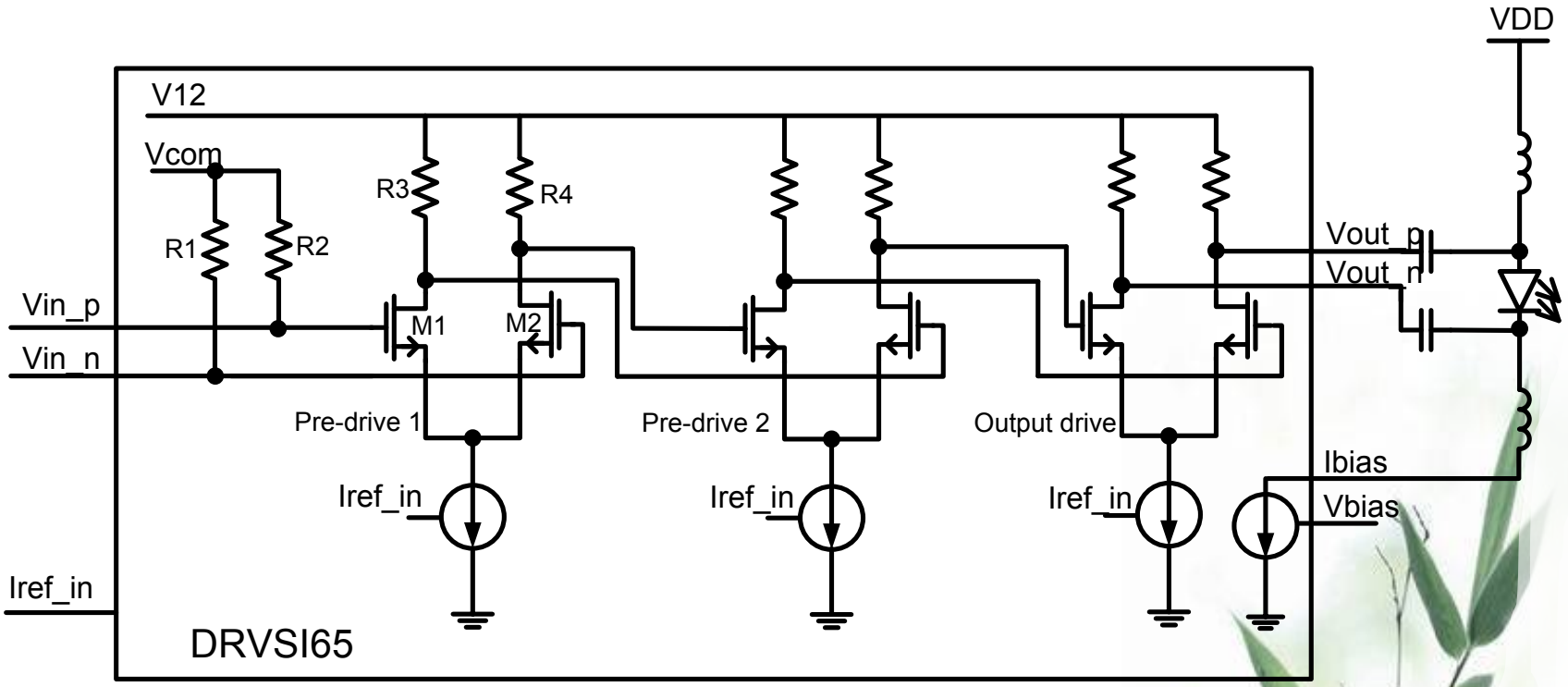
- The VCSEL driver design
- Simulations
- On board test results

- Future work
  - Rad-tolerance potential from process feature
- Summary

Our first try on 65-nm process

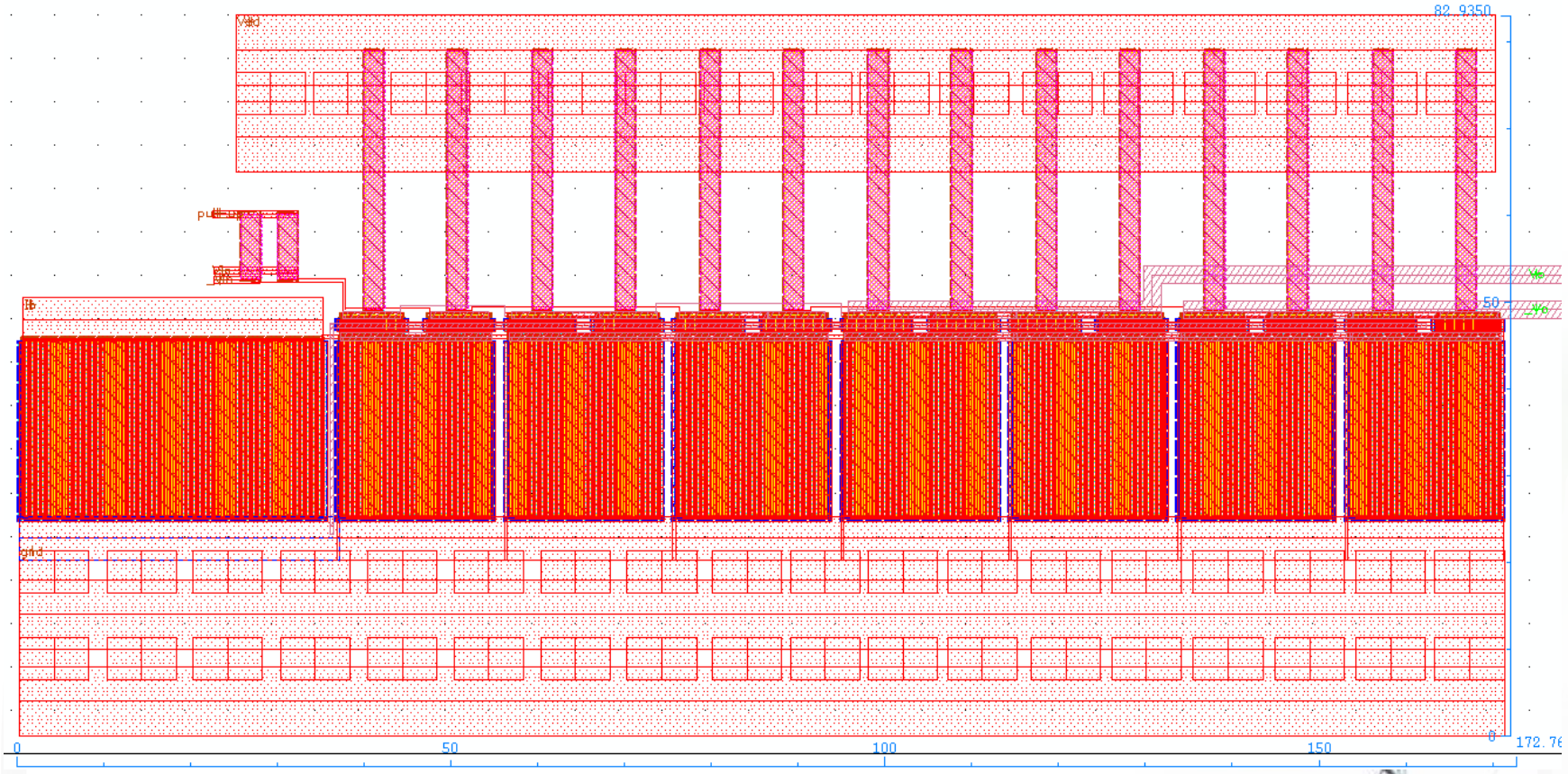
- 65-nm process
  - Logic Low Leakage 1.2/1.8/2.5V
  - 1P8M with 2 top metal
  - Size: 1.5 mm x 1.5 mm
- Free run & one month before the submit date
  - submit date: June 2012
- VCSEL driver with basic structure
  - 10 Gbps in simulation
  - study on process feature & radiation

The VCSEL driver design



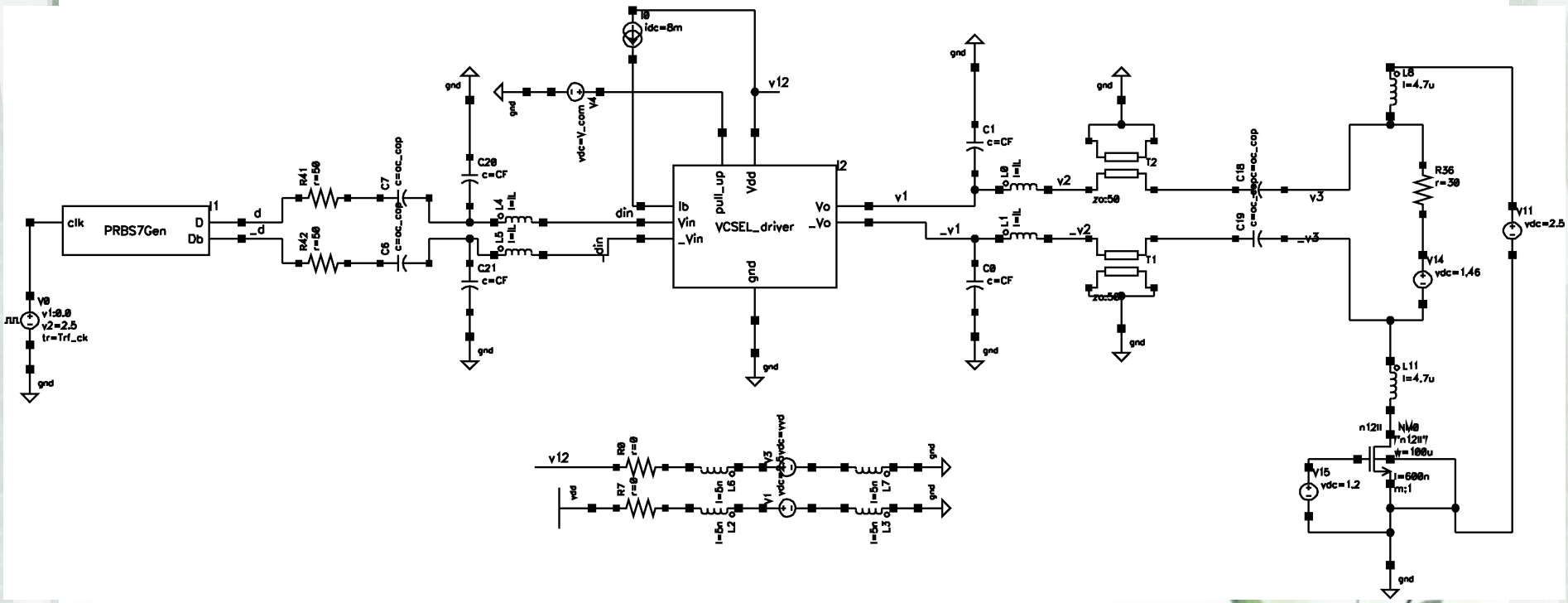
Stage	M0	M1, M2	R3, R4
Per 1	500u/500n, m=1	25u/70n, m=1	R=200,W=2u, L=29.695u
Per 2	1m/500n, m=1	50u/70n,m=1	R=100, W=2u, L=14.85u
Output	1m/500n,m=2	50u/70n,m=2	R=50, W=2u, L=7.425u
Ratio	2	2	0.5

Layout



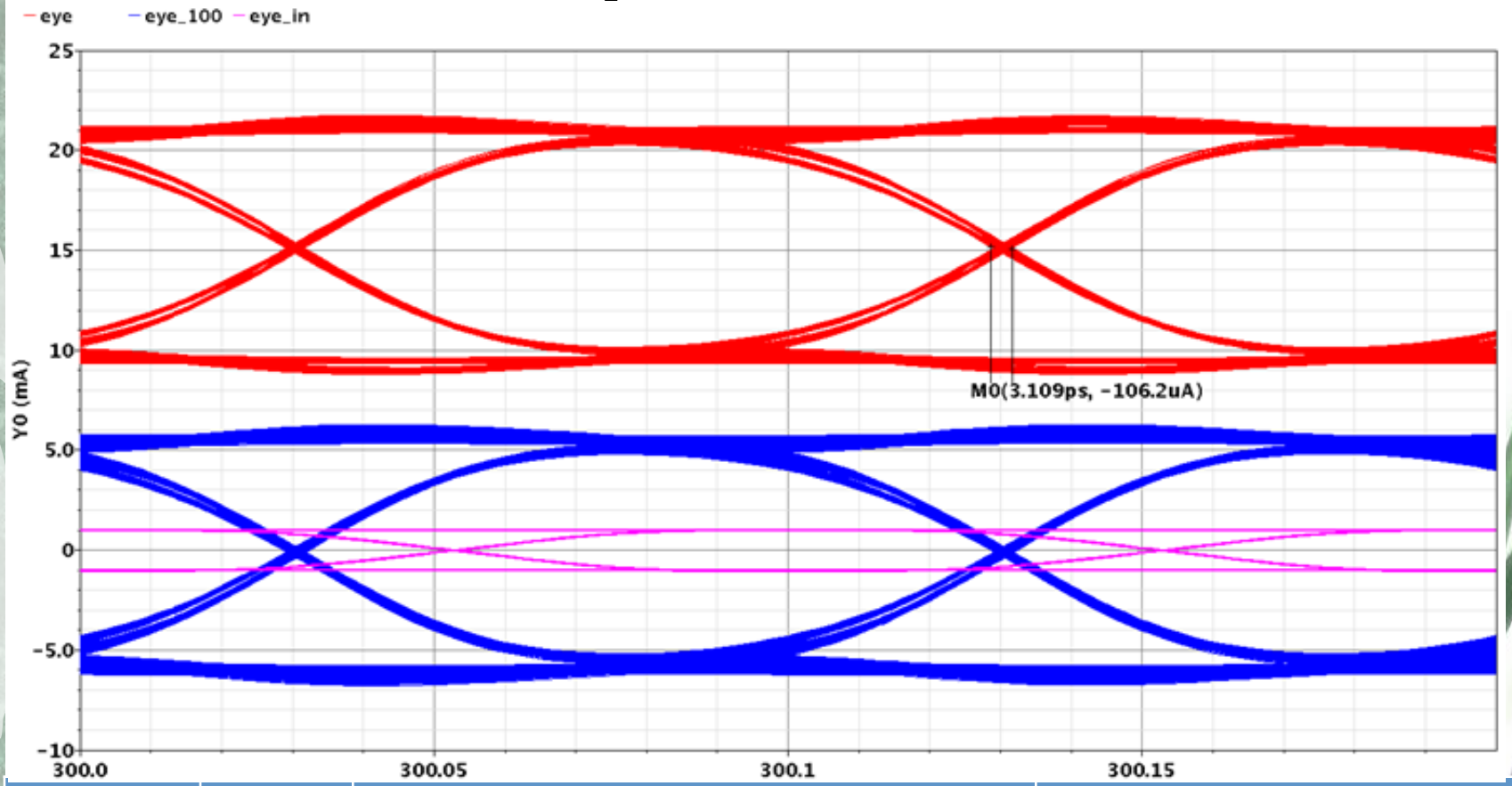
Biase current nMOS is excluded in the above layout.
Size: 170 um x 80 um
A balance layout in three stages.

Pre-layout simulation



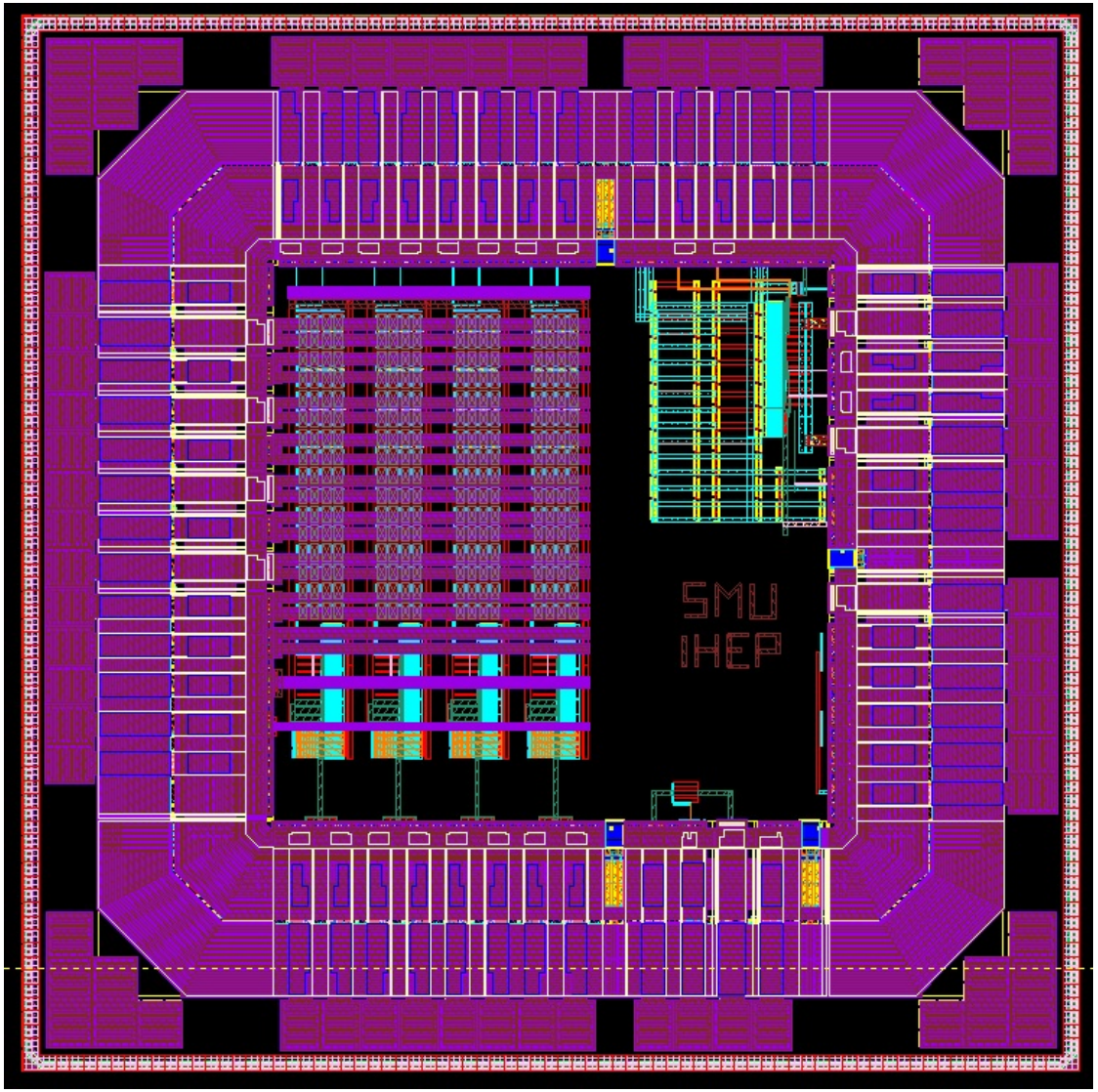
- A 2^7-1 pseudo-random binary sequence (PRBS) generator as the data source.
- 50 ohm resistor and 1.4 V voltage source as the essential VCSEL load.
- 1 nH indouctors and 200 fF capacitors as the bonding wire / package parameters.

Pre-layout simulation



Corner	Temp.	Parameters	Simulation results
Nominal	27 °C	Deterministic jitter (Dj)	3.1 ps
		Eye vertical opening	~10 mA
		Power consumption of V1.2	26.18 mA
		Power consumption of VDD	8.04 mA
		Propagation delay	~75 ps

Tape out

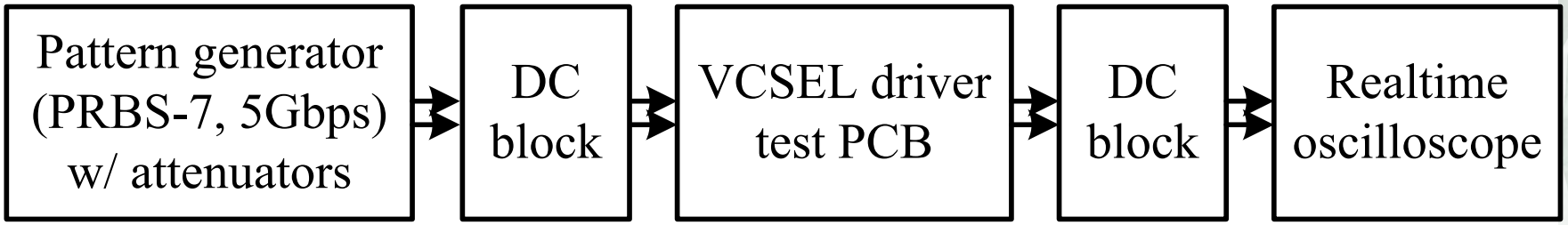


Submitted on: June 2012
Delivered on: Nov. 2012

100 pcs of bare dies

We packaged 50 pcs with QFN-52 package.

On board test results--electrical

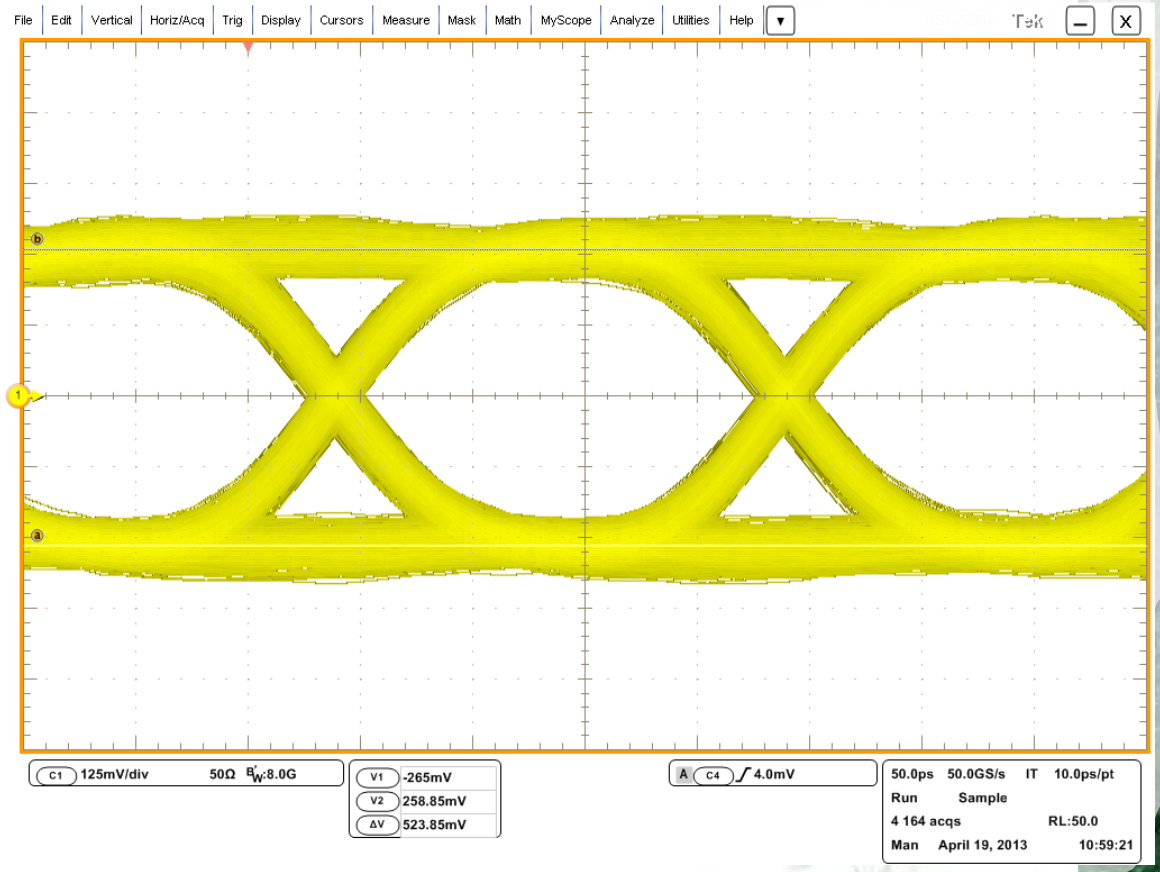


Test unit:
Wire bonded bare die

Inputs:
•200 mV differential 5 Gbps PRBS-7
•AC coupled to a test PCB

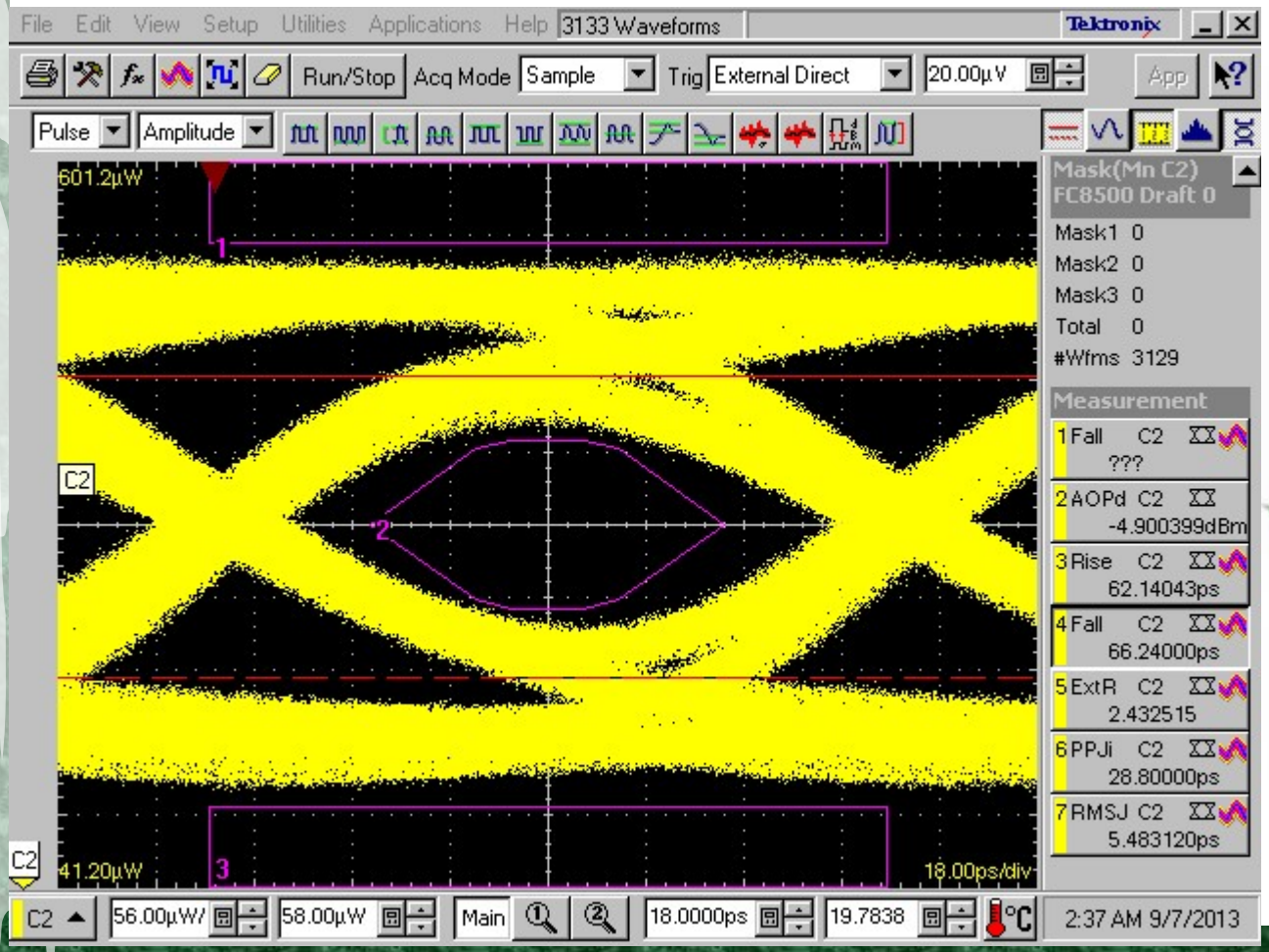
Outputs:
•AC coupled to a realtime oscilloscope differential probe with 8 GHz bandwidth

Eye vertical size: 523 mV
Tj: 30ps



On board test results--optical

- Inputs: Same as the electrial test.
- VCSEL: Finisar HFE6192-261 (10 Gbps)

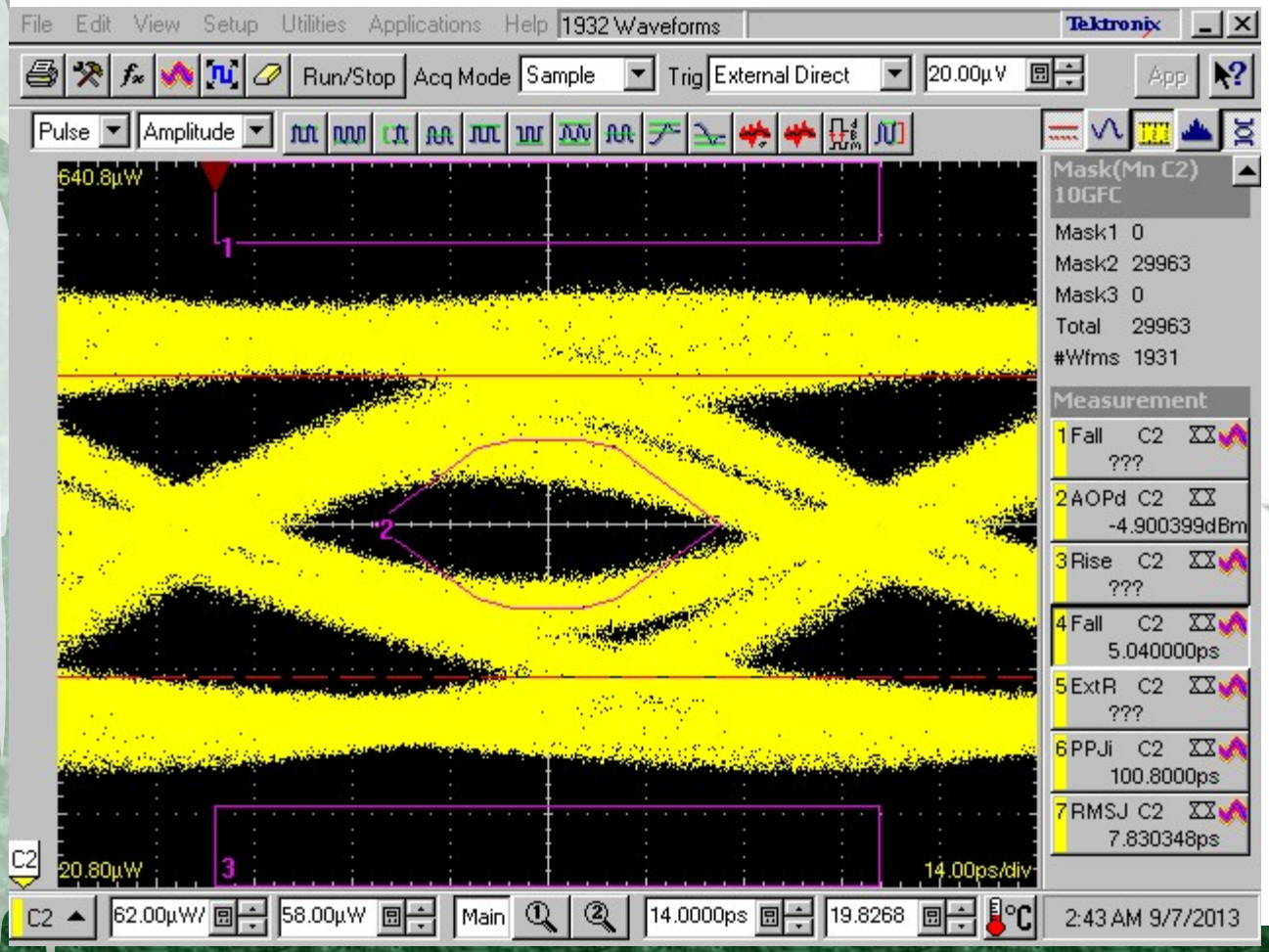


Test unit: packaged

With 8 Gbps inputs, the eye can pass the eye mask test

On board test results--optical

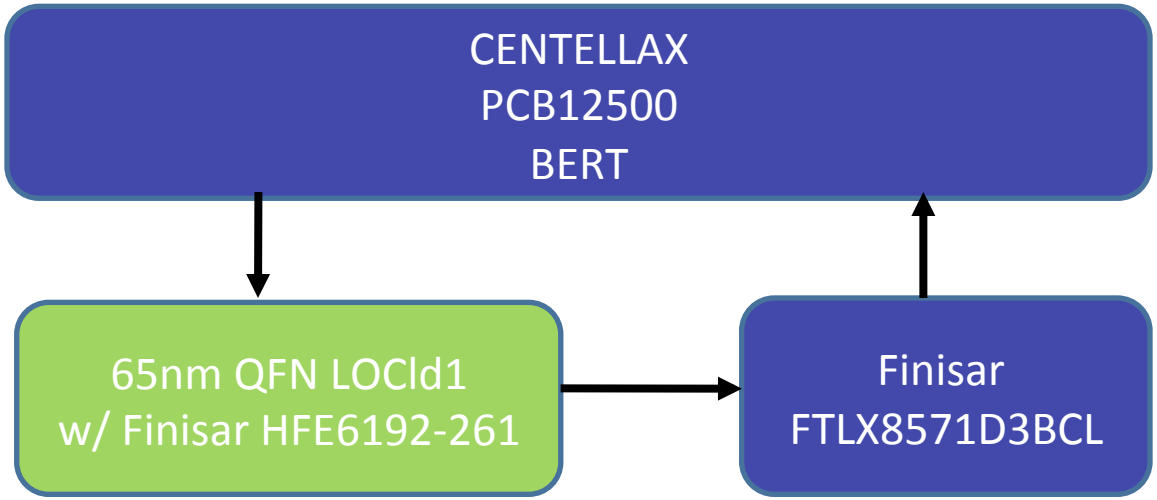
- Inputs: Same as the electrial test.
- VCSEL: Finisar HFE6192-261 (10 Gbps)



Test unit: packaged

With 10 Gbps inputs, the eye cannot pass the eye mask test

On board test results--optical BERT



It passed the BER test (10^{-12} confident level 95%) at

1) 8G, 200 mv differential input
2) 10G, 200 mv differential input

Tests summary

Wire bonded						Packaged					
electrical			optical			electrical			optical		
5G	8G	10G	5G	8G	10G	5G	8G	10G	5G	8G	10G
Tj 30ps	-	-	-	-	-	-	-	-	-	Tj 29ps	Closed

Passed the optical BER test (10^{-12} confident level 95%) at
1) 8G, 200 mv differential input
2) 10G, 200 mv differential input

analyse the design and results

- The reasons for a limited bandwidth:
  - Only a very basic driver structure.
  - There was no post-layout simulation.
  - The bandwidth of IO pad from the process.
  - Parasitic parameters from the package not included in the design.
  - Long bonding wires in the package.

Future work

- Study radiation tolerance on this 65 nm process
  - analog circuits.
  - deep submicron technologies has the advantage in TID effects.
  - sensitivity to the SEU needs to be checked.

Radiation tolerance

The test was done with a neutron beam up to 800 MeV.

Setup: Kintex-7 generated PRBS (2^7-1) at 8 Gbps is sent to DRVSI65. A commercial SFP+ receiver loops back signal to the FPGA which checks for errors.

DRVSI65 is inside the neutron beam. All other components are not.

The test lasted 37.45 hours.

The flux was in average 2.43E+05 n/cm^2/s.

The total fluence was 3.27E+10 n/cm^2 .

No SEU error was observed during the test.

The cross section < 3.06E-11 cm^2.

DRVSI65 will be irradiated with x-rays (maximum energy 160 keV) in the future and the results will be reported in the proceeding.

Summary

- A VCSEL driver has been taped out with a 65nm CMOS process.
- The current test results shown that the design was not as good as we expected.
- More tests are scheduled for both charaterizing and irradiation to provide information for the next design.

- Thank you for your attention.

Backup slides

Electrical inputs from Centellax, 5 Gbps