Contribution ID: **24** Type: **Oral**

A 65-nm-CMOS-process-based 10-Gbps VCSEL driver

Thursday, 26 September 2013 09:50 (25 minutes)

A VCSEL driver has been designed and fabricated in a SMIC 65-nm CMOS process. The preliminary testing results show the ASIC can work at 10 Gbps without peaking or emphasis structures. Due to the thin gate oxide of the technology and large size transistors used in the design, the VCSEL driver is potential radiation tolerant. We will present the irradiation testing results in the conference. To the best of our knowledge, the ASIC is the first VCSEL driver designed in a 65-nm CMOS process for high energy particle physics experiments.

Summary

In this paper, we present a Vertical-Cavity Surface-Emitting Laser (VCSEL) driver ASIC fabricated in a 65-nm CMOS process of Semiconductor Manufacturing International Corporation (SMIC). To the best of our knowledge, the ASIC is the first VCSEL driver designed in a 65-nm CMOS process for high energy particle physics applications.

The design objective is to amplify a 2-mA differential input current to an 8-mA VCSEL modulation current at 10 Gbps. The ASIC consists of three-stage current amplifiers without the use of any inductor peaking or emphasis structures. The VCSEL driver provides a pair of 50-ohm pull-up resistors at the output nodes for impedance matching. The ASIC is biased with a DC current of 6 to 8 mA. The modulation and the biasing currents are externally adjustable.

The VCSEL driver ASIC bare die has been bonded to a printed circuit board and the electrical performance is measured using a high-speed oscilloscope. When the input is a 2^7-1 pseudo-random binary sequence (PRBS) running at 10 Gbps, the measured peak-to-peak jitter in the electrical eye-diagram is less than 20 ps (0.2 UI). The rise and fall times are about 50 ps without the use of any peaking or emphasis structures. With an input of 200 mV, the output current is 4.6 mA under a differential 100-Ω-ohm load. The measured transition times are larger than the simulated results and the measured amplitude is slightly less than the simulated one. The reason is still under investigation. The ASIC will be tested to drive a VCSEL and the testing results will be reported in the conference. The ASIC has been packaged in a 52-pin QFN package. The packaged chips will be extensively tested and the testing results will be reported in the conference.

The SMIC 65-nm CMOS process has a thin gate oxide and is potentially radiation tolerant for total ionizing dose effects. The ASIC is a current driver with large transistor size and is potentially radiation tolerant for single event effects. We will conduct irradiation testing within the next few months and will present the radiation performance of the VCSEL driver in the conference.

For future work, we plan to further improve the VCSEL driver design by adopting inductor peaking or emphasis structures to extend the bandwidth and to also include digital control interface circuit.

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Session Classification: Optoelectronics and Links