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TRB3 264 Channel High Precision TDC Platform and Its Applications

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The TRB3 features four FPGA-based TDCs with <20ps RMS time precision between two channels and 256+4+4 channels in total. One central FPGA provides flexible trigger functionality and GbE connectivity including powerful slow control. We present recent users' applications of this platform following the COME&KISS principle: Successful test beamtimes at CERN (CBM), in Juelich and Mainz with an FPGA-based discriminator board (PaDiWa), a charge-to-width FEE board with high dynamic range, read-out of the n-XYTER ASIC and software for data unpacking and TDC calibration in ROOT. We conclude with an outlook on future developments.

Summary

The 4+1 FPGA board "TRB3" can serve various applications in experimental particle physics and beyond due to its general-purpose design. It uses FPGAs as complex commercial electronic components while realizing the remaining auxiliary parts with simple standard components. Consequently, the board provides flexible connectivity by eight SFP ports and mezzanine extensions for every FPGA including a high pin-out for the peripheral FPGAs. We call this concept COME&KISS: COMplex COMmercial Elements & Keep It Small and Simple. This ensures a wide range of applications in data acquisition scenarios as well as a long-term maintainability of the platform.

Usually, in each of the four peripheral FPGAs a tapped delay line TDC is implemented with <20ps RMS time precision between two channels providing 64 channels plus one reference channel. The TDCs are used for leading edge measurements or by using the TDC channels in pairs, one can additionally extract the width of the digital pulse. The central FPGA serves as a flexible central trigger system and manages slow control and read-out of the peripheral FPGAs over a single gigabit Ethernet connection. The project provides a comfortable, robust and modular software environment, ranging from low-level register access to the FPGA firmwares on the command line to high-level control via web2.0 technologies. This is complemented by comprehensive specifications and documentation.

To convert the analog signals from the detector to digital pulses suitable for the TDC, the front-end electronics board PaDiWa was designed using the differential input buffers of an FPGA as discriminators with a PWM generated voltage as a variable threshold. However, the charge information of the pulse extracted from time over threshold is usually not precise enough for calorimeters. Thus, the leading edge measurement can be complemented by a modified Wilkinson

ADC circuit, which encodes the charge in the width of the digital pulse delivered to the TDC. A proof-of-concept board was successfully tested and a version with an improved dynamic range is currently designed. Both approaches follow again the COME&KISS principle, already enabling other groups to use the existing FEE boards without major modifications. The overall reliability, flexibility and performance of this platform was proven in three test beamtimes with different detectors and FEEs at CERN (CBM), in Juelich and Mainz with up to 2400 channels, of which results are shown.

Furthermore, the TRB3 can be used as an infrastructure to read out specialized integrated solutions using the peripheral FPGAs, for example to provide a timing reference, transport the acquired data to the eventbuilder and slow control configuration of the chip. This was realized for the n-XYTER ASIC. Additionally, the platform enables every user group to profit from common software developments, such as a ROOT unpacker for the TDC datastream including the necessary calibration of the delay lines.

Finally, we present planned extensions of the platform: The detection of leading and trailing edge in a single TDC channel, which doubles the number of channels per board for timestamp and width measurements, and the integration in data acquisition frameworks such as DABC.

Primary author: NEISER, Andreas (Institute of Nuclear Physics, Mainz - Germany)

Co-authors: SCHMIDT, Adrian (Physikalisches Institut IV, Universitaet Erlangen-Nuernberg - Germany); UGUR, Cahit (GSI Helmholtz Centre for Heavy Ion Research GmbH, Darmstadt - Germany); KORCYL, Grzegorz (Jagiellonian University, Krakow –Poland); MICHEL, Jan (Goethe-University Frankfurt - Germany); ADAMCZEWSKI--MUSCH, Joern (GSI Helmholtz Centre for Heavy Ion Research GmbH, Darmstadt - Germany); MAIER, Ludwig (Technische Universitaet Muenchen, Munich - Germany); PENSCHUCK, Manuel (Goethe-University, Frankfurt - Germany); PALKA, Marek (Jagiellonian University, Krakow –Poland); HOEK, Matthias (Institute of Nuclear Physics, Mainz - Germany); TRAXLER, Michael (GSI Helmholtz Centre for Heavy Ion Research GmbH, Darmstadt - Germany); LINEV, Sergey (GSI Helmholtz Centre for Heavy Ion Research GmbH, Darmstadt - Germany); KOENIG, Wolfgang (GSI Helmholtz Centre for Heavy Ion Research GmbH, Darmstadt - Germany)

Presenter: NEISER, Andreas (Institute of Nuclear Physics, Mainz - Germany)

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