

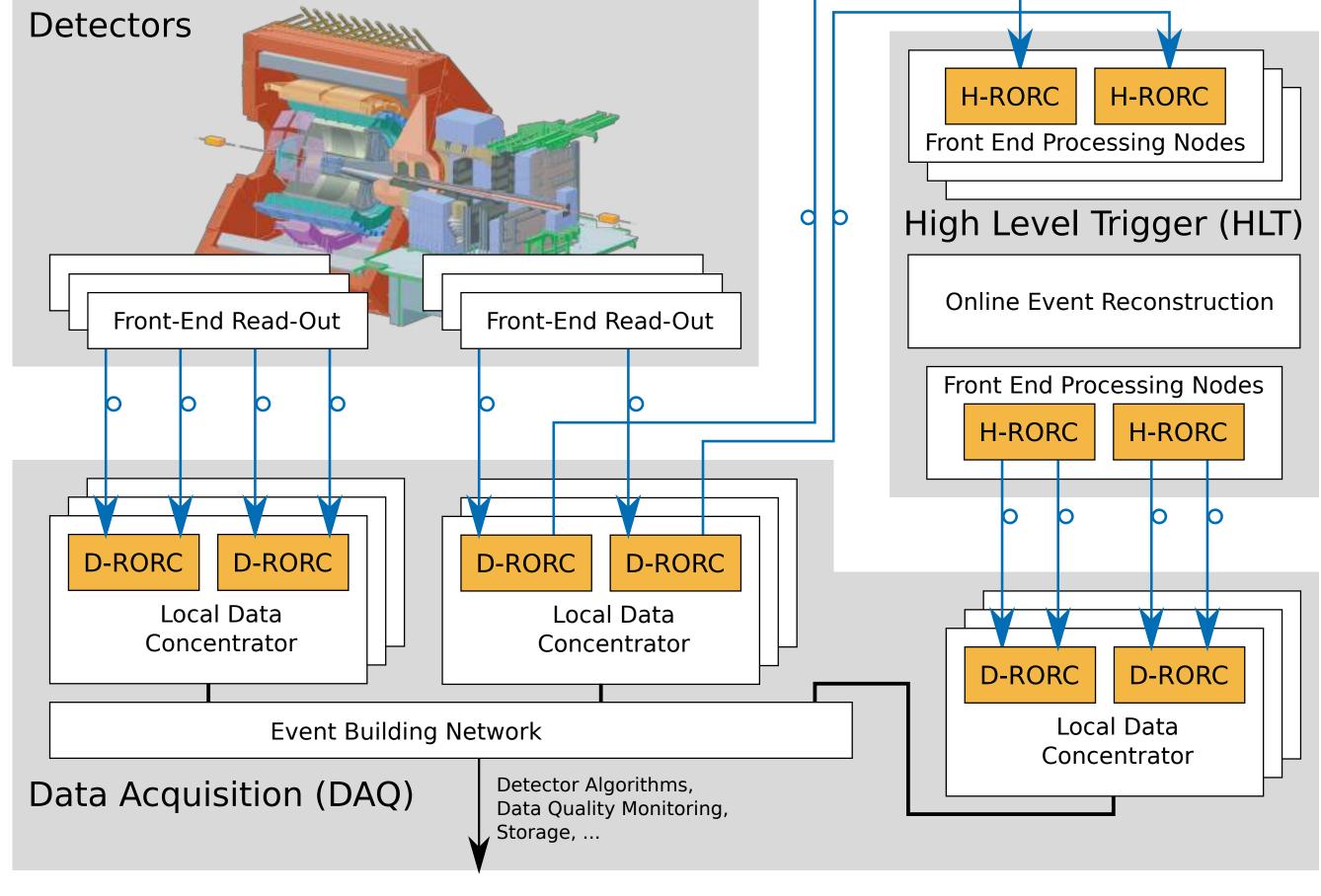
Common Read-Out Receiver Card for the ALICE Run2 Upgrade

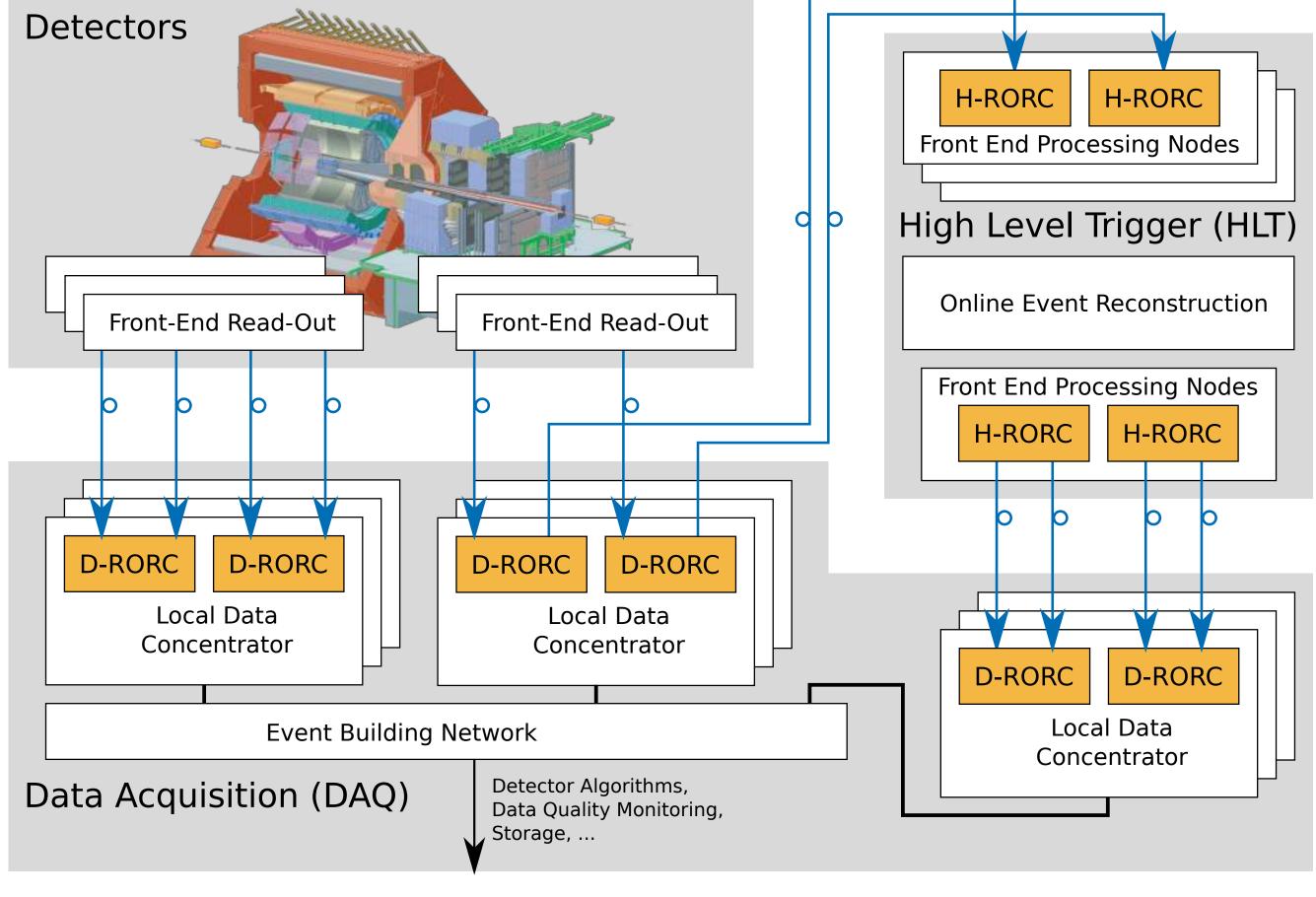
Heiko Engel and Udo Kebschull for the ALICE Collaboration



Chair for Infrastructure and Computer Systems for Data Processing (IRI), Frankfurt University

ALICE Read-Out Architecture





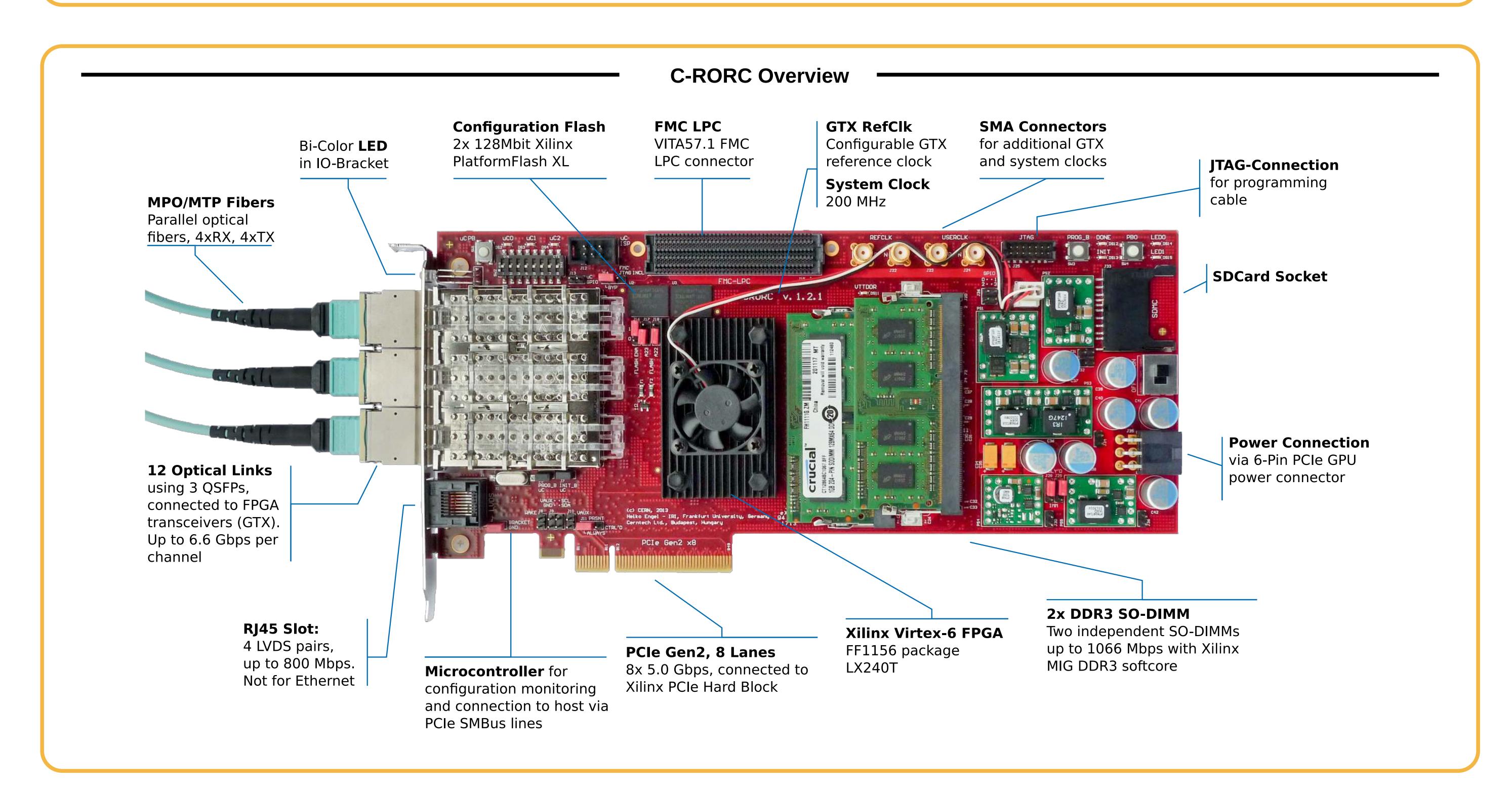
The ALICE experiment uses custom FPGA-based computer plugin cards as interface between the optical detector readout link and the PC clusters of Data Acquisition (DAQ) and High-Level Trigger (HLT). These **R**ead-**O**ut **R**eceiver **C**ards (RORC) have previously been developed as independent projects by Data Acqusition (\rightarrow D-RORC) and High-Level Trigger (\rightarrow H-RORC).

Limitations after Run1:

- Optical interfaces are limited in rate and density
- Obsolete electrical interfaces, especially PCI-X to host PC

Development of a **Common Read-Out Receiver Card** (C-RORC)

- Replacing D-RORCs and H-RORCs
- Compatible with the Run1 link rates and protocols
- Up-to-date interfaces
- Highly increased link density, decreasing number of nodes and costs per link
- Link rate & data preprocessing upgrade possibilities
- PCIe compliant form factor



Features

- Configuration monitoring & management:
 - Onboard storage for multiple configurations
 - Monitor and retrigger configuration process even if PCIe link is down
 - Firmware upgrade via PCIe

Status

- PCB layout and prototype production by Cerntech, HU
- First boards available since Dec. 2012
- Only minor hardware adjustments required
- 2nd series of boards available since May 2013
- Extensive hardware tests of all interfaces and board features over several months

- FPGA configuration within less than 100 ms
- Custom scatter-gather DMA engine with 12 channels
- Host side: Microdriver with userspace library ^[1]
- Online data preprocessing: TPC FastClusterFinder^[2]
- DDR3 tested up to 2x 8GB DDR3 SO-DIMM modules
- PCIe throughput: ~3400 MB/s (SandyBridge)
- Reusing existing fiber installation with break-out fibers and compatible QSFP transceivers
- All hardware tests have been successful by now
- Test setup at CERN and several institutes
- ATLAS will use the same board for their ROS upgrade
 - \rightarrow Common purchase with ATLAS ongoing
- Production of the large series of boards is about to start.

SPONSORED BY THE



05P12RFCAA



[1] *Microdrivers in High-Throughput and Real-Time Environments*, D. Eschweiler and V. Lindenstruth, FIAS Scientific Report 2012 [2] Status of the HLT-RORC and the Fast Cluster Finder, T. Alt and V. Lindenstruth, GSI Scientific Report 2009

Topical Workshop on Electronics for Particle Physics (TWEPP) 2013

Contact: hengel@cern.ch