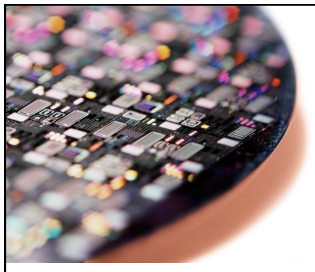
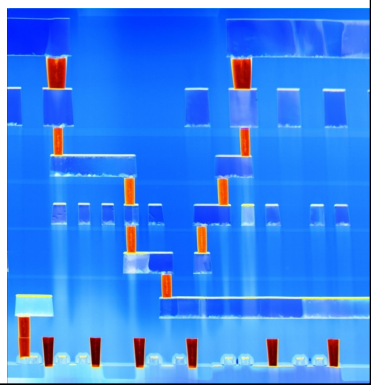


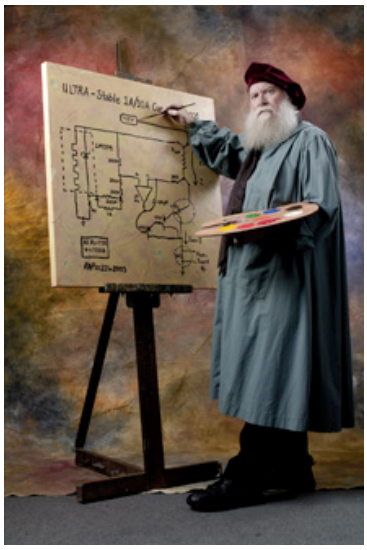
Mismatch in deep-submicron and the consequences for analog designs

Marcel Pelgrom,
www.pelgromconsult.nl
pelgromconsult@kpnmail.nl

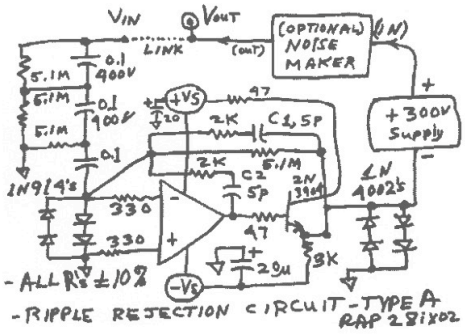
Topical Workshop on Electronics for Particle Physics (TWEPP-13), 24 September 2013 Perugia



Some analog designers are artists…



www.ti.com: in memoriam Bob Pease



…unfortunately most are just scientists!

2

Dilemmas in analog design

Power
Low current
Low capacitances
Low voltage

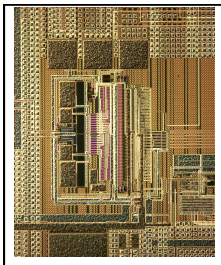
Analog design is about making optimum choices

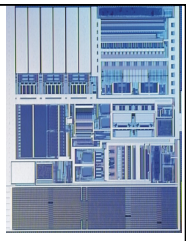
Bandwidth
Short channels
Low capacitances
High current
Bandwidth variation, jitter

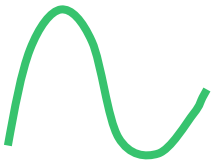
Accuracy
Large device area
High gain
High voltage: signal cascode

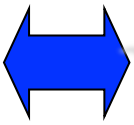
3

Analog-to-digital







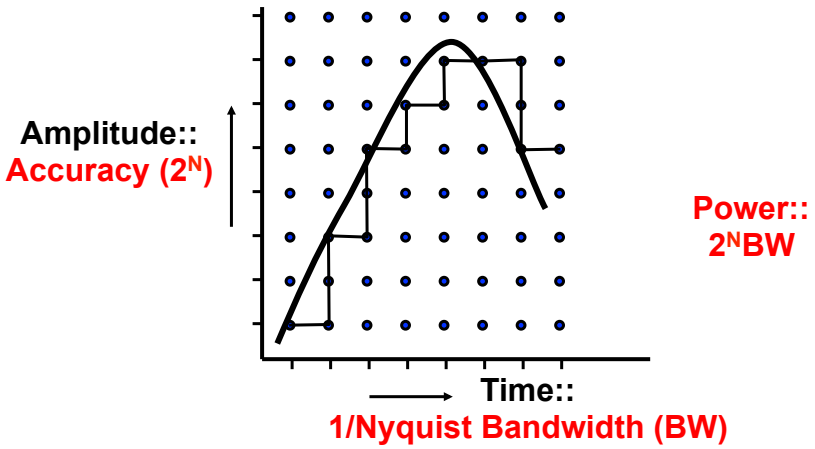


Analog signal:
- Time continuous
- Amplitude continuous
- Physical quantity

Digital signal:
- Time discrete
- Amplitude discrete
- Numerical value

4

Quantization in time and amplitude



5

Insufficient quantization

Insufficient time and amplitude quantization limit the usability of digital signal processing

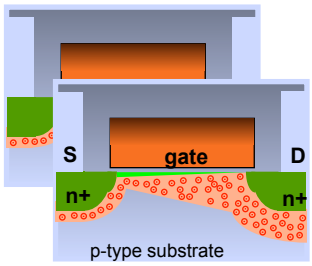
6

Outline

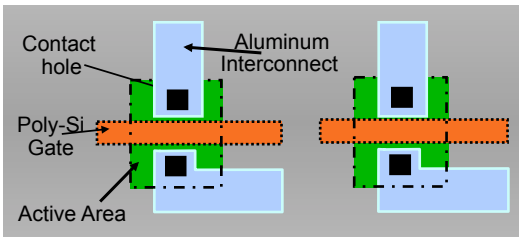
- Mismatch: background and process
- Timing related: Jitter
- Limits
- Solution directions
- Conclusion

7

How equal can we make 2 devices?

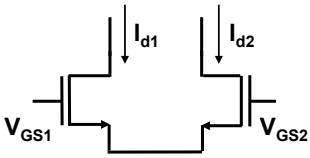


Physical properties
(e.g. N_a, μ, d_{ox})



Layout properties (e.g. W,L)

Electrically



8

Deterministic and Statistical errors

Deterministic	Pseudo random	Random
Supply voltage	Dyn IR drop, WPE	Line edge roughness
Process	Cross talk	Dopant fluctuations
Temperature	Temp gradient	Noise (1/f, kT)
Lithography	jitter	Granularity
Soft breakdown	Substrate noise	Interface states
Stress, STI, wire	Hot carrier, NBTI	Work-function fluct.
IR drop,	Drift	Fixed-oxide charges
Wiring differences	CMP density	

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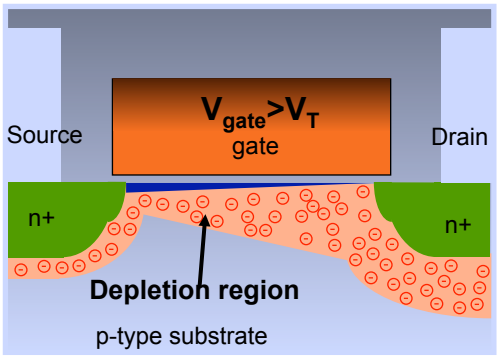
Classical MOS transistor



$V_{drain}>V_{gate}-V_T$

The main source of variation in many semiconductor devices is in the varying number of dopants in the depletion region (Random dopant fluctuation).

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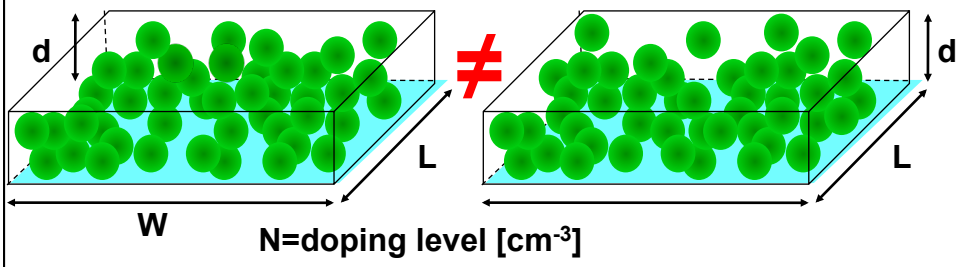
Basic mismatch model



The number of dopants in a certain volume is on average controlled by the average implantation dose N_a.

However, in one specific volume the actual number will fluctuate from one volume to another due to random processes.

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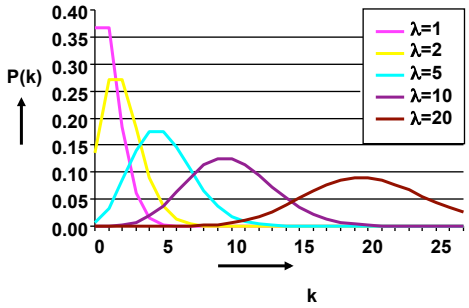
Statistics for mismatch

Probability of having k ions in the box if the average is λ ions, is given by a Poisson distribution:

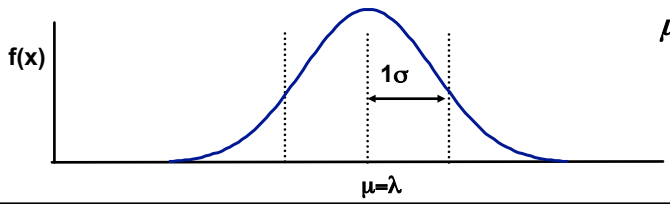


$$p(k) = \frac{e^{-\lambda}\lambda^k}{k!}$$

Where λ is the average number of ions

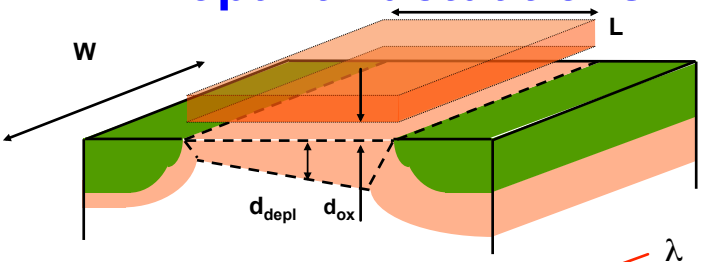
For large λ →Gaussian distribution with:

$$\mu = \sigma^2 = \lambda$$



12

Dopant fluctuations



λ

$$V_T - V_{FB} = \frac{Q_{bulk}}{C_{gate}} = \frac{q N_a W L d_{depl}}{C_{ox} W L},$$

matching : 2 transistors

$$\sigma_{\Delta VT} \propto \frac{d_{ox}\sqrt[4]{N_a}}{\sqrt{W \times L}} \Rightarrow \boxed{\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{W \times L}}}$$

⇒ factor $\sqrt{2}$

More accuracy→large area→large capacitive load→higher power
[Stolk et al., slide 97] have included the random distribution in depth,
Correction factor √(4/3).

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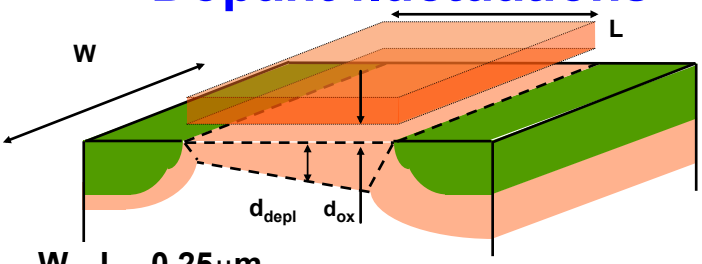
Dopant fluctuations



$W = L = 0.25\,\mu m$

$d_{depl} \propto \frac{1}{\sqrt{N_a}} \approx 0.1\,\mu m$ ⇒ $N_{act,depl} \approx 1000$ atoms

(Next to 10^9 Si-atoms)

$N_a \approx 2 \times 10^{17}\ cm^{-3}$

P approximates a normal distribution with parameters:

Mean value $\mu_N = n \times \mu_x$, $N_{act,depl} \approx 1000$ atoms

Standard dev. $\sigma_N = \sqrt{n} \times \mu_x$ $\sqrt{N_{act,depl}} \approx 30$ atoms

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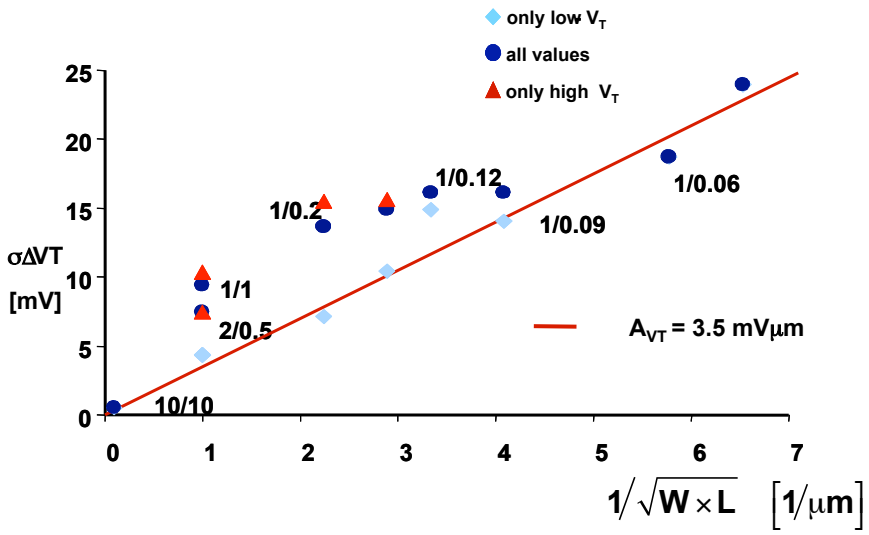
CMOS65 NMOS matching



Ref: N. Wils, H. Tuinhout

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Granularity: stochastic variation

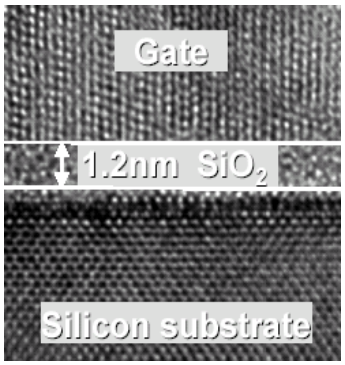

photo: Intel

Granularity on molecular level is reached:

0.25/0.25 transistor = 1000 doping atoms

0.1/0.065 transistor = 60-80 atoms

(Shockley SSE 1960, granularity means: no continuous change in doping, but in discrete portions, i.e. 1 electron charge 1.6 10^{-19} C)

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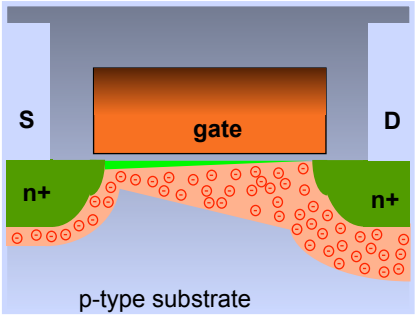
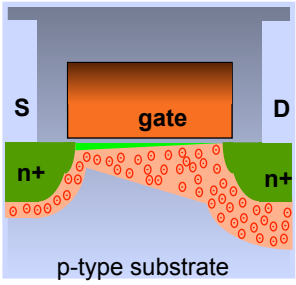
Matching and technology scaling





$$\sigma_{\Delta VT} \propto \frac{d_{ox}\sqrt[4]{N_a}}{\sqrt{W \times L}}$$

d_{ox} ↓

$\sqrt[4]{N_a}$ ↑

Hence: V_T matching **improves** for more advanced technologies

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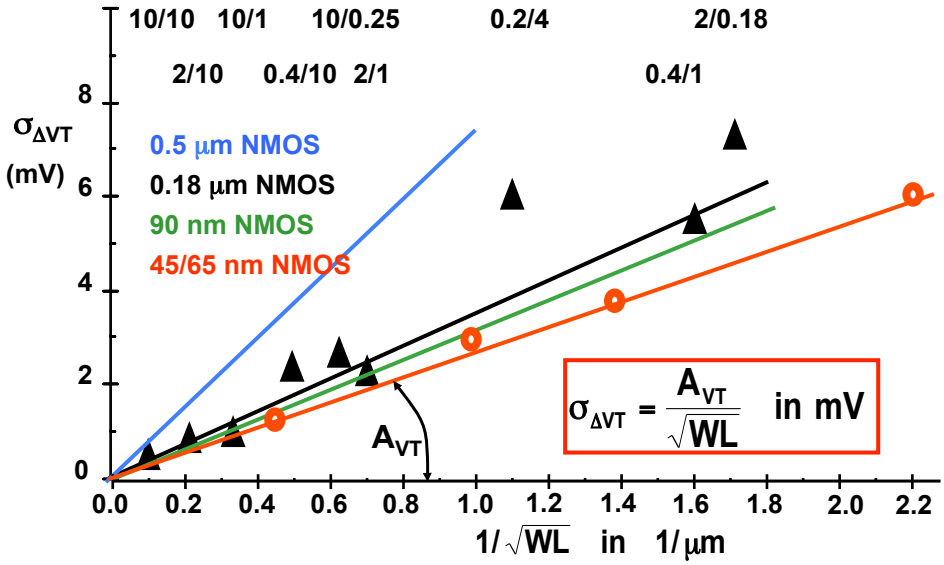
CMOS matching



Ref: M. Pelgrom IEEE JSSC 1989 p. 1433, Tuinhout, Wils, and work by many others

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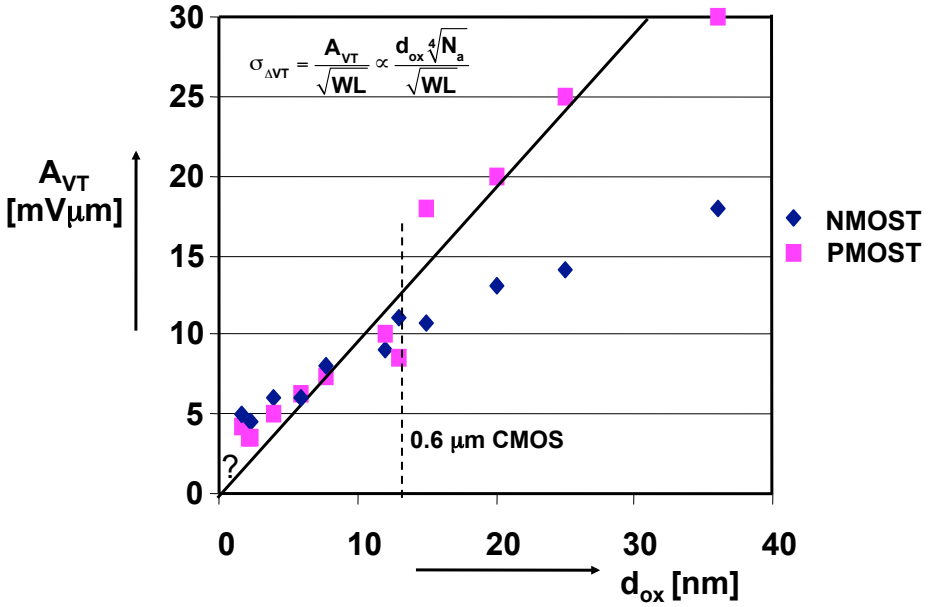
V_T matching for CMOS generations



Ref: Pelgrom, Tuinhout, Vertregt AACD2012, for 28, 22 nm see pdk of foundry

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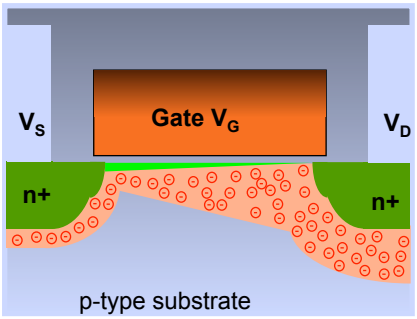
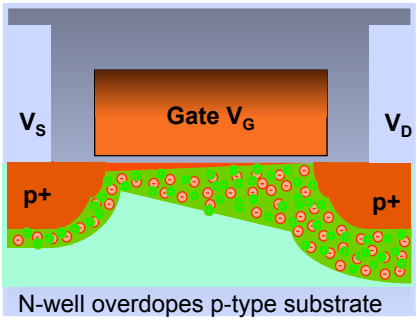
CMOS compensating dopes





$$V_T \propto WLy \times N_a$$

$$\sigma_{\Delta VT} \propto \sqrt{WLy \times N_a}$$

$$V_T \propto WLy \times (N_a - N_d)$$

$$\sigma_{\Delta VT} \propto \sqrt{WLy \times (N_a + N_d)}$$

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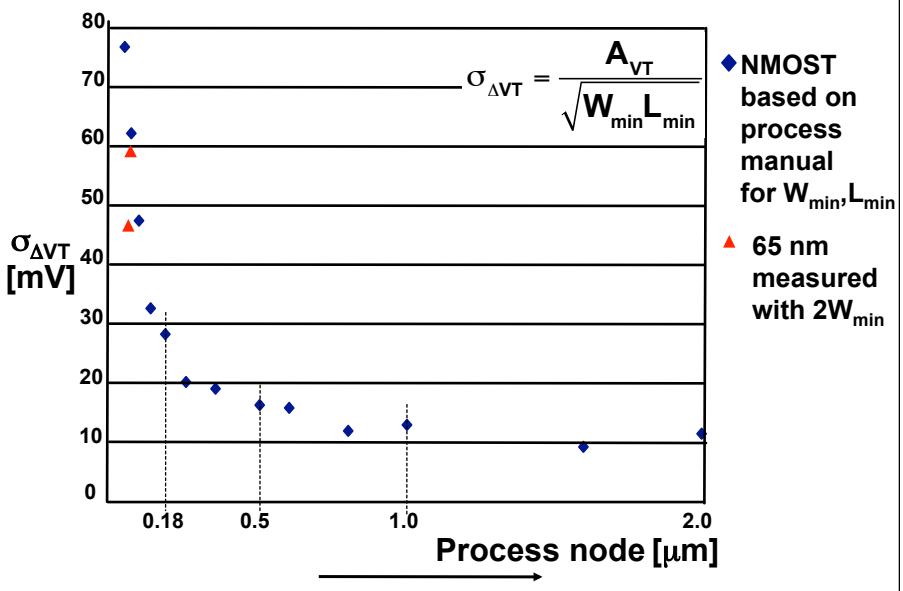
V_T matching minimum size transistor



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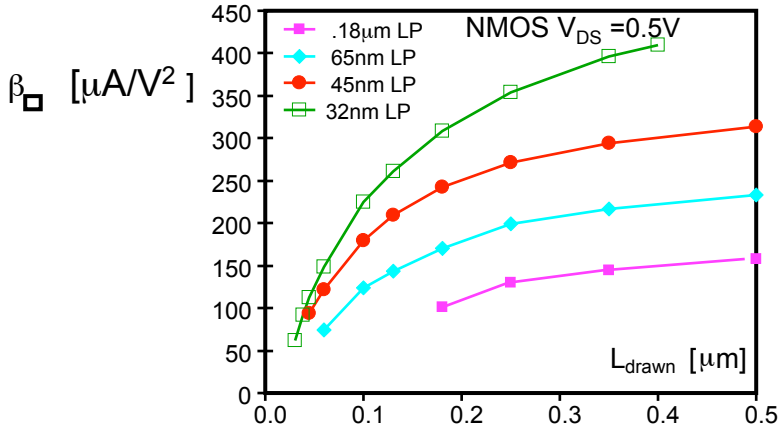
Hope on the horizon



Backing off on transistor length:

- W/L decreases -30%
- $\beta_{\square}$ increases +20%
- σ_{ID}/ID decreases +20%
- static leakage -90%
- gatecap increase +30% ?

From: M. Vertregt IEDM 2006

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Modeling valid for other devices

	Description	Value
MOS transistors	$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{WL}}$	A_{VT} = 1mVμm/nm
MOS transistors	$\frac{\sigma_{\Delta\beta}}{\beta} = \frac{A_{\beta}}{\sqrt{WL}}$	A_{β} =1-2%μm
Bipolar transistors BJT	$\sigma_{\Delta VBE} = \frac{A_{VBE}}{\sqrt{W_B L_B}}$	A_{VBE} = 0.3mVμm
Diffused or poly resistors	$\frac{\sigma_{\Delta R}}{R} = \frac{A_R}{\sqrt{WL}}$	A_R =0.5-5%μm
Plate, fringe capacitors	$\frac{\sigma_{\Delta C}}{C} = \frac{A_C}{\sqrt{C}}$	A_C =0.3%/√(C in fF)

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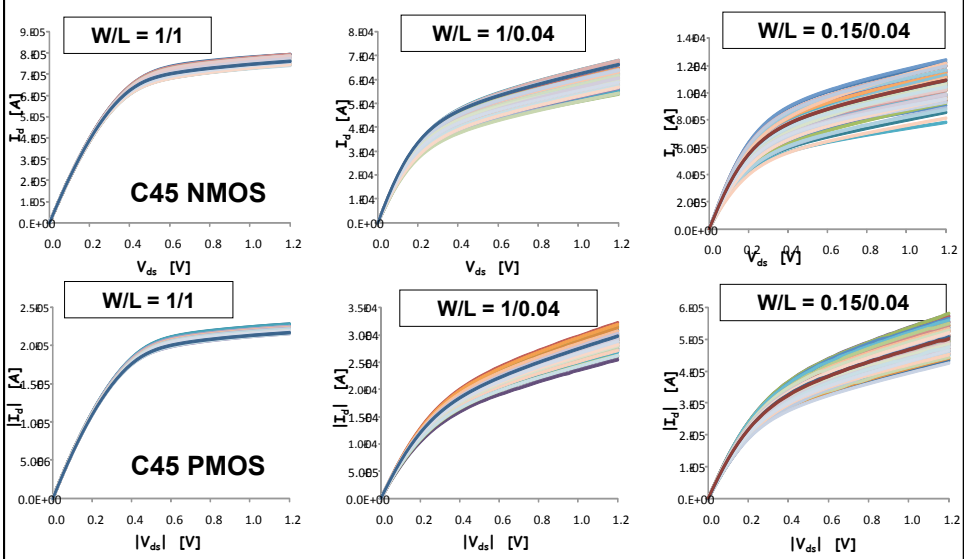
Mismatch: 45 nm CMOS



C45 NMOS and PMOS: I_d-V_{ds} for 3 different W/L ($|V_{gs}|$ = 1.1V)

Courtesy: N. Wils and H. Tuinhout 2011

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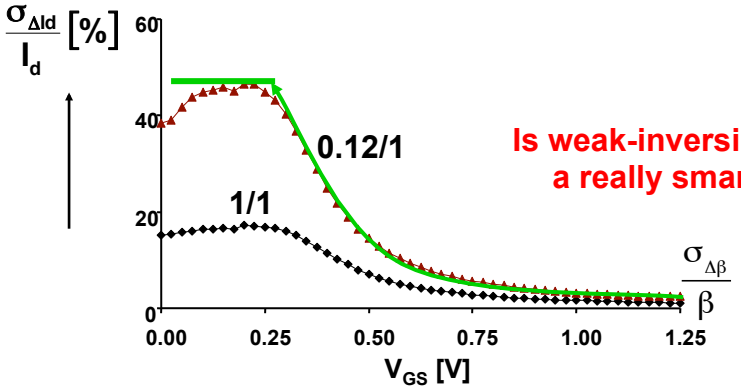
Back of the envelope

$$I_d = I_0 e^{\frac{q(V_{GS}-V_T)}{mkT}} \Rightarrow \qquad I_d = \frac{\beta}{2}(V_{GS}-V_T)^2 \Rightarrow$$

$$\frac{\sigma_{\Delta Id}}{I_d} = \frac{\sigma_{\Delta VT}}{mkT/q} \qquad \frac{\sigma^2_{\Delta Id}}{I_d^2} = \frac{4\sigma^2_{\Delta VT}}{(V_{GS}-V_T)^2} + \frac{\sigma^2_{\Delta\beta}}{\beta^2}$$

Weak Inversion **Strong Inversion**



Is weak-inversion design a really smart idea?

Source data: N.Wils, H Tuinhout

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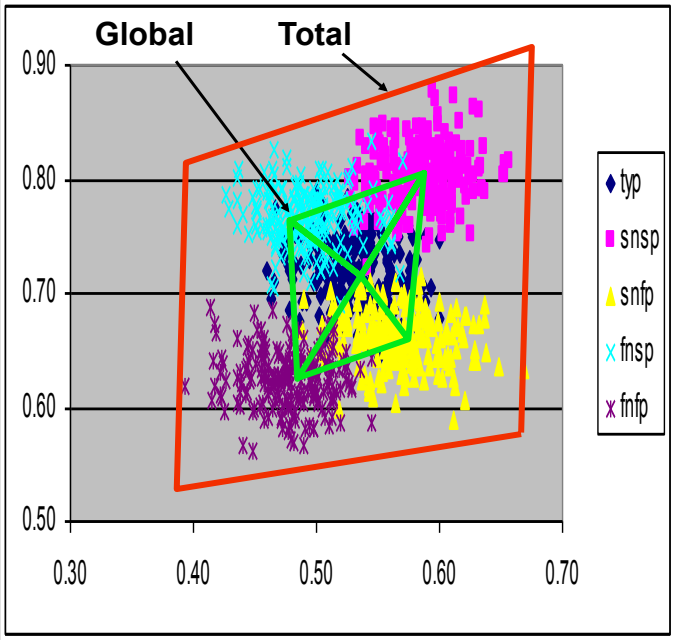
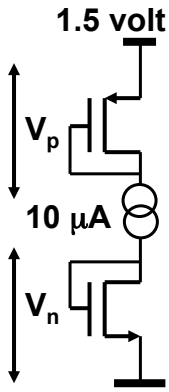
Matching: CMOS 90nm, W/L=0.2/0.1





(simulation)

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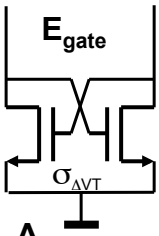
Mismatch energy



$$\sigma_{\Delta VT} = \frac{A_{VT}}{\sqrt{W \times L}}, \quad C_{gate} = WLC_{ox}$$

$$E_{gate} = C_{gate} \times \sigma^2_{\Delta VT} = C_{ox} A^2_{VT}$$

Transistor mismatch dominates in design:

- **Major issue in many analog multiplexed designs**
- **Starts bothering digital designers**
- **Power issue, but independent of W,L choice**

Ref: Pelgrom 1994, Kinget 1996

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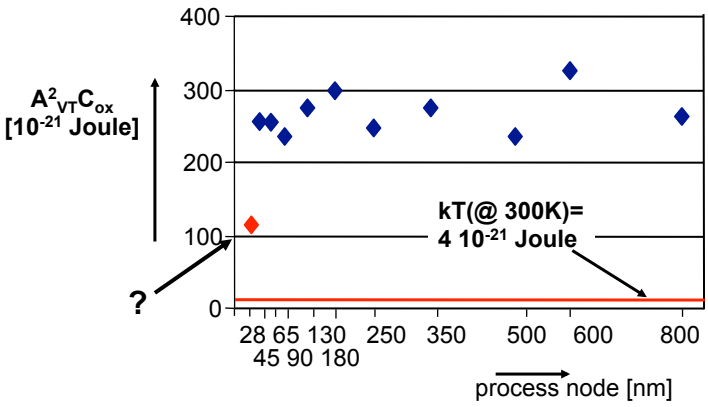
Mismatch energy

Energy to overcome threshold mismatch with 1σ certainty:

$$\sigma^2_{VT} \times C_{gate} = A^2_{VT} C_{ox}$$



Note that mismatch energy directly links to the power budget and is 70x higher than thermal noise energy.

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Outline

- Mismatch: background and process
- Timing related: jitter
- Limits
- Solution directions
- Conclusion

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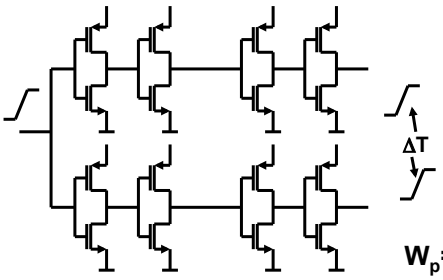
Digital clock tree



Note: the delay difference in one specific pair of buffers is time-invariant
Not the same as jitter

$W_p=2W_n=8L_{min}$

	0.25 μm	0.18 μm	0.13 μm	90 nm	65nm
Clock period	10 ns	5 ns	2 ns	1 ns	500 ps
$\sigma_{\Delta T}$ (C_{load}=50fF)	16 ps	21 ps	38 ps	68 ps	88 ps
$\sigma_{\Delta T}$	16 ps (50 fF)	16 ps (35 fF)	22 ps (25 fF)	33 ps (20 fF)	32 ps (15 fF)

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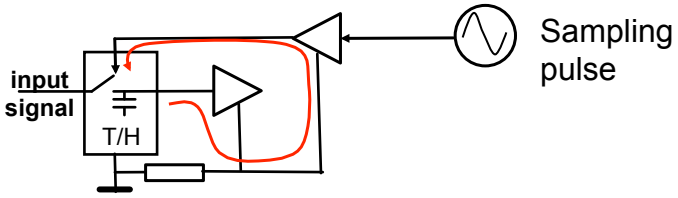
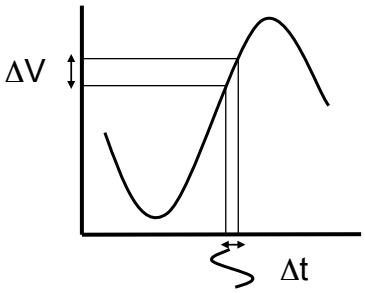
timing jitter: amplitude errors





Time jitter is caused by:
Noise during generation
Parasitic coupling between lines
Substrate coupling
power supply rejection

Timing jitter results in:
Noise, distortion and offset

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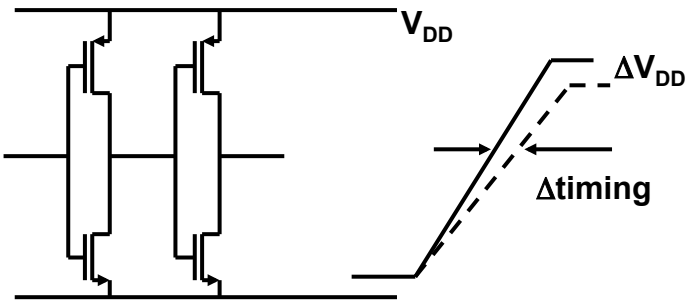
timing offsets: clock distribution



- 10% power supply variation gives ≈ 5% timing edge variation with 60 ps rise time that easily translated into 3-5 ps jitter
- Use separate power connections for digital and analog clocks

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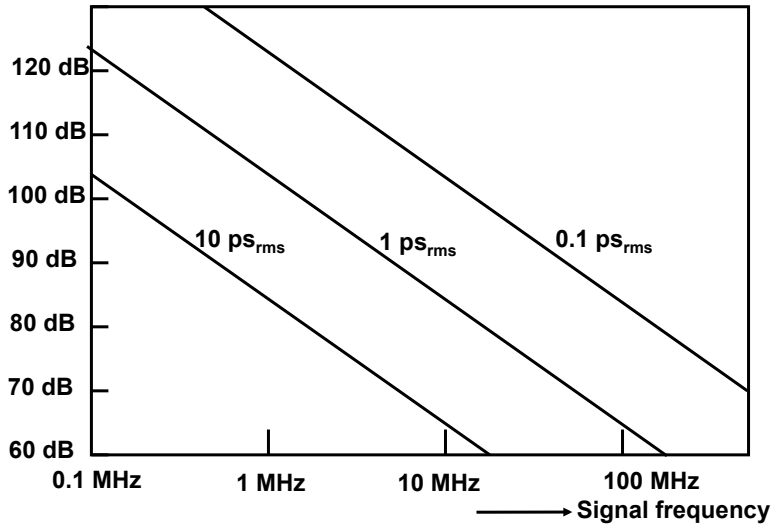
SNR due to jitter



(Epson, quartz EG2011 50-170 MHz: 3 ps rms
Programmable oscillator SG8002: 25 ps rms jitter)

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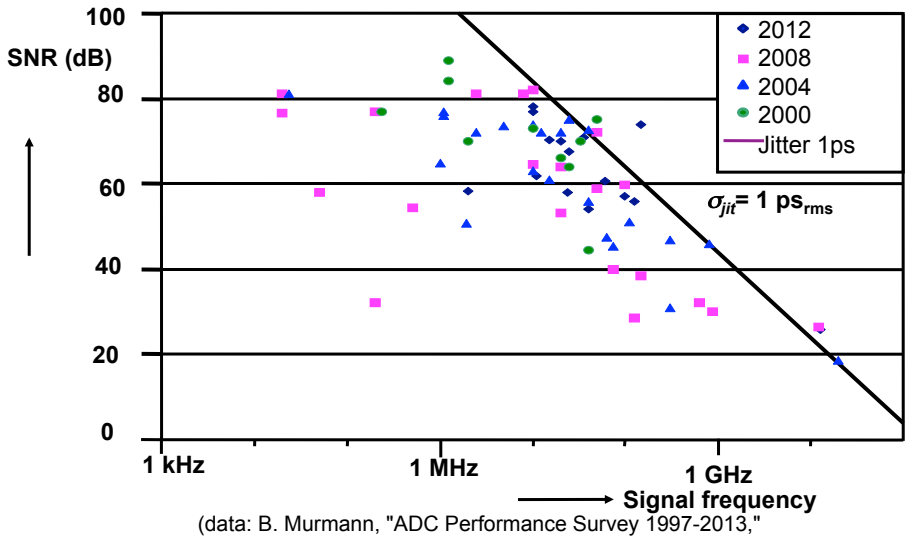
SNR loss due to jitter in ADCs



(data: B. Murmann, "ADC Performance Survey 1997-2013,"
Available: http://www.stanford.edu/~murmann/adcsurvey.html)

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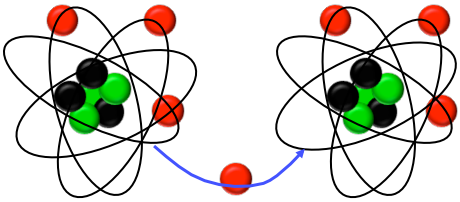
Challenge: Electrical and optical jitter

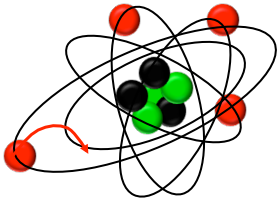
Jitter in Electrical pulses:
Oscillators, PLLs on-chip
> 1picosec$_{rms}$

Electrical design is based on electrons moving from one atom to the next.



Jitter in Optical pulses:
e.g. Ytterbium lasers
below 1 femtosec$_{rms}$

Optical design is based on electrons moving from one orbit to another in one atom.



Cf. Tom Lee, Stanford

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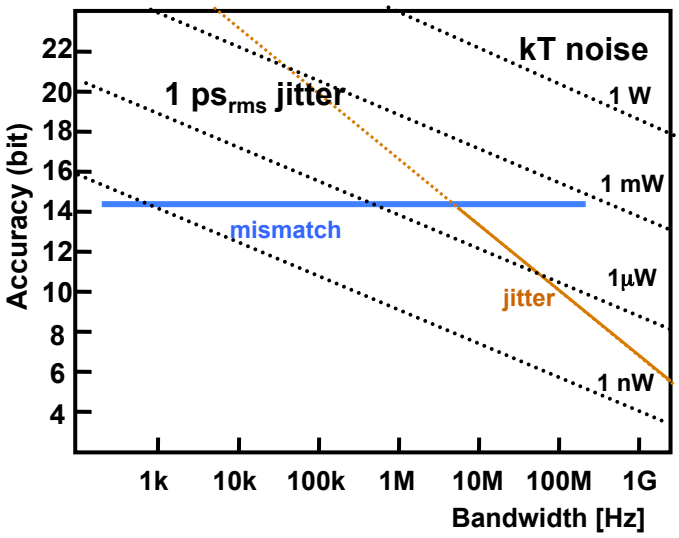
Limits to conversion



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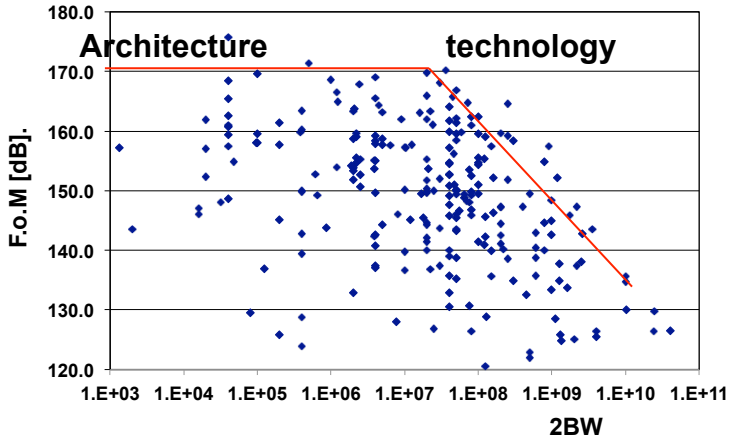
F.o.M. Benchmark



Architectural and technological borders
B. Murmann, "ADC Performance Survey 1997-2013," [Online].
Available: http://www.stanford.edu/~murmann/adcsurvey.html

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Solutions in analog design

Power
Duty-cycling

Analog design is about making optimum choices

Bandwidth
Time interleaving
Compressive sampling?

Accuracy
(Incremental)
Sigma-Delta conversion

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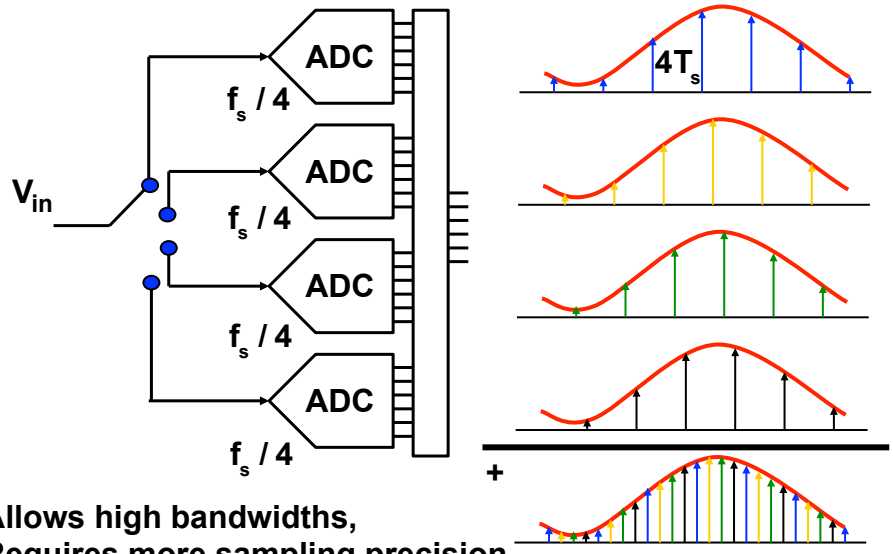
Time-interleaved processing



Allows high bandwidths,
Requires more sampling precision
Sensitive to Jitter, skew, mismatch

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Conclusion

Accuracy, Power and Bandwidth remain the main challenges for the next decade in IC design.

Some aspects of accuracy are fundamental: atoms don't scale and noise is inevitable.

In analog design component mismatch can be statistically estimated and corrected. This allows to remove unnecessary overdesign.

Many interesting research challenges ahead!

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