



Contribution ID: 0

Type: Oral

## How to create successful open hardware projects - about White Rabbits and open fields

Wednesday 25 September 2013 14:49 (26 minutes)

CERN's accelerator control group has embraced "Open Hardware" (OH) to facilitate peer review, avoid vendor lock-in and make support tasks scalable. A web-based tool for easing collaborative work was set up and the CERN OH Licence was created. New ADC, TDC, Fine delay and carrier cards based on VITA and PCI-SIG standards were designed and drivers for Linux were written. Often industry was paid for developments, while quality and documentation was controlled by CERN. An innovative timing network was also developed with the OH paradigm. Industry now sells and supports these designs that find their way in new fields.

### Summary

The CERN team responsible for the infrastructure that controls the accelerators decided in 2009 that it would put a strong effort in making sure that new electronics would be available as "Open Hardware". By having access to all design information, CERN is able to correct bugs immediately, can repair or rebuild and improve electronics even when the original developer or company is not able to do so anymore.

Unfortunately, at that time no open designs were available with the required functionality, nor was there an infrastructure present that allowed professional engineers to easily collaborate and share information. Therefore a web-based collaboration tool ([ohwr.org](http://ohwr.org)) was first developed where all design data could be stored, issues could be tracked and communications made. The CERN Open Hardware Licence was created because existing licences did not cover the specific needs for hardware developments.

The team decided that to stimulate collaborations new hardware would be based on VITA and PCI-SIG standards such as FMC (FPGA Mezzanine Card), PCI Express and VME64x. As system-on-chip interconnect the public domain Wishbone specification would be used while drivers for Linux would be written.

Rather general purpose ADC, TDC and Fine Delay mezzanines that can be mated with VME64x and PCI Express carriers are examples of boards that were developed in this way. Often help was called in from industry for development work, while the CERN team reviewed the results and finalised them to have consistent quality and documentation. Particular effort was spent on making reusable firmware, high quality production specifications and on setting up comprehensive production test systems.

In the same period the team needed to develop a new timing network for CERN's future control systems. From the start this so-called White Rabbit project was set up as a collaboration between institutes and industry. This innovative network allows sub-ns precision synchronization of many nodes over a span of more than ten kilometres while it simultaneously can be used to send Ethernet data. The developed White Rabbit switch, hardware and firmware allow for novel applications such as wide area triggering and sub-ns time tagging of data and make the open hardware projects even more appealing.

To guarantee that the projects could easily find their way to other users without being dependent on CERN, engineering companies were asked to not only produce the hardware for CERN but also to add them to their own product catalogue. To assure quality CERN closely followed the production. By April 2013 sixteen companies have been involved in the development, production and sales of over ten open hardware and related open software projects. These same companies also support the designs, allowing the scaling of the number of users.

The open hardware designs originally made for CERN are now finding their way in diverse fields such as telescope arrays, national metrology networks and industrial applications which makes them even more in-

teresting to the participating companies while the sharing of experience improves the quality and efficiency of these publicly-funded projects.

**Primary authors:** VAN DER BIJ, Erik (CERN); SERRANO, Javier (CERN)

**Co-authors:** GOUSIOU, Evangelia (CERN); DANILUK, Grzegorz (AGH University of Science and Technology (PL)); GONZALEZ COBAS, Juan David (CERN); LEWIS, Julian (CERN); LIPINSKI, Maciej Marek (Warsaw University of Technology (PL)); CATTIN, Matthieu (CERN); ARRUAT, Michel (CERN); VOUMARD, Nicolas (CERN); STANA, Theodor (CERN); WLOSTOWSKI, Tomasz (CERN)

**Presenter:** VAN DER BIJ, Erik (CERN)

**Session Classification:** Systems, Planning, Installation, Commissioning and Running Experience