Contribution ID: **96** Type: **Poster**

Development of CMOS Pixel Sensor with digital pixel dedicated to future particle physics experiments

Tuesday, 24 September 2013 17:04 (1 minute)

Two designs of CMOS pixel sensor with in-pixel analog to digital conversion have been prototyped in a 0.18μm CIS process. The first design integrates a discriminator into each pixel within an area of 22×33μm2 in order to meet the requirements of the ALICE-ITS upgrade. The second design features 3-bit charge encoding inside a 35×35μm2 pixel which is motivated by the specification of the outer layers of ILD vertex detector. This work is to validate the concept of in-pixel digitization which offers higher readout speed, lower power consumption and less peripheral surface of active area compared to column-level charge encoding.

Summary

CMOS pixel sensors have become an attractive alternative in tracking and vertex detecting when priorities are given to high granularity and low material budget with sufficient readout speed and moderate radiation tolerance. The state-of-the-art ULTIMATE (MIMOSA28) sensor equipping the STAR-PXL upgrade was developed at IPHC and fabricated in a 0.35μm OPTO CMOS process [1]. It features in-pixel signal amplification and CDS with column level discriminator followed by zero suppression circuit to provide sparse outputs. A rolling shutter mode is employed to read out the matrix row by row in favor of power consumption. However, future projects (ALICE upgrade, CBM-MVD, etc.) call for more demanding requirements especially in radiation tolerance and readout speed which cannot be satisfied by the current development utilizing 0.35μm technology. A 0.18μm CIS technology is chosen to replace the former 0.35μm counterpart. It offers thinner gate oxide and a higher resistivity epitaxial layer which can improve radiation hardness in both ionizing and non-ionizing aspects. The radiation tolerance for this technology is well validated to be adequate for the upgrade of ALICE-ITS [2]. Furthermore, the availability of quadruple well allows implementing PMOS transistors inside pixel. This possibility together with smaller feature size and more metal layers offers the opportunity to integrate more features in a pixel.

This work develops the concept of in-pixel discrimination by a prototype sensor called AROM0. Compared with the column level discrimination, in-pixel discrimination sets the analog processing within the pixel and the strong analog buffer driving the long distance column line is no longer needed. Thus, the static current consumption per pixel is reduced from ˜120 to ˜10 μA and also the readout time per row can be halved down to 100ns due to small local parasitic.

The pixel of AROM0 has a pitch of 33×22μm² mainly driven by the specification of the ALICE-ITS upgrade. It is composed of three parts: a sensing diode, a pre-amplifier and a high precision discriminator. The performance of the first two parts has been validated in former chips. Thus the development of AROM0 focuses on the discriminator design and pixel integration. Three different architectures of discriminators have been developed employing different offset compensation schemes. Each version of pixels lies in its respective matrix of 32×32 with 4 extra analog columns for sensing calibration purpose. And the array is read out in a rolling-shutter mode. Moreover, to further shorten the integration time, the double-row readout scheme is also implemented with one matrix of 16x18 including 2 analog columns.

The functionality test of AROM0 as well as sensing calibration will be performed in July 2013. Based on AROM0, a larger prototype called AROM1 featuring double-row readout and full peripheral functionalities integrated on chip (internal bias, sequence management, JTAG, etc.) will be developed.

[1] I. Valin et al, A reticle size CMOS pixel sensor dedicated to the STAR HFT, 2012 JINST 7 C01102

[2] S. Senyukov et al., Charged particle detection performances of CMOS pixel sensors produced in a 0.18 μm process with a high resistivity epitaxial layer (arXiv:1301.0515)

The vertex detector (VTX) in ILD, as one of the two detectors for ILC, has two alternative geometries. One features 5 equidistant single layers, while the other one consists of 3 double layers. In both geometries, the sensors equipped in the innermost layer give the priority to the single point resolution (≤3 μm) and the integration time (≤10 μs) dominated by beamstrahlung background. The outer layers, which are less demanding in terms of spatial resolution (3˜4 μm) and integration time (˜100 μs), are needed to consume much less power to avoid complex heavy cooling components that increase the material budget. To satisfy these requirements, a prototype sensor (MIMOSA-31) integrated with 4-bit ADCs ending the columns had been designed and is now under the test.

In this work, we proposed a new approach which implements at the pixel-level digitalization with the 3-bit charge encoding as an alternative solution for the outer layer of the VTX. Comparing to the chip-level and the column-level ADC, the pixel-level has several advantages. The digitalization of pixel output makes the readout speed to be not limited by bus capacitance, so the data readout is possible at very high bit rates. A large pixel array together with high frame rate can be achievable. Moreover, the digital output from the pixel requires no analog buffer with huge drive ability, but the digital buffers as alternatives consuming much less power. Pixel-level ADCs can also minimize the dead zone in the sensor. Although the pixel-level ADCs have many attractive features, the difficulties of design restrict its implementation.

The design of the CPS integrated with the pixel-level ADCs is in the face of the following constraints:
1. The spatial resolution requirement of the ILD-VTX limits the size of the pixel. To integrate a complete ADC into the compact pixel is a great challenge to design the circuit and layout.
2. To conform the required integration time, the high sampling speed is necessary.
3. The sensors for the outer layers of the VTX have the severe restriction on the power consumption.
4. The least significant bit (LSB) has the same value as the equivalent input noise of the sensing diode, demanding the noise of the ADCs to be minimized.
5. For CPS, as the sensing diode and the signal processing circuits are integrated on the same substrate, the interference in one pixel and the crosstalk between the neighboring pixels should not be neglected.

The first prototype, called MIMADC, which features of 35×35 μm2 pixels integrated with in-pixel 3-bit ADCs, has been designed and fabricated in a 0.18 μm 1P6M CIS process. The MIMADC prototype contains three arrays of pixels with different ADC structures. This report focuses on one matrix of 16x16 pixels employing SAR ADC associated with the conversion time of 160 ns. The power consumption of each pixel is about 140 μW with the 1.8 V supply. The pixels are read out in the row by row rolling shutter mode, and the digital output signals are transferred through 4:1 multiplexers to be serially read out by the LVDS.

The preliminary laboratory experimental results are expected to be achieved in the Autumn 2013.

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Presenter: PHAM, Thanh Hung (CNRS)

Session Classification: Poster

Track Classification: ASICs