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The sROD Module for the ATLAS Tile Calorimeter Phase-2 Upgrade Demonstrator

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TileCal is the central hadronic calorimeter of the ATLAS experiment at the Large Hadron Collider at CERN. The main upgrade of the LHC to increase the instantaneous luminosity is scheduled for 2022. The High Luminosity LHC, also called upgrade phase-2, will imply a complete redesign of the read-out electronics in TileCal. In the new read-out architecture, the front-end electronics aims to transmit full digitized information to the back-end system in the counting room. Thus, the back-end system will provide digital calibrated information with enhanced precision and granularity to the first level trigger to improve the trigger efficiencies. The demonstrator project has been envisaged to qualify this new proposed architecture. A reduced part of the detector, 1/256 of the total, will be upgraded with the new electronics during 2014 to evaluate the proposed architecture in real conditions.The sROD module is designed on a double mid-size AMC format and will operate under an AdvancedTCA framework. The module includes one Xilinx Kintex 7 and one Xilinx Virtex 7 for data receiving and processing, as well as the implementation of embedded systems. Related to optics, the sROD uses 4 Avago MiniPODs to receive data from the front-end electronics and 2 Avago MiniPODs to send control commands to the front-end and for communication with the first level trigger. A QSFP optical module is also included for expansion functionalities and a SFP module to maintain compatibility with the existing hardware.A complete description of the sROD module for the demonstrator including the main functionalities, circuit design and the control software and firmware will be presented.

Summary

The main upgrade to increase the luminosity of the Large Hadron Collider (LHC) at CERN is scheduled for 2022. It will imply a complete redesign of the readout electronics of the central hadronic calorimeter (TileCal) of the ATLAS experiment. The TileCal demonstrator project has been envisaged to verify the new proposed architecture in real conditions. Thus, a reduced part of the detector will be equiped with this new architecture during the 2014 shutdown.

The sROD demo module represents the core of the back-end electronics of the TileCal demonstrator project and it will include all the functionalities required for the new proposed read-out architecture. It should provide high speed optical links to receive data from the on-detector electronics, pipeline memories with programmable depth, reception of L1 trigger signal, transmission of processed data to DAQ system as well as preprocessor functionalities for pulse recognition, feature extraction and merging of cell sums and optical links for data transmission to the L1-Calo system.

It is designed in a double mid-size Advanced Mezzanine Card (AMC) to be operated into an Advanced Telecommunications Computing Architecture (ATCA) carrier or in a Micro Telecommunications Computing Architecture (μTCA) framework.

The sROD demo module is populated with a Xilinx Virtex 7 FPGA with 48 MultiGigaBit Transceivers (MGTs) connected to four Avago MiniPOD receiver modules to receive the data from the on-detector electronics whereas one transmitter module provides the uplink for on-detector configuration. A QSFP+ connector has been included to evaluate this radiation tolerant technology for the future system. Furthermore, a SFP+ optical connector provides back compatibility with one input link for reception of trigger information and one output link for data transmission to the present ROD module.

On the other hand, a Xilinx Kintex 7 FPGA with 24 MGTs implements the preprocessor functionalities and the interface with the L1-Calo system through one Avago MiniPOD transmitter. Flash and RAM memories

are used to implement embedded systems in both FPGAs which will include an operating system to handle the communication with external modules and with the ATCA backplane.
Power connection to the ATCA carrier is managed by the Module Management Controller mezzanine which implements the Intelligent Platform Management Interface (IPMI) communication standard for manage the hot swap power sequence with the ATCA system.
The sROD demo module includes other peripherals as two USB interfaces and one 10/100 Ethernet port. One slot for a FPGA Mezzanine Card (FMC) is available to extend the sROD demo board functionalities.

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