Contribution ID: **123** Type: **Oral**

The CMS MTF7 Trigger Board

Wednesday, September 25, 2013 12:00 PM (25 minutes)

One of the workhorses for the CMS Level-1 Muon Trigger upgrade is the Muon Trackfinder board with a Virtex-7 generation FPGA (MTF7). Optimized to handle large input bandwidth for data from the different muon sub-detectors, the board also has 1 Gigabyte of fast access memory to be used as a look-up table while assigning muon momenta. We discuss the challenges and solutions for implementing the design with all these characteristics within the uTCA form factor, as well as projected performance, and results from test-stand runs with available prototypes.

Summary

To accommodate the increase in energy and luminosity of the upgraded LHC, the CMS Endcap Muon Trigger system has to be significantly modified. To provide the best track reconstruction, the Trigger system must now import all available trigger primitives generated by Cathode Strip Chambers and by certain other subsystems, such as Resistive Plate Chambers. In addition to massive input bandwidth, this also requires significant increase in logic and memory resources.
To satisfy these requirements, a new Sector Processor unit is being designed. This unit follows the micro-TCA standard recently adopted by CMS. It consists of three modules. The Core Logic module houses the large FPGA that contains the processing logic and multi-gigabit serial links for data exchange. The Optical module contains optical receivers and transmitters; it communicates with the Core Logic module via a custom back-plane section. The Pt Lookup Table (PTLUT) module contains large amount of low-latency memory that is used to assign the final Pt to reconstructed tracks. The name of the unit –Modular Track Finder –reflects the modular approach used in the design.
The talk presents the details of the hardware and firmware design of the prototype unit based on Xilinx's Virtex-6 FPGA family, as well as results of the conducted tests. Also presented are plans for the pre-production prototype based on Virtex-7 FPGA family.

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Session Classification: Trigger