Design of a deterministic link initialization mechanism for serial LVDS interconnects

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Abstract

The Compressed Baryonic Matter (CBM) experiment at the Facility for Antiproton and Ion Research (FAIR) in Darmstadt has special requirements on the Data Acquisition Network. One of them is deterministic latency of all links from the back-end to the front-end, which enables synchronization in the whole read-out tree. Since front-end electronics (FEE) contains mixed-signal circuits for processing of detector raw data, special ASICs were developed. Double Data Rate (DDR) Low Voltage Differential Signaling (LVDS) links are used as interconnects between FEEs and readout controllers. An adapted link initialization mechanism ensures determinism for them by balancing cable lengths, adjusting phase differences and handling of environmental behavior. After re-initialization timing precision has to be on bit-clock level.

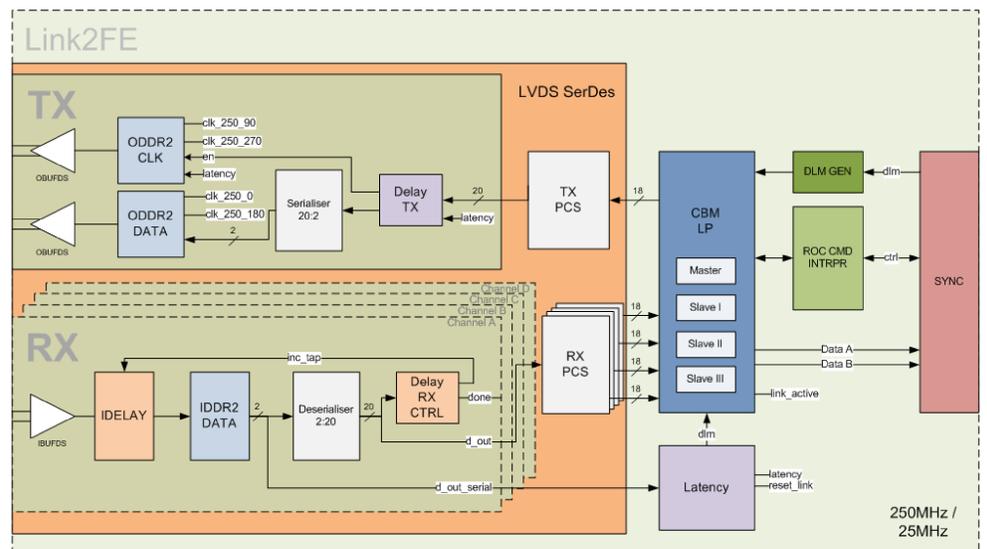## Hardware design of the readout controller (ROC)

The readout controller (ROC) is currently represented by the SysCore3, a custom-made PCB with a Spartan 6 FPGA. The design allows to aggregate detector transport messages (DTM) from up to four FEE ASICs with up to four lanes to one back-end root. A second traffic class allows to send detector control messages (DCM) through the network to get registerfile access to every device in the readout-chain. The third traffic class in the protocol provides a channel for deterministic latency messages (DLM) which can be sent independently from the connection workload to synchronize the respective sub-tree and trigger detector events.

To achieve this deterministic behavior all clocks in the sub-chain are derived from the receive clock which is recovered from this high-speed link from the back-end node to the ROC. The receive clock is fed to a jitter-cleaner IC and then used as reference clock for transmit part of the Xilinx GTP. A complex crossbar structure has been developed to route and combine the three traffic classes. An auxiliary module enables access to general purpose I/Os for detector slow control.

One link to the front-end runs with a global derived word- and bit-clock. It contains an adapted CBMnet link port with master/slave-option to support unbalanced links and the LVDS SerDes tile. A latency module measures the roundtrip time of DLM0 and delays the TX data and clock to ensure deterministic and synchronous arrival of DLMs in the FEE ASIC, which receives the bit-clock from the ROC over the HDMI connection and therefore runs completely synchronous on bit-clock level.

For the serial LVDS links, the Xilinx built-in SelectIO logic resources are used. Because ISERDES data reception with an internal clock is not possible for DDR transfer, SelectIO is configured as ILOGIC, containing IODelay block and IDDR shift register. The RX path of the SerDes starts with a differential input buffer, which changes the incoming LVDS current to a CMOS signal. The following IODelay cell moves the phase of the signal by 256 taps per clock-period. An IDDR shift register samples the double data rate stream with two inverse clocks. The adjacent deserializer merges the two bit streams to a 20 bit word and the delay-control block looks for stable comma-character detection in the 8B/10B coding and manages the IODelay cell. The outgoing data is sent to the physical coding sublayer and after decoding further to the link port which represents the media access control layer.

Equally, the transmit path of the SerDes is realized. The additional Delay-TX block delays data and the fast bit-clock by a given value and can interrupt the sending of signals by clock gating. As the counter which generates the word-clock in the FEE ASIC immediately depends on the received bit-clock, this enables the possibility to move the word-clocks in the FEE ASICs so they will run with an identical phase with accuracy below 2ns.
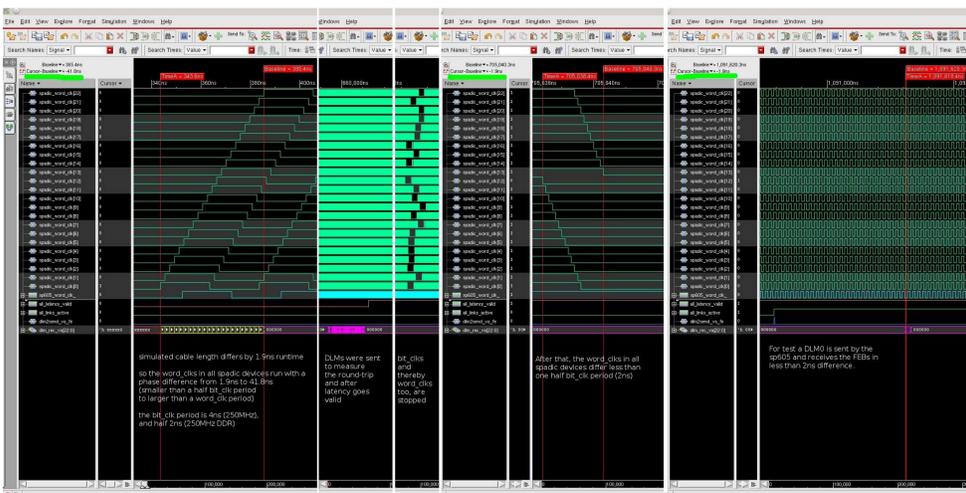

Initialization mechanism with word-clock alignment on bit-clock level

Laboratory test setup

The Syscore3 respectively the Xilinx SP605 evaluation board are connected to the Active Buffer Board (ABB) in the backend computer via optical SFP. A custom-made FPGA Mezzanine Card provides four HDMI connectors to wire the front-end boards.

There are two FEE ASIC implementations available. Both FEE ASICs were jointly developed and use the digital communication modules implemented by the computer architecture group. One was developed at the ZITI Heidelberg University at the Chair of Circuit Design (Prof. Dr. Fischer, spadic.uni-hd.de) and the other one at AGH University of Science and Technology, Krakow (Robert Szczygiel). Both were successfully tested and show the expected behavior.

Link to front-end with adapted Xilinx SelectIO logic, SerDes structure, latency module and the CBMnet link port for unbalanced links

Algorithm, Simulation and Verification

To ensure a fail-safe deterministic behavior of the link initialization, the whole hardware parts had to be built up considering a reliable structure without any buffering. Sampling the outgoing clock and data directly in the I/O cells prevents any divergent result through the implementation process.

The algorithm contains the following steps. First the incoming data stream in the ROC has to become aligned to the bit-clock with the delay structures. An eye-measurement mechanism tries to find edges and calculates the best position for sampling the data. In the second step several DLMs which consist of special 8b/10b control-symbols are sent to the FEE ASIC and the round-trip time is quantified and latency values were calculated. By gating and inverting the bit-clocks by the particular values, the word-clocks in the front-ends can be aligned to bit-clock accuracy. This can be understood as the initialization of the physical coding sublayer (PCS). In a last step the link port does some pattern comparison before data acquisition can start. The simulation was run with 24 front-end devices which all have an increasing cable length runtime of 1,9ns, which is nearly the bit-clock period. After the first two initialization steps the word-clocks phase in all FEE ASICs differs by less than 2ns.
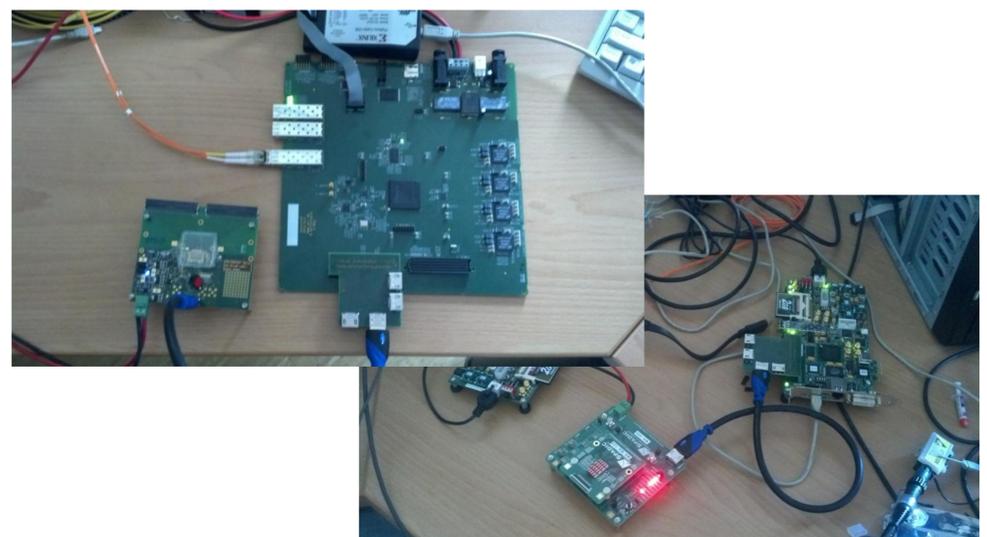

Laboratory test setups showing the Syscore3 and SP605 with the SPADIC and STSXYTER detector ASIC readout platforms with HDMI connection and optical SFP

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