Contribution ID: **125** Type: **Poster**

Design of a deterministic link initialization mechanism for serial LVDS interconnects

Wednesday, 25 September 2013 16:58 (1 minute)

The Compressed Baryonic Matter experiment at FAIR in Darmstadt has special requirements on the Data Acquisition Network. One of them is deterministic latency of all links from the back-end to the front-end, which enables synchronization in the whole read-out tree. Since front-end electronics (FEE) contains mixed-signal circuits for processing of detector raw data, special ASICs were developed. DDR LVDS links are used as interconnects between FEEs and readout controllers. An adapted link initialization mechanism ensures determinism for them by balancing cable lengths, adjusting phase differences and handling of environmental behavior. After re-initialization timing precision has to be on bit-clock level.

Summary

The front-end electronic ASICs consist of an analog part to amplify and digitize raw signals from the detector and a digital part, which contains modules as a registerfile, the CBMnet, providing the network protocol, and an LVDS serializer/deserializer. The transceivers use 8B/10B coding to achieve DC-balance. Fault tolerance is assured by using K-characters with hamming distance for special characters correction and CRC secured data with retransmission functionality. Because of restricted design space at the FEBs, an additional wire provides a clock to abstain from crystal oscillator. Data bandwidth in back-end direction can be increased by using unbalanced links, which means up to four lanes are supported for data transmission from the FEE while only one link is used for management data to the FEE.

The readout controller (ROC) design, which can aggregate data from up to four front-end ASICs to one back-end node, is currently running on a Xilinx evaluation board SP605. It will soon be replaced by a custom-made solution. The whole design and due to clock distribution all front-ends, run with the recovered clock or derived fractions from the high-speed serial link to the back-end. In addition, this receive clock is jitter-cleaned and then used for the transmit part to guarantee a source synchronous and deterministic behavior.

The front-end SerDes PHY has to delay the outgoing signals to assure that all FEE word-clocks run in phase. This adjustment allows to receive deterministic latency messages (DLM) in the front-ends synchronously. The returned data stream has to be aligned since it will not run in phase with the bit-clock due to e.g. diversifying cable lengths. Therefore, the Xilinx built-in SelectIO logic resources are used as ILogic and a delay adjust mechanism ensures that data sampling is done in the middle of the eye. An IODelay cell moves the phase of the signal by 256 taps per clock-period. The resulting measurement is used to find the transitions in the incoming serial bitstream and calculate the sampling position.

After phase alignment on bit-clock level is done, the initialization of the SerDes physical coding sublayer (PCS) is taking place. While sending specific secured character, the barrel-shifters in ROC and FEE deserializer arrange the bit sequence to the word clock.

Finally, to obtain a simultaneous arrival of a DLM in all front-ends, the clock and data signals will be delayed to assure DLM arrival after a fix time period. Measurement DLMs are sent through the links to calculate time values for every lane for inter lane adjustment. Therefore, front-end ASICs simply reflect them to the ROC and the round-trip time can be measured. After initialization, the word-clocks run in phase with less than 2ns difference. All links to the front-end ASICs provide a deterministic latency for DLMs. Latest tests showed the successful transmission and deterministic arrival of messages at the front-ends.

Primary author: SCHATRAL, Sven (University of Heidelberg)

Co-authors: Dr LEMKE, Frank (University of Heidelberg); Prof. BRUENING, Ulrich (University of Heidelberg)

Presenter: SCHATRAL, Sven (University of Heidelberg)

Session Classification: Poster