MISTRAL & ASTRAL:
Two CMOS Pixel Sensor Architectures dedicated to the Inner Tracking System of the ALICE Experiment
R&D strategy with two main streams
Christine Hu-Guo/Frédéric Morel (on behalf of PICSEL-ALICE team of IPHC-Strasbourg)
CMOS Pixel Sensors: Established Architecture

- MIMOSA26: sensor equipping EUDET BT + MIMOSA28: sensor equipping STAR-PXL
  - Rolling shutter readout
  - In-pixel amplifier + cDS → analogue output
  - Pixels organised in columns ended with discriminators
  - Discriminators followed by integrated zero suppression μ circuit logic (SUZE)
  - 2 output buffers storing the SUZE results
  - JTAG for parameters setting and control

0.35 μm twin-well technology → only NMOS can be used in pixel cells

Installation of 3 sector engineering detector on May 8, 2013
Run ended June 10, 2013

STAR Detector

MIMOSA26

MIMOSA28 (ULTIMATE)
Towards Higher Read-Out Speed and Radiation Tolerance

Next generation of experiments calls for improved sensor performances:

<table>
<thead>
<tr>
<th>Expt-System</th>
<th>$\sigma_t$</th>
<th>$\sigma_{sp}$</th>
<th>TID</th>
<th>Fluence</th>
<th>$T_{op}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>$\sim 200,\mu s$</td>
<td>$\sim 5,\mu m$</td>
<td>150 kRad</td>
<td>$3\times10^{12},n_{eq}/cm^2$</td>
<td>30 °C</td>
</tr>
<tr>
<td>ALICE-ITS</td>
<td>10-30 μs</td>
<td>$\sim 5,\mu m$</td>
<td>700 kRad</td>
<td>$10^{13},n_{eq}/cm^2$</td>
<td>30 °C</td>
</tr>
<tr>
<td>CBM-MVD</td>
<td>10-30 μs</td>
<td>$\sim 5,\mu m$</td>
<td>&lt;~10 MRad</td>
<td>&lt;~ $10^{14},n_{eq}/cm^2$</td>
<td>&lt;&lt;0 °C</td>
</tr>
<tr>
<td>ILD-VXD</td>
<td>&lt;~2 μs</td>
<td>&lt;~ 3 μm</td>
<td>O(100) kRad</td>
<td>O($10^{11},n_{eq}/cm^2$)</td>
<td>&lt;~30 °C</td>
</tr>
</tbody>
</table>

Main improvements required to comply with forthcoming experiments’ specifications:

- Aim for higher radiation tolerance
  - epitaxial layer resistivity
  - smaller feature size process
- Aim for high readout speed
  - more parallelised read-out & reduce number of pixels per column
  - new pixel array architectures
- Aim for lower power consumption

remain inside virtuous circle: spatial resolution, speed, power, flex material budget, ...

$\Rightarrow$ 0.18 μm process needed instead of currently used 0.35 μm process

- Several groups involved in the design $\Rightarrow$ see W. SNOEYS's talk in this section
General Strategy

- 2 developments in parallel at IPHC in Strasbourg in order to match the timescale: (Rolling shutter RO)
  - MIMOSA: based on the architecture of MIMOSA26 & 28: end-of-column discrimination
  - AROM (Accelerated Read-Out Mimosa): in-pixel discrimination

  for 2 final sensors
  - MISTRAL (~3x1 cm²) = **MIMOSA** Sensor for the inner **T**racker of **ALICE**
    - Mature architecture
    - Relatively low readout speed (200 ns/ 2rows)
  - ASTRAL (~3x1 cm²) = **AROM** Sensor for the inner **T**racker of **ALICE**
    - New architecture: design is being integrated in large pixel array
    - Higher speed (100 ns/ 2rows)
    - Lower power consumption
      - ~ 150 mW/cm² for inner layer, ~ 70 mW/cm² for outer layer

- Upstream of sensors:
  - Charge sensing node
  - In-pixel amplification + signal processing (cDS)
  - Discrimination

- Downstream of sensors (common part both for MISTRAL & ASTRAL):
  - Zero-suppression circuitry + Output memory buffers
  - Data transfer circuitry
  - Steering circuitry + Slow control

- Modular design for optimising R&D time
Chip development for MISTRAL & ASTRAL

MISTRAL RO Architecture
MIMOSA-22THRA
MIMOSA-22THRBB

ASTRAL RO Architecture
AROM-0
AROM-1

Diode + in-pixel amplification Optimisation
MIMOSA-32FEE
MIMOSA-32N
MIMOSA-34

MIMOSA-32 & ter

Zero Suppress Logic
SUZE02

Prior runs
SUZE

Serial read out
LVDS
PLL

~1 cm² array
~1 cm² array
~1 cm² array

August run
March 2013 ER

Previous runs
Upstream of MISTRAL Sensor

- Sensing node: $N_{\text{well}}$-$P_{\text{EPI}}$ diode, its dimensions depending on the choice of pixel pitch
  - Test results of MIMOSA34 under analyse
- In-pixel amplification and cDS: similar topology as that of MIMOSA26, PMOS can be used
  - Limited dynamic range compared to the previous process
  - Noise optimisation especially for random telegraph signal (RTS) noise

- Read out 2 rows simultaneously ➔ 2 discriminators per column (22 µm)
- Discriminator: similar schematics as that of MIMOSA26
  - Offset compensated amplifier stage
  - 200 ns per conversion

- Designed by Y. Degerli (IRFU/AIDA)

**Diagram:**
- Pixel Array
- In-pixel amplification
- cDS
- Offset compensated amplifier stage
- 200 ns per conversion
- Layout of 4 discriminators (2 columns)
Test Results of the Upstream of MISTRAL Sensor

- Lab test results:
  - Diode and in-pixel amplification optimisation
    - CCE of seed pixel optimum for:
      - Surface diode of 8-11 µm²
      - Pixel pitch of 22x33 µm
  - MISTRAL RO Architecture
    - Validation of global architecture for single and double RO
    - Discriminator are operational
    - Reduction of RTS noise by a factor of 10 to 100

- Beam test results (DESY):
  - SNR for MIMOSA-22THRA closed to 34
    - In agreement with MIMOSA-34
    - 8 µm² diode features nearly 20% higher SNR(MPV)
  - Detection efficiency ≥ 99.5% while Fake ≤ O(10⁻⁵)
  - 22×33 µm² binary pixel resolution:
    - seems to be 5–5.5 µm as expected from former studies
  - Ionisation radiation tolerance assessment under way
Upstream of ASTRAL sensor

- Sensing node & in-pixel pre-amplification as same as MISTRAL sensors
- In-pixel discrimination
  - 2 promising topologies: still optimising
  - AROM0 with 6 sub-matrices tested at laboratory
    - Total noise ~28 e-, in-pixel discriminator a bit noisy
- The first prototype AROM0 has validated the full functionality of the two architectures and the feasibility of the project
- Further development will focus on large sensor integration along with power consumption and noise reduction → AROM1 submitted in August
Zero Suppression Logic (SUZE02)

- AD conversion (pixel-level or column-level) outputs are connected to inputs of SUZE

![Diagram showing hit clusters](image)

- More efficient encoding than the previous one (SUZE01) implemented in ULTIMATE sensor
  - It searches windows of 4x5 pixels which contain hit cluster information
  - Results are stored in 4 SRAM blocks allowing either continuous or triggered readout
  - Sparsified data are multiplexed onto a serial LVDS output
    - Data rate: 320 Mbit/s per channel (1 or 2 channels in SUZE02)
    - Compression factor: 1 to 4 order of magnitudes

- Preliminary test results: SUZE02 is functional for main configurations @ full speed

- For MISTRAL / ASTRAL a data rate of 500 Mbit/s – 1 Gbit/s is required
  - INFN Torino is working on data transmission up to 2 Gbit/s
Conclusions

- 2 sensors are developed at IPHC for ALICE ITS upgrade

- MISTRAL upstream and downstream architectures validation confirmed
  - 22x33 µm² pixel binary resolution ~5-5.5 µm
  - Detection efficiency > 99.95% for fake hit rate ≤ O(10⁻⁵)
  - Readout speed: 200 ns/2 rows
  - Integration time: ≤ 30 µs
  - Data rate of ~0.5-1 Gbit/s per chip after zero suppression logic
  - Power consumption <350 mW/cm²

- ASTRAL architecture validation on going
  - ASTRAL pixel front-end amplification (same as MISTRAL part) validation confirmed
  - Downstream of ASTRAL (shares the same logic with MISTRAL) validation confirmed
  - Feasibility of the In-pixel discrimination validated
    - Fine optimisation on going
  - ASTRAL performs 2 x higher readout speed and lower power consumption than MISTRAL
    - Integration time: <20 µs
    - Power consumption ~150 mW/cm² for inner layers & < 70 mW/cm² for outer layers
Next steps:

- Q4/13: AROM-1b
  - AROM1 with optimised pixel in term of noise and power consumption
- Q1/14: FSBB-0
  - Full chain prototype based on FSBB-M approach
  - Utilisation of existing block with minor modification
- Q3/Q4/14: FSBB-A or M
  - Depends on AROM1 and FSBB-0 test results
- Q3/Q4/15: Final prototype ASTRAL or MISTRAL

Thanks for your attention