Contribution ID: **53** Type: **Oral**

Design of a Hardware Track Finder (Fast Tracker) for the ATLAS Trigger

Wednesday, 25 September 2013 15:15 (25 minutes)

The ATLAS Fast TracKer is a custom electronics system that will operate at the full Level-1 accept rate, 100 kHz, to provide high quality tracks as input to the Level-2 trigger. The event reconstruction is performed in hardware, thanks to the massive parallelism of associative memories (AM) and FPGAs. We present the advantages for the physics goals of the ATLAS experiment and the recent results on the design, technological advancements and testing of some of the core components used in the processor.

Summary

The existing three level ATLAS trigger system is deployed to reduce the event rate from the bunch crossing rate of 40 MHz to ˜400 Hz for permanent storage at the LHC design luminosity of 10ˆ34 cmˆ-2 sˆ-1. When the LHC reaches beyond the design luminosity, the load on the Level-2 trigger system will significantly increase due to both the need for more sophisticated algorithms to suppress background and the larger event sizes. The Fast TracKer (FTK) will provide high quality tracks at the beginning of the Level-2 trigger, exploiting the massive parallelism of associative memories (AM) and FPGAs. We report innovative developments included in the detailed design of the system just completed.
An important characteristic of the system is its significant data reduction capability by clustering the incoming hits from the pixel sensors. This functionality will be implemented on a mezzanine board with two Spartan 6 FPGAs that process incoming data at full speed with small latency. The clustering algorithm is executed by multiple sliding window algorithms operating in parallel which achieve nearly linear processing time with respect to the number of readout hits.
The core of the system is composed of the associative memory board (AMBSLP) and a rear transition module (RTM) that have a very high computational power and I/O bandwidth. The AMBSLP is a 9U VME motherboard and contains four large mezzanines, the LAMBSLPs, where 64 AM chips are located. It has to support very large data traffic: a huge number of hits must be distributed at high rate with very large fan-out to all AM chips and a huge number of roads must be collected and sent to the RTM. A network of high speed serial links characterizes the bus distribution on the AMBSLP: 12 input serial links provide a 24Gb/s input bandwidth to the LAMBSLPs, and 16 output serial links are received from the LAMBSLPs for a total of 32Gb/s output bandwidth.

The RTM card for the FTK has to perform very intensive tasks: providing the input for the AMBSLP and doing a preliminary determination of the goodness of fit for the track candidates. The RTM needs access to the VME bus for configuration, setup and monitoring, something that is not normally possible for rear modules. This feature has been achieved using the J2 feed-through pins to communicate with the front module, extending the local data and address VME buses. Finally we will report on the studies to optimize the construction of the pattern bank used in the system. In order to make maximal use of variable resolution pattern recognition, which is achieved with ternary AM cells (storing 0, 1 or “don’t care”values) included in the new AM chips. We have performed extensive simulation studies searching for the best trade-off to maintain good efficiency and high rejection of random coincidences. We have found that even using a limited number of ternary cells, we can make a pattern bank that performs well in the harsh conditions expected for the LHC after the Phase-I luminosity upgrade.

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Session Classification: Trigger

Track Classification: Trigger