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Pixel chip architecture optimization based on a simplified statistical and analytical model

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The technical challenges related to increased collision rates of the LHC will significantly affect detector electronics design. Efficient hit processing is achieved in pixel detectors by grouping pixel chips in regions, which share buffering logic. We present an approach to determine an optimized sharing strategy between pixels, depending on the shape of clustered hits in the detector. Simple statistical models of such shapes have been developed with respect to the position in detector where hits take place. Then the buffering performance of different pixel region configurations has been compared, showing significant improvement from architectures that do not feature pixel grouping.

Summary

New hybrid pixel detectors supporting hit rates up to 2GHz/cm2 will be developed for future High Energy Physics experiments. In this scenario complex on-chip digital logic at the lowest possible power consumption will be designed requiring special techniques to develop a system working reliably.
We describe an approach to determine an optimized logic sharing in pixel chip arrays, depending on simplified shapes of clustered hits in a detector. A cluster is made of a certain number of hit pixels and its shape depends on a quantity of factors, e.g. position in the detector, pixel size, sensor thickness, discriminator threshold. In order to correctly process clustered hits each hit pixel should associate hit information to the same cluster without errors. This can be accomplished efficiently by grouping pixels in so-called pixel regions so that the buffering logic is shared between them.
The optimal pixel region configuration to adopt is correlated to cluster shape. We have estimated the buffering performance of a set of pixel region configurations, with statistical assumptions on cluster shapes related to position in the detector. According to simulation data clustered hits shapes at the center of the barrel are symmetrical, while the ones at the edge are elongated along z direction. According to this we have respectively developed two simplified cluster shape models. The former have been modeled as square envelopes sized 3x3 pixels, where hit pixels inside it identify a cluster. For the latter one-dimensional shapes with variable z have been assumed; the more hit pixels constitute the cluster, the more elongated its shape is along z. Arbitrary statistical distributions have been constructed in order to provide information on the probability of each cluster model to be composed of a given number of hit pixels. From these assumptions we have calculated the required number of buffer locations for each pixel region configuration. We have quantified the bit depth of the hit information stored inside the shared buffer, as it depends on pixel region size. The study is currently being validated using detailed cluster footprint data from physics simulation in place of the simplified cluster model. Moreover, a suitable SystemVerilog verification environment is currently being developed to model the proposed pixel chip architecture in more detail. This verification environment will then be used for further architecture optimizations and will finally be used for extensive design verification.

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