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Characterization of the CBC2 readout ASIC for the CMS strip-tracker high-luminosity upgrade

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The CMS Binary Chip 2 (CBC2) is a full-scale prototype ASIC developed for the front-end readout of the high-luminosity upgrade of the CMS silicon strip Tracker. The 254-channel, 130nm CMOS ASIC is designed for the binary readout of double-layer modules, and features cluster-width discrimination and coincidence logic for detecting high-PT track candidates. The chip was manufactured in January 2013 and has since been bump-bonded to a dual-chip hybrid and extensively tested. The CBC2 is fully functional and working to specification: we present the result of electrical characterization of the chip, including gain, noise, threshold scan and power consumption, together with the performance of the stub finding logic. Finally we will outline the plan for future developments towards the production version.

Summary

The CMS Binary Chip 2 (CBC2) is the latest version of the silicon strip readout ASIC being developed for the High-luminosity upgrade of CMS (Phase II). The CBC2 is a 254-channel, bump-bonded full-scale prototype which includes the functionality necessary to identify hits associated with high-PT tracks ("stubs"). Designed in 130nm CMOS, CBC2 is a binary readout ASIC building on the successful first CBC prototype: each channel comprises of pre-amplifier, shaper and comparator; the L1-triggered data are stored in a 256-deep digital pipeline and serially read-out un-sparsified. Unlike its predecessor, the CBC2 is designed to instrument double-layer modules and is therefore a substantially revised chip that includes major new features, such as the adoption of a bump-bonded layout, coincidence logic for stub finding and cluster-width discrimination, and twice the number of channels than its predecessor. The input channels are divided between top and bottom sensors allowing the chip to look for coincidences between the two layers: the position of these stubs can be read out serially for test purposes. A fast-OR test pad signals the presence of either stubs or input activity allowing self-triggering operation.
The CBC2 was delivered in January 2013: a manufacturing split provided wafers with metallization for either wire-bonding or bump-bonding. The wire-bonded prototypes were initially tested for a rapid performance evaluation: the CBC2 was characterized and found to be working well. The C4-processed chips were then probe tested on the wafer before being diced and mounted on a dual-chip hybrid. Together with the yield figures resulting from the wafer-probing of ˜800 chips, we present the results of full electrical characterization, including gain, noise, linearity, threshold scans and power consumption. We also present a measurement of the performance of the on-chip LDO and DC-DC switched capacitor converter.
The dual-CBC2 module obtained by bonding microstrip sensors to the hybrid is an important milestone towards the 2S ("strip-strip") module being developed for the outer Tracker. It allows for the data links between adjacent CBC2s to be exercised and, by incorporating only known-good dice with a high number of bump-bonded pads, these modules will provide a good indication of the assembly yield before a more extensive production is launched. Importantly, they also offer a unique opportunity to evaluate the performance and efficiency of the PT -cut concept in a realistic scenario such as a test beam.

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