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## The Front-End Hybrid for the ATLAS HL-LHC Silicon Strip Tracker

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For the HL-LHC, ATLAS will install a new all-silicon tracking system. The strip part will comprise five barrel layers and seven end caps on each side. The detectors will be connected to highly-integrated low-mass front-end electronic hybrids with custom-made ASICs in 130nm technology. The hybrids are flexible PCB four-layer copper polyimide constructions. They are designed and populated at the Universities involved, while the flex PCB is produced in industry. This presentation will describe the evolution of hybrid designs for the barrel and endcap, discuss their electrical performance, and present results from reading out prototype modules made with the hybrids.

### Summary

The Large-Hadron-Collider (LHC) will undergo a major upgrade to the High Luminosity LHC (HL-LHC), which is designed to deliver of order five times the LHC nominal instantaneous luminosity along with luminosity leveling. The final goal is to extend the data set to 3000 fb<sup>-1</sup> by around 2030.

The challenge of coping with HL-LHC instantaneous and integrated luminosity, along with the associated radiation levels, requires major changes to the ATLAS detector. The designs are developing rapidly for an all-new inner-tracker, significant upgrades in the calorimeter and muon systems, as well as improved triggers and data acquisition.

This submission is connected to the HL-LHC upgrade of the ATLAS Inner Tracker (ITK), which consists of replacing the entire current Inner Detector (silicon pixels, silicon strips and transition radiation tracker) with a completely new silicon-only system. This new ITK will be made from several pixel and strip layers, and both detectors and read-out electronics have to be designed to withstand the extreme radiation environment in close proximity to the HL-LHC interaction point. This broadly speaking means an order of magnitude higher radiation hardness than the existing ID. At the same time, the radiation length should be kept to the level of the present system or below in order to conserve the physics performance of ATLAS. In the current planning, the pixel system involves four barrel layers and six disks on each side for a total pixel area of 7m<sup>2</sup> and 400 million channels. The strip system will contain five barrel layers and seven end-cap disks, covering 200m<sup>2</sup> of silicon and 45 million channels.

This presentation concentrates on the front-end electronic hybrids for the silicon strip tracking system. In order to minimize the mass, the hybrids, realized as flexible PCB with a four-layer copper polyimide buildup, are characterized by a very high integration density. The development of the hybrid is an evolutionary process closely linked to the development of the read-out CMOS ASIC (the ATLAS Binary Chip or ABC), and the strip detectors to be read out. The present hybrids employ the 250nm version of the ASIC, derived from the ABC (though in DMIL technology) running in today's ATLAS strip tracker. A 130nm version has been designed and will be produced during this year, with the matching hybrids also currently under design. In our presentation, will be describe the detailed design of the various hybrids for barrel and endcap detectors. The endcap region has added complications due to its wedge-shaped geometry, requiring around ten different hybrid designs with a different layout and varying numbers of ASICs. We will show our experience with producing the PCBs in industry and the process of populating them with active components in-house. We will also show the electrical performance with a number of powering, grounding, shielding and read-out options. In addition, we will discuss lessons learned along the way, and present results from testing prototype

silicon detector modules made by connecting several designs of ATLAS HL-LHC prototype detectors with our hybrids.

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