The Versatile Link

System-level Component Tests

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Outline

- Introduction
- Versatile Link architectures
- System-level testing
- Optical link budget
- Typical applications
- Summary
Versatile Link project

- Optical layer linking front-end to back-end up to 150 m distant.
- Bi-directional @ 5 Gbps
- Two Point-to-point solutions
  - 850 nm Multimode
  - 1310 nm Single-mode
- Front-end pluggable module
- Rad-hard front-end

- Joint Project Proposal submitted to ATLAS & CMS upgrade steering groups in 2007 and endorsed in 2008
- Project Kick-off: April 2008
  - Phase I: Proof of Concept (18mo)
  - Phase II: Feasibility Study (18mo)
  - (Consolidation)
  - Phase III: Pre-production readiness (18mo)
  - Production: Phase I Upgrade: ATLAS, CMS, LHCb (calorimeter-grade components)

Jan Troska et al. “Versatile Transceiver and Transmitter Production Status” (poster session)
Supported architectures

- Single-channel readout, or control links
- Single-mode and multi-mode variants exist
- Multi-channel receiver and transmitter arrays increase density at the back-end
- Typically multi-mode, however, some single-mode solutions exist too
- Asymmetric bandwidth needs (up>>down)
- Typically complemented by single-channel control links
- Multi-mode solution
System-level testing

- **Component testing**
  - Verify compliance w.r.t. their specifications
  - Carried out extensively during component selection and prototyping

- **System-level testing**
  - Verify compatibility of the components in the system
  - Allows to measure system performance vs. component parameters (e.g. fibre type/length)

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Rainer Schwemmer et al. “Evaluation of 400m, 5Gbit Versatile Link lengths over OM3 and OM4 fibres for the LHCb upgrade” (poster session)
Optical link budget

- Allows you to calculate the margin in your system
- Accounts for the statistical spread of the component specifications
- Includes losses and various penalties
  - Fibre attenuation
  - Insertion loss (connectors, splices)
  - Radiation damage (front-end, passive and active components)
  - Link penalty
- Considers raw link performance
  - Encoding and/or equalization can also contribute to the link margin
- Target is to keep 3dB margin (conservative)
  - Ageing and unforeseen effects
  - Don’t forget high-reliability requirements we have in our systems
Optical link budget
# Link specifications and margins

<table>
<thead>
<tr>
<th></th>
<th>MM_VTx_Rx</th>
<th>MM_Tx_VRx</th>
<th>SM_VTx_Rx</th>
<th>SM_Tx_VRx</th>
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<tbody>
<tr>
<td>Min. Tx OMA</td>
<td>-5.2 dBm</td>
<td>-3.2 dBm</td>
<td>-5.2 dBm</td>
<td>-5.2 dBm</td>
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<tr>
<td>Max Rx sensitivity</td>
<td>-11.1 dBm</td>
<td>-13.1 dBm</td>
<td>-12.6 dBm</td>
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<td>Power budget</td>
<td>5.9 dB</td>
<td>9.9 dB</td>
<td>7.4 dB</td>
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<tr>
<td>Fiber attenuation</td>
<td>0.6 dB</td>
<td>0.6 dB</td>
<td>0.1 dB</td>
<td>0.1 dB</td>
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<tr>
<td>Insertion loss</td>
<td>1.5 dB</td>
<td>1.5 dB</td>
<td>2.0 dB</td>
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<tr>
<td>Link penalties</td>
<td>1.0 dB</td>
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<td>1.5 dB</td>
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<tr>
<td>VTx rad. penalty</td>
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<td>-</td>
<td>0 dB</td>
<td>-</td>
</tr>
<tr>
<td>VRx rad. penalty</td>
<td>-</td>
<td>2.5 dB</td>
<td>-</td>
<td>2.5 dB</td>
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<tr>
<td>Fiber rad. penalty</td>
<td>0.1 dB</td>
<td>0.1 dB</td>
<td>0 dB</td>
<td>0 dB</td>
</tr>
<tr>
<td>Margin¹</td>
<td>2.7 dB</td>
<td>4.2 dB</td>
<td>3.8 dB</td>
<td>4.1 dB</td>
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</tbody>
</table>
Multi-mode application: uplink

![Diagram of Versatile Link system](image)

- Clock Gen.
- BERT
- VTRx on MCB
- VOA
- PC
- Scope
- OPM
- 400m OM4
- 40MHz
- Mini POD
- RX
- FPGA
- AMC40

**Graphs:**
- VTRx to MiniPOD, PRBS-7
- VTRx 451 (GBLD + MM VCSEL), short cable
- VTRx 451 (GBLD + MM VCSEL), 400m OM4

**Text:**
- The Versatile Link: System-level Component Tests

TWEPP 2013, 23-27 September
Multi-mode application: lab setup
Multi-mode application: downlink
Applications summary

The Versatile Link: System-level Component Tests

Versatile Link

On-detector - Radiation zone

Off-detector - Radiation-free zone

VTRx

VTTx

GBLD
Laser Diode
PIN+GBTIA
ROSA

4.8 Gb/s

50-150 m

TOSA

PCB

edge-connector
I2C

Array Tx

Array Rx

SFP+

Array Rx

Heat sink

Module

21mm

21.7mm
Summary

- Versatile Link components are available for interested users to carry out similar tests
  - Single-, and multi-mode VTRx and multi-mode VTTx
  - We are happy to assist you
- Different link architectures are supported
  - VTRx to SFP+
  - VTRx/VTTx to Array Tx/Rx/TRx
  - VTRx to QSFP+ (to be investigated)
- Compatible back-end components have been identified and are recommended for interested users
- System-level testing allows users to optimize their system and to evaluate the performance