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Next generation Associative Memory devices for the FTK tracking processor of the ATLAS experiment

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The AMchip is a VLSI device that implements the associative memory function, a special content addressable memory specifically designed for high energy physics applications and first used in the CDF experiment at Tevatron. The 4th generation of AMchip has been developed for the core pattern recognition stage of the Fast TracKer (FTK) processor: a hardware processor for online reconstruction of particle trajectories at the ATLAS experiment at LHC. We present the architecture, design considerations, power consumption and performance measurements of the 4th generation of AMchip. We present also the design innovations toward the 5th generation and the first prototype results.

Summary

The AMchip ASIC is a VLSI device implementing a special kind of Content Addressable Memory (CAM) called associative memory (AM).

The main difference between a standard CAM and an AM is the possibility of the latter to identify correlations in data, while CAMs recognize single words. Precalculated coincidences of several data
words received at different times are found by the AM in scrambled data streams. The correlations to be found can be also partial.

This function is especially useful for trajectory reconstruction in high energy physics applications. The data coming from different layers of the tracking detector is processed in parallel by the AM for pattern recognition and the ability to perform partial matching copes with the detector inefficiency. This approach was first used with great success by the CDF experiment at Tevatron with the SVT tracking
processor where the pattern recognition stage was performed by an AM bank.

Since the first AM device of the late 90s several generations of AM chips has been developed. Here we present the 4th generation: AMchip04. This latest version has been specifically developed as a prototype for the FTK tracking processor for the ATLAS experiment at LHC. FTK is a second generation of tracking processor similar to SVT. The core pattern recognition function of FTK is performed by AM chips like in SVT.

The AMchip04 represents a major step in terms of design and technology with respect to the AMchip03 used in SVT. It has been developed in TSMC 65 nm CMOS technology using a mixed standard cells / full custom approach and it can store up to 8k patterns in a 14mm2 die. The core associative memory block has been developed in full custom for maximum optimization in terms of power consumption and silicon area using several design optimizations. The control, I/O and computation logic is written in VHDL and synthesized in standard cells for faster development, re-usability and testability. For the first time it has been introduced the possibility to store ternary values (0, 1, X: don't care) in the AM bank. They will allow pattern recognition with variable resolution described in [doi:10.1109/ANIMMA.2011.6172856]. The chip is designed to run with a working frequency equal to
100 MHz.

The results of the tests performed on a batch of 100 AMchip04 dies is presented. Power consumption at different core clock rates is measured in detail with an estimation of the power consumption of each component inside the chip (I/O, clock distribution, standard cell logic, full custom AM block). Consumption for a chip with a bigger pattern bank (64k) is projected to be under 1.9 W at 100 MHz. Yield is estimated.

Further development is needed toward a 5th generation of AM chip to meet the requirements to be installed in FTK experiment. We present the design and simulation results of an intermediate R&D mini@sic with 5th generation features: serialized I/O and lower consumption associative memory block.

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