Upgraded Readout and Digitizing System for the ATLAS Tile Calorimeter Demonstrator

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on behalf of the ATLAS Tile Calorimeter System

Overview

1. Motivation
2. The ATLAS Tile Calorimeter
3. The present system
4. The future system
5. The Demonstrator readout
    1. 3-in-1 front-end board
    2. MainBoard
    3. DaughterBoard
6. Test setup
7. Conclusion / Outlook

1. Motivation

- LHC upgrade program aims at 5-10 fold luminosity increase
  → more radiation → better radiation tolerance required
- Aging electronics → originally planned for 10 years of operation
- Higher event rates require more efficient trigger algorithms

Complete redesign of TileCal electronics for upgrade in 2022

- Currently digitized data stored on the detector
  → Readout only for triggered events

- Redesigned electronics should transfer all digitized data off the detector
  → Fully digital Trigger with higher selectivity and finer granularity possible

Implementing the new concept in a Demonstrator in 2014
→ Discover and solve issues as early as possible

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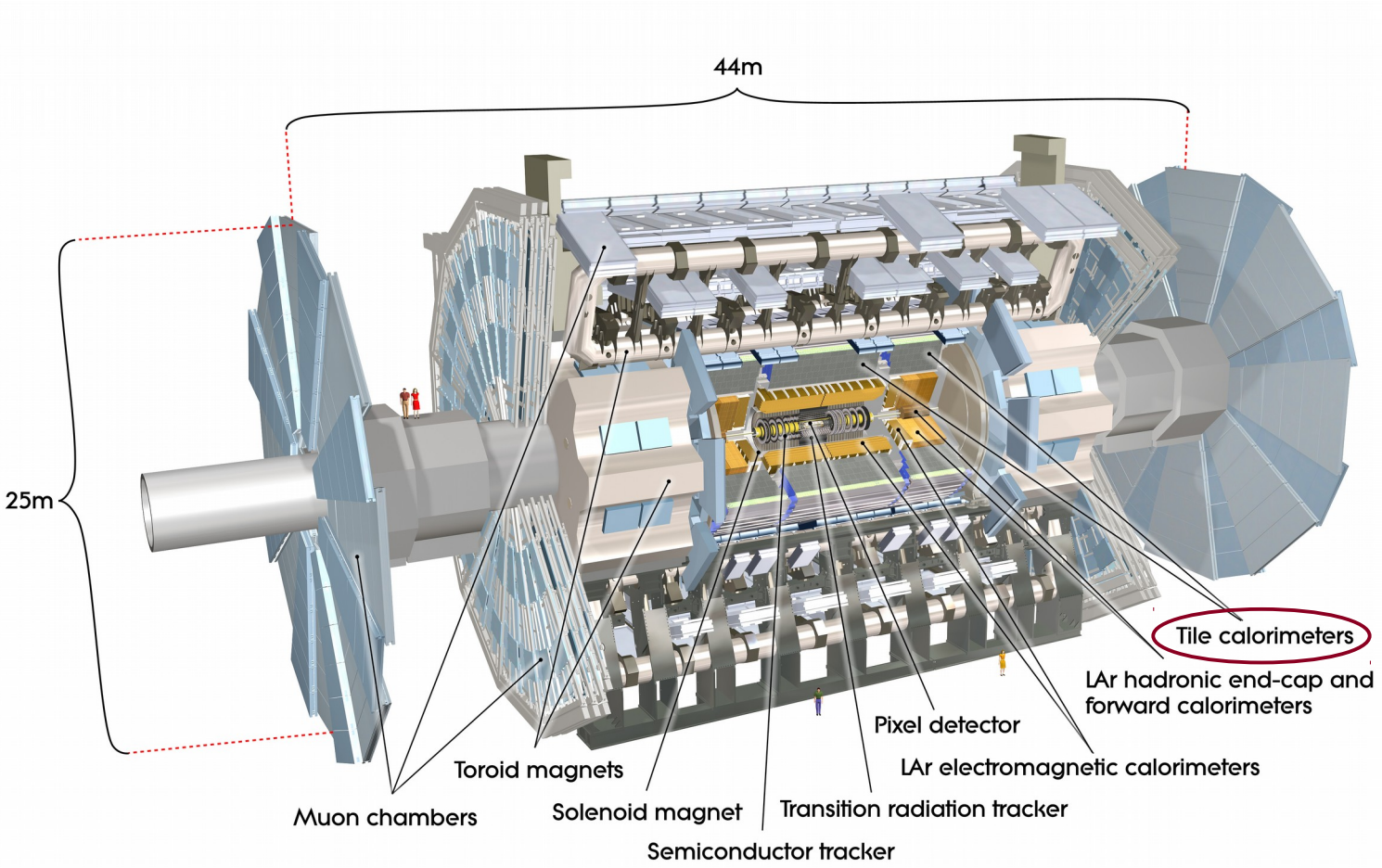
2. The ATLAS Tile Calorimeter



Source: ATLAS

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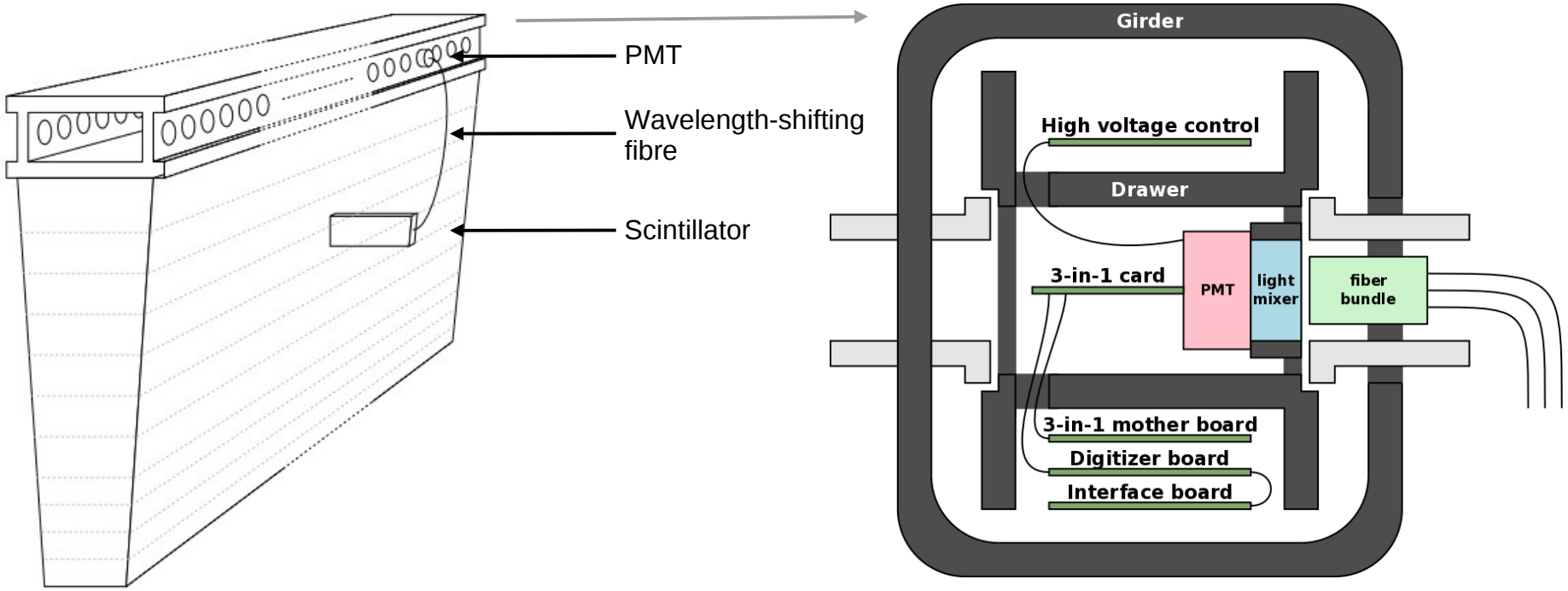
2. The ATLAS Tile Calorimeter

- The Tile Calorimeter (TileCal) is a hadron calorimeter
- Measures the energy and direction of hadrons and jets
- Divided in 64 wedges in azimuth
- Consists of steel plates with scintillator material in between
- Front-end electronics and PMTs located in “drawers” along the outer surface



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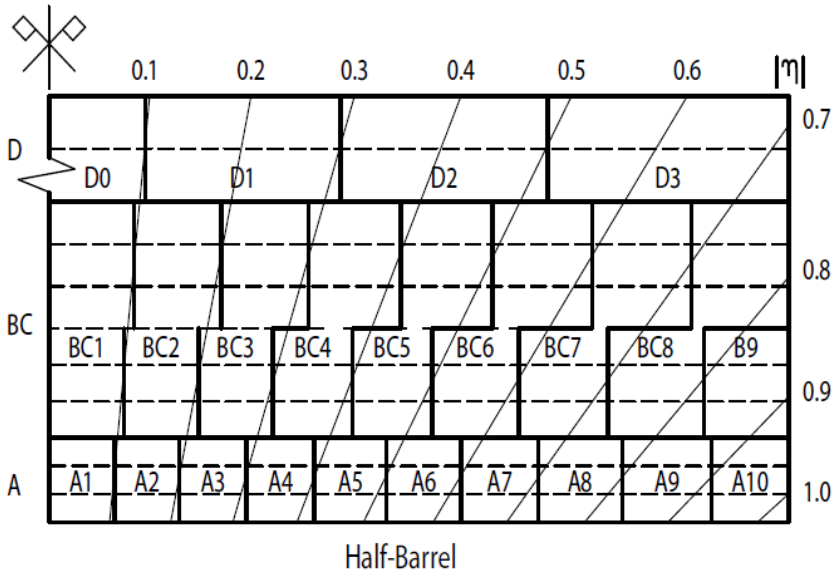
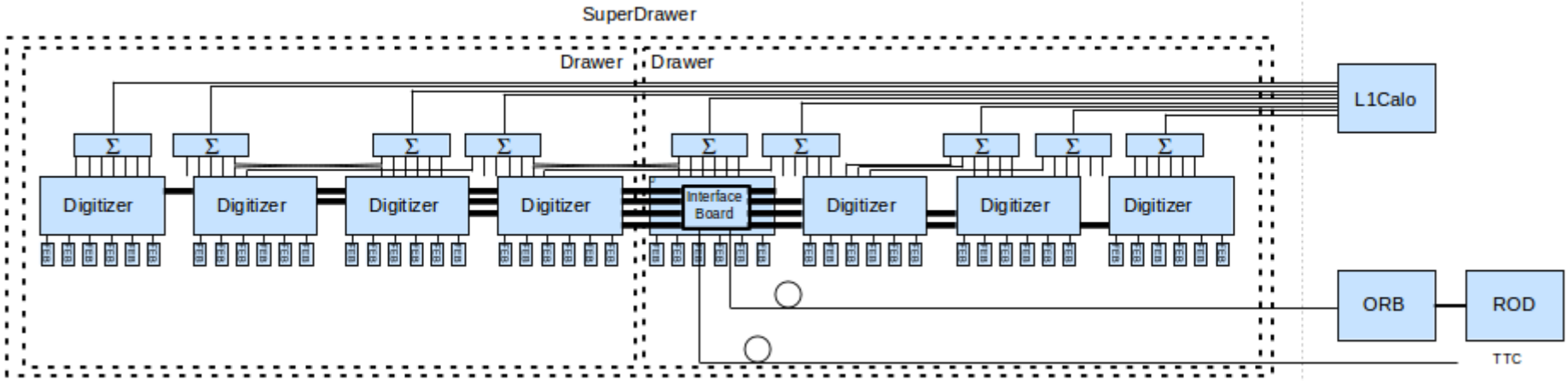
2. The ATLAS Tile Calorimeter

- **Key component for the first-level trigger**
- Analog trigger sum formed on-detector (Σ)
  → organized as tower sums
- 16 bit resolution read out achieved by two gain ranges
- Digitized data stored on-detector in pipeline and de-randomizer memories





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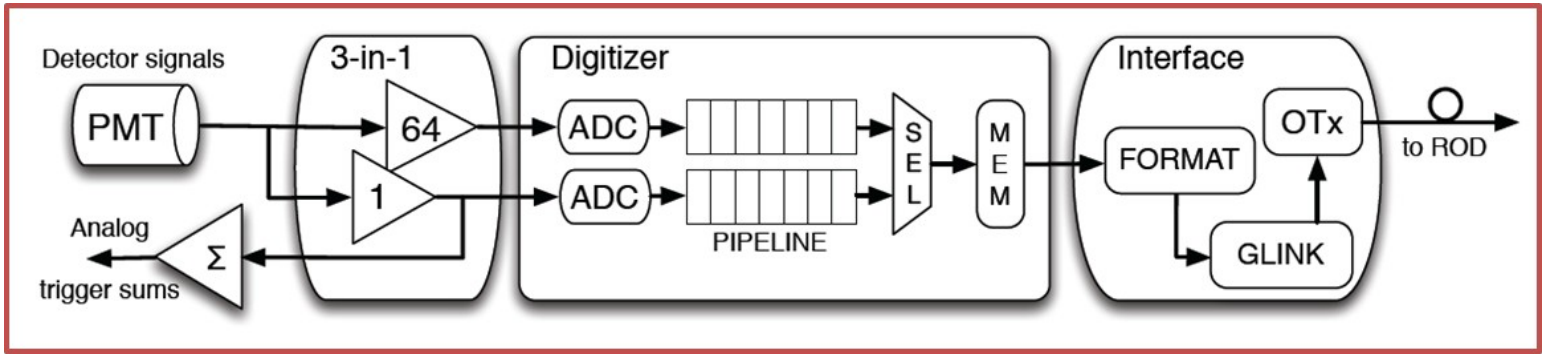
3. The present system

- **3-in-1 Front-end boards:**
  - Shaping of PMT signals for digitization with LHC clock
  - Integration of PMT signals and production of Charge injection pulses for calibration
- **3-in-1 mainboard:**
  - Programming and control of the 3-in-1 board
- **Digitizer board:**
  - Digitization into pipeline and de-randomizer memories
- **Interface board:**
  - Timing Trigger and Control (TTC), fan-out and readout merging links to off-detector area (USA-15)



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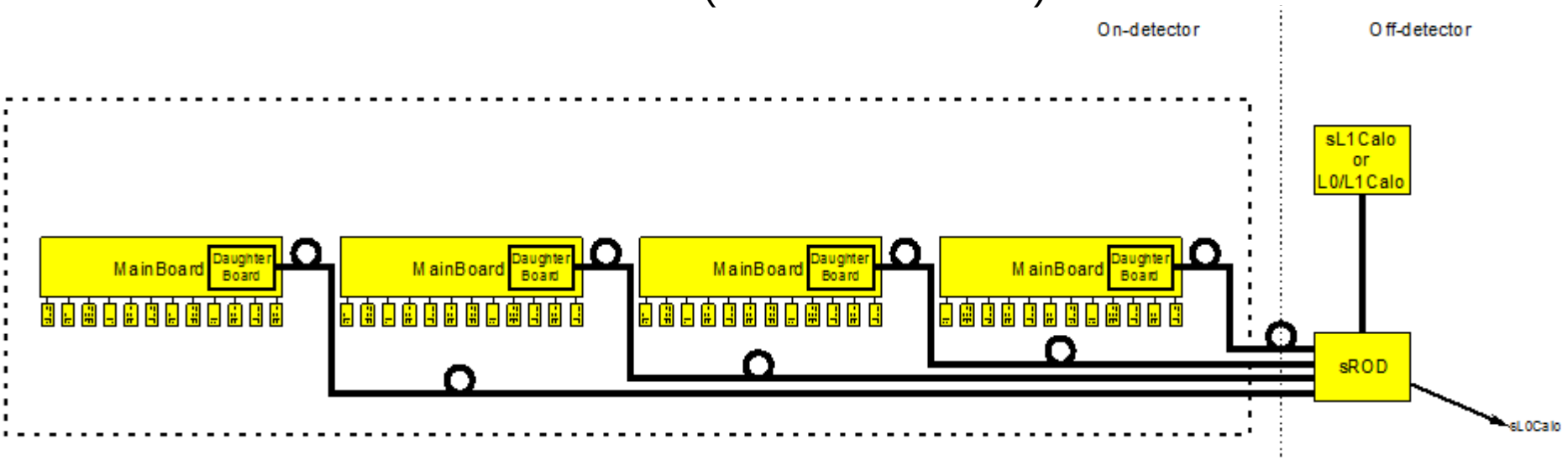
4. The future system

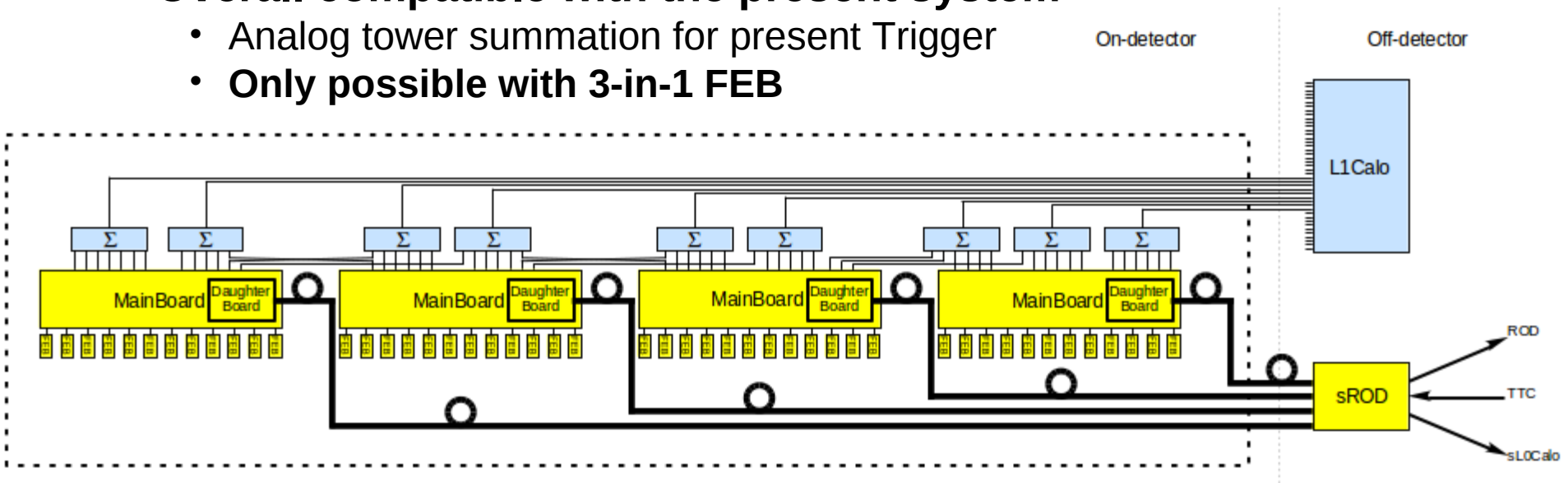
- **Readout of all data to the upgraded Read Out Driver (sROD)**
- Pipeline and de-randomizers in USA-15
- High speed serial data communication with up to 11.25 Gbps
- **New modularity → MiniDrawers**
- Local voltage regulation, error monitoring and DCS integration
- Remote programmability and configuration of all on-detector boards
- **Three different alternative FEBs under development**
  - 3-in-1 (University of Chicago)
  - QIE (Argonne National Laboratory)
  - FATALIC Front-end ASIC (Clermont-Ferrand)



5. The Demonstrator readout

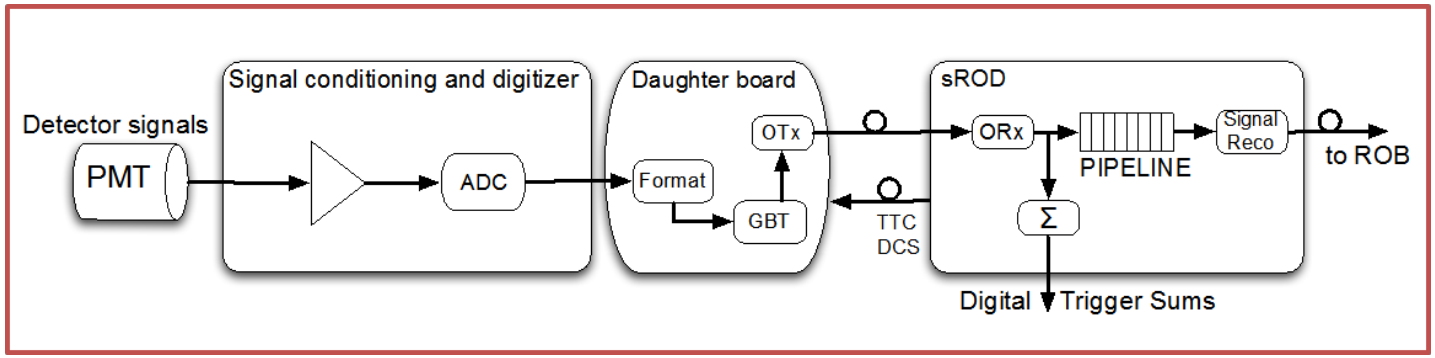
- **As close as possible to a final system** but
  - Capable of receiving commands from the TTC data-stream decoded by the sROD
  - Compatible with the current DCS system
  - Compatible with the current test procedures
  - Transmitting standard output data to a standard ROD via sROD

- **Overall compatible with the present system**
  - Analog tower summation for present Trigger
  - **Only possible with 3-in-1 FEB**



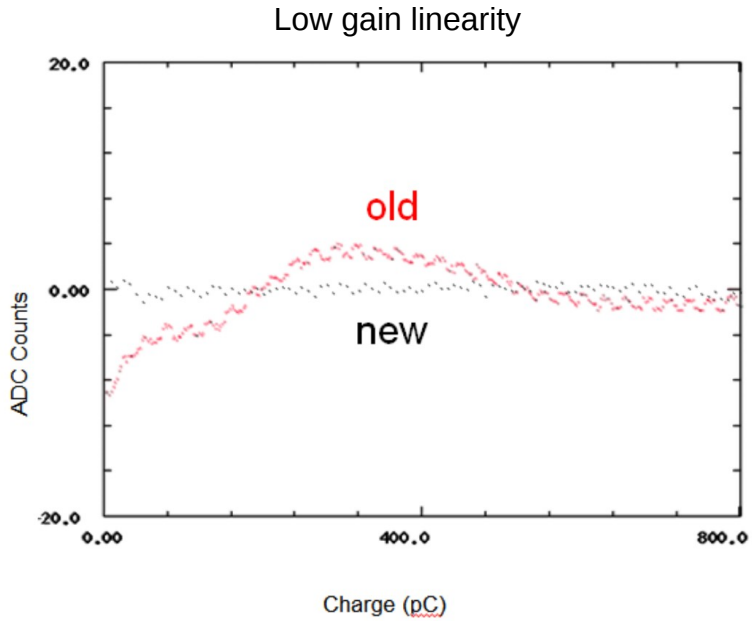
5. The Demonstrator readout

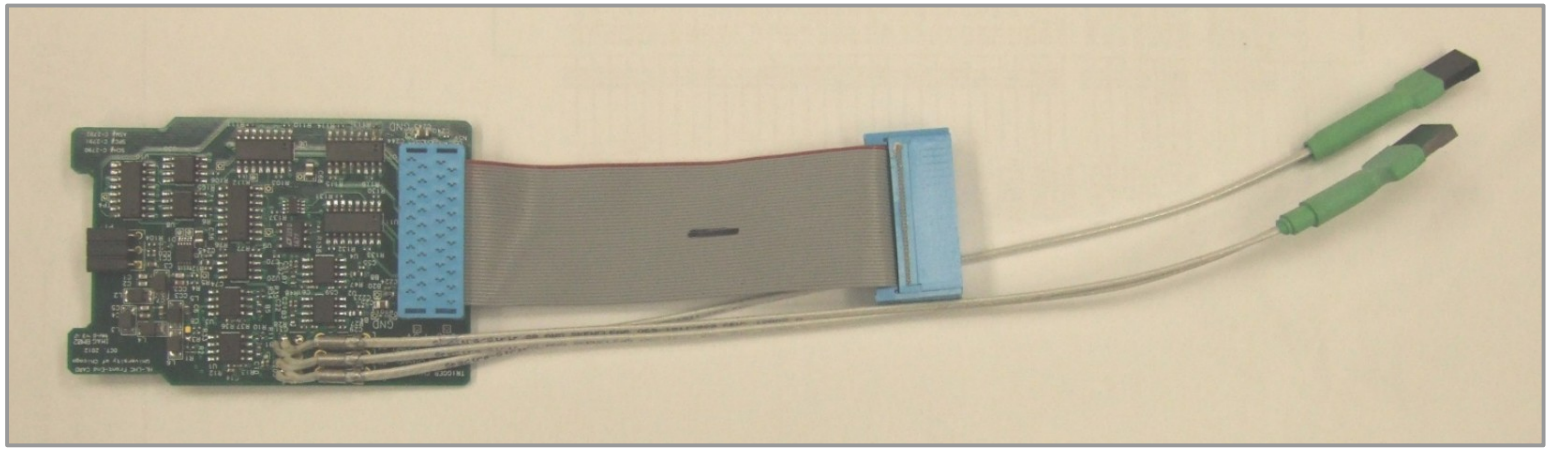
- **Redesigned 3-in-1 Front-end boards:**
  - Shaping of PMT signals for digitization with LHC clock
  - Integration of PMT signals and production of Charge injection pulses for calibration
- **Mainboard:**
  - Programming and control of the 3-in-1 board
  - Digitization of PMT signals
- **DaughterBoard:**
  - Monitoring and controlling of the front-end electronics
  - LHC clock recovery and distribution
  - Data transmission to and from off-detector electronics



5.1. 3-in-1 front-end board

- **Front-End-Board (3-in-1):**
  - Only analog components for integration and shaping used
  - Digital components moved to the MainBoard
  - **Improved noise performance**
  - **Improved linearity**
  - **Shortened shaping time**
  - **Passed radiation testing**
  - Final iteration manufactured

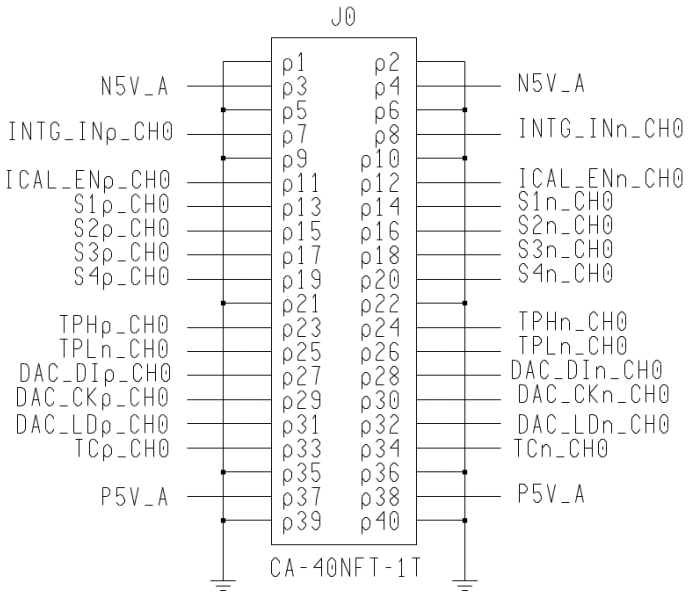




5.1. 3-in-1 front-end board

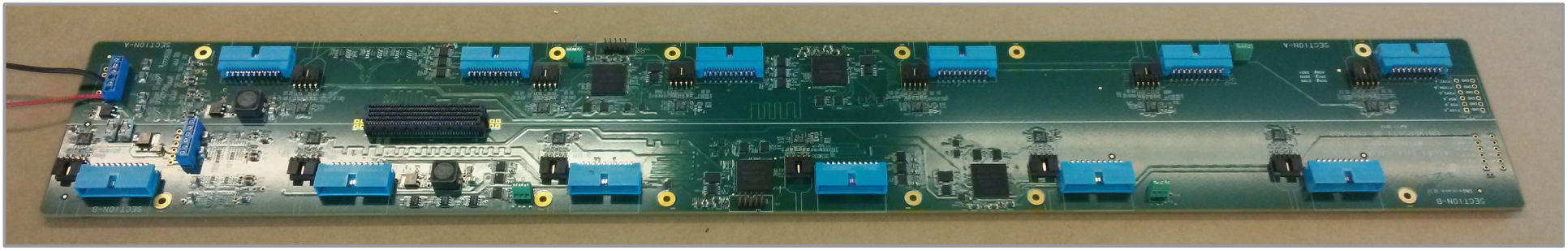
- **Connected to MainBoard (through 40 pin connector):**
  - 5 pairs of LVDS signals for integrator gain/calibration controls
  - 2 pairs of LVDS signals for charge injection
    - High and low gain independently
  - 3 pairs of LVDS signals for setting the calibration DAC
  - One pair of analog integrator output signals
  - +5V, -5V, ground

- **Connected through 3 cables:**
  - 2 pairs of high/low gain fast PMT signals
    → MainBoard
  - 1 differential pair of signals for analog trigger
    → summing board



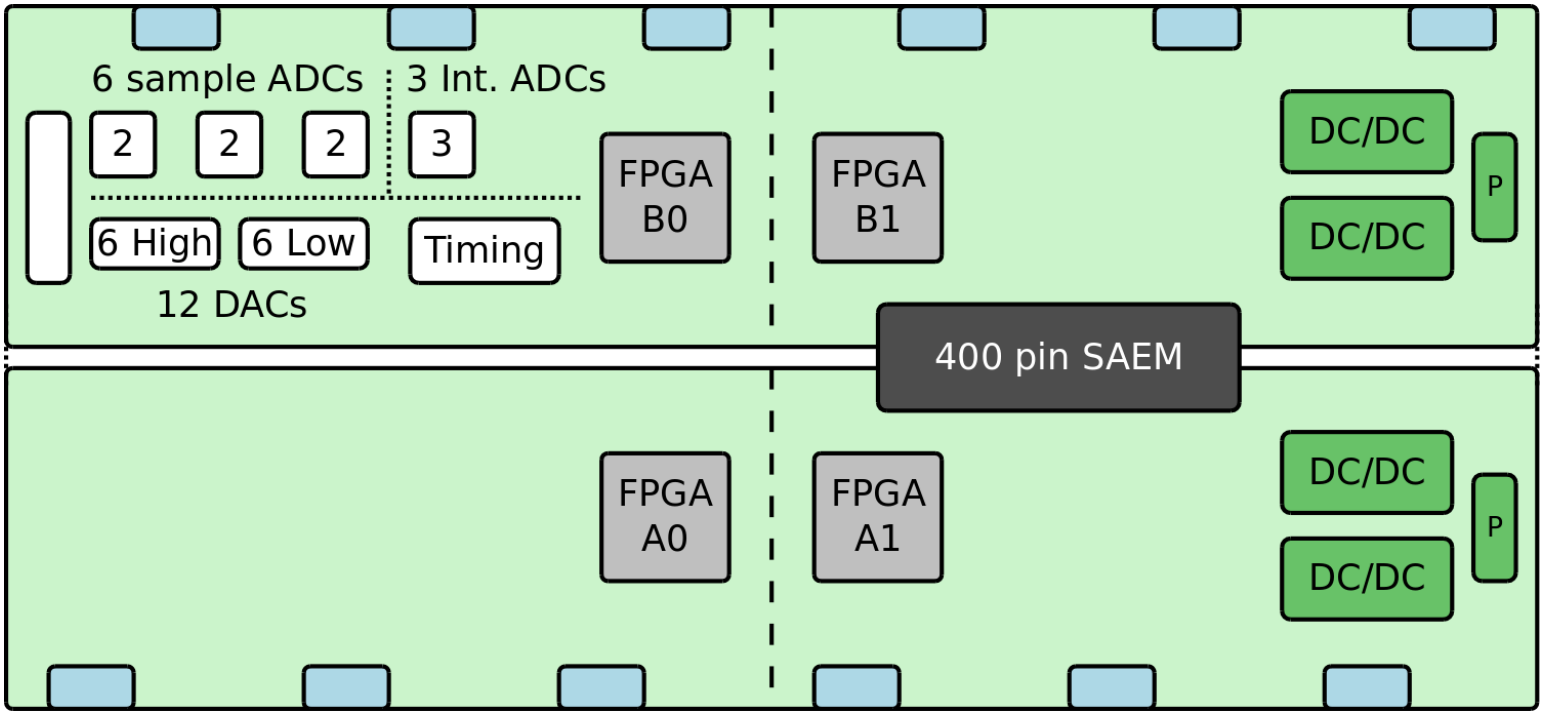
5.2. MainBoard

- **MainBoard:**
  - **Dimensions: 690mm x 100mm (over-sized board)**
  - **14 layers in total including 3 power planes**
  - **Two completely independent sides** (including power supply network)
  - **Connected to twelve 3-in-1 cards (6 on every side)**
  - Four FPGAs for clock distribution and 3-in-1 control
  - Local regulated voltages: +5V, -5V, +2,5V, +1,8V, +1,2V
  - LVDS communication with DaughterBoard at 560Mbps over up to 50cm long traces
  - Voltage monitoring capability
  - Signal lines simulated thoroughly up to 800Mbps



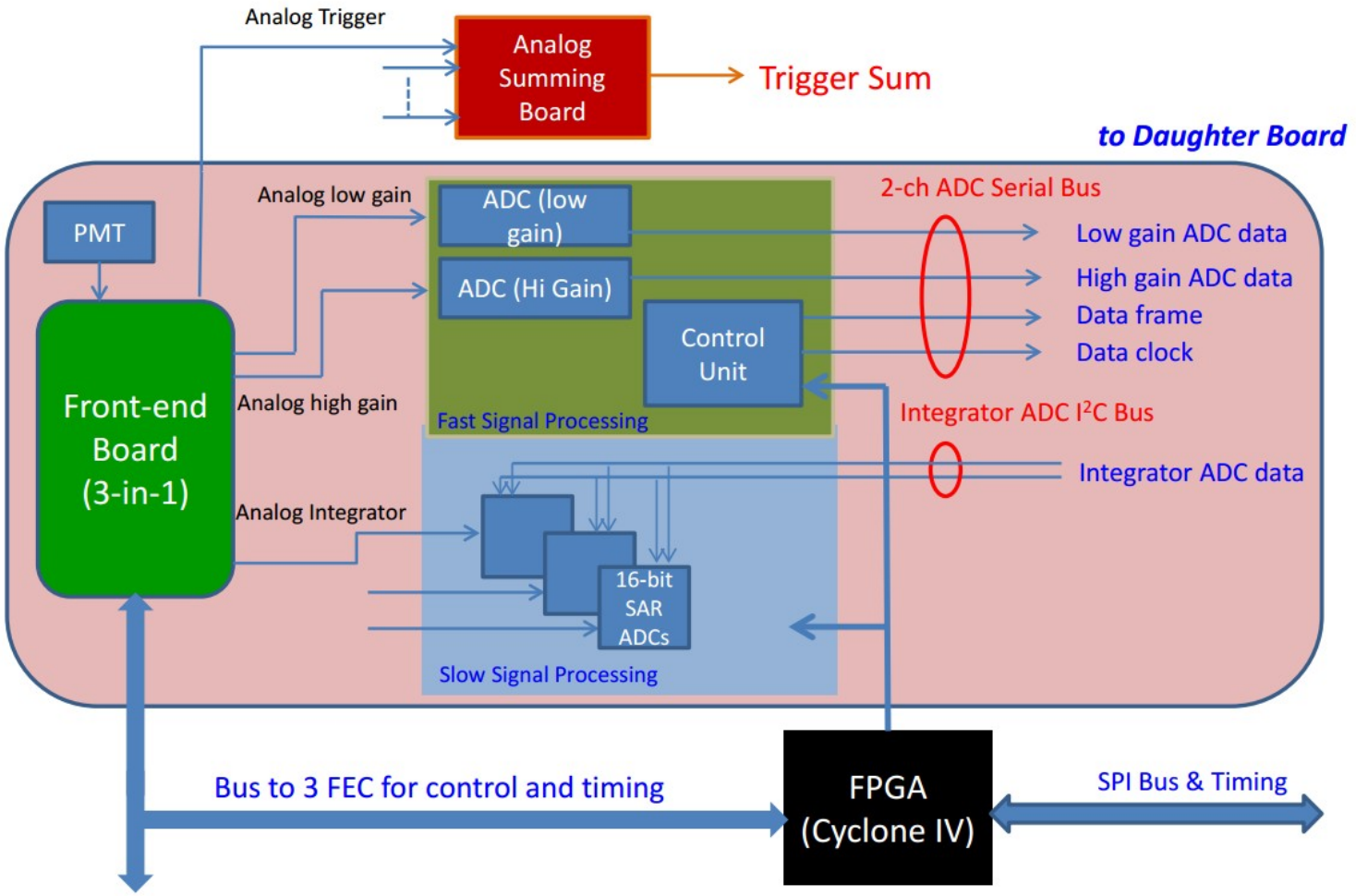
5.2. MainBoard

- **MainBoard – logical partition:**
  - 4 times:
    - 1 Cyclone IV FPGA from Altera
    - 6 ADC for pulse sampling
    - 3 ADC for integration
    - 12 DAC for pedestal correction



5.2. MainBoard

- MainBoard PMT readout data flow



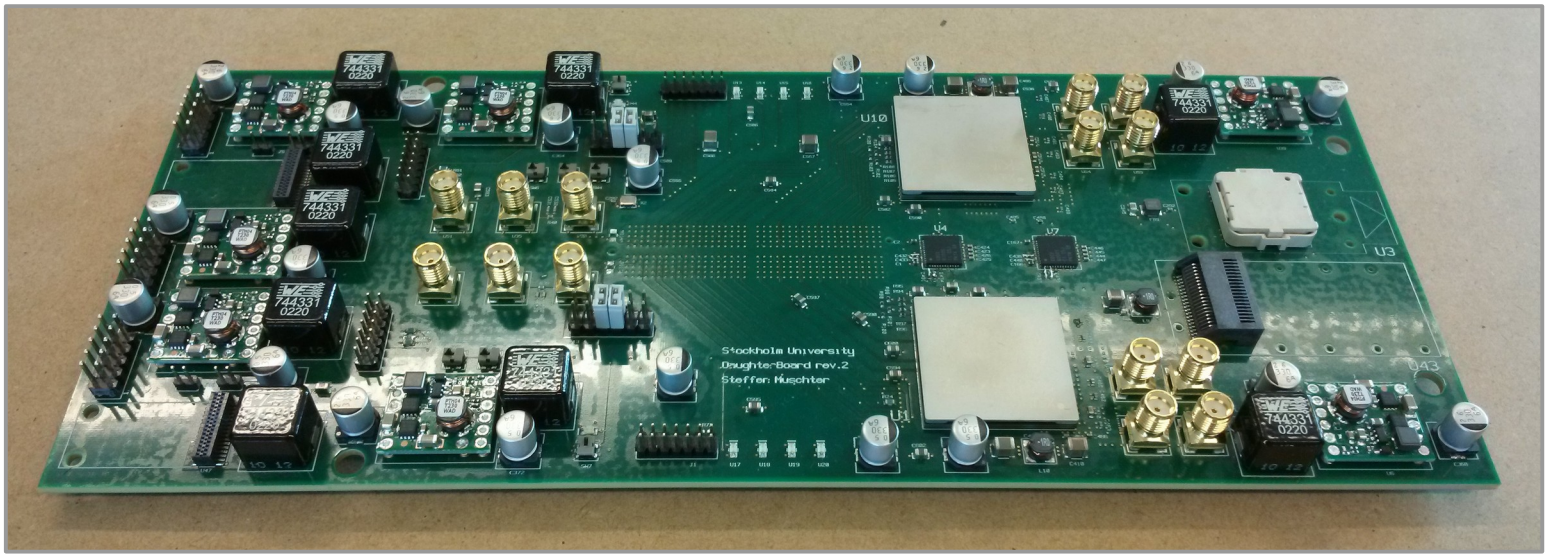
5.2. MainBoard

- **Connected to DaughterBoard (through 400 pin connector):**
  - Dedicated serial buses to read out digitizing ADCs
  - 4 groups of SPI buses one for each MainBoard FPGA
  - 2 groups of LVDS charge injection signals
  - 4 groups of CMOS I2C buses for integrator ADC readout
  - **2 groups of JTAG signals**
  - **6 single-end LV signals (0V to 1V) for low voltage monitoring**
  - LVPS supply voltage (+10V) and ground

	FPGA_B					FPGA_A				
	K	J	H	G	F*	E*	D	C	B	A
1	SUPPLY_K	GND	SUPPLY_H	GND	SUPPLY_F	SUPPLY_E	GND	SUPPLY_C	GND	SUPPLY_A
2	GND	I/O -	GND	clk_I/O -	GND	GND	clk_I/O +	GND	I/O +	GND
3	GND	I/O +	GND	clk_I/O +	GND	GND	clk_I/O -	GND	I/O -	GND
4	I/O -	GND	I/O -	GND	I2C_SDA	I2C_SDA	GND	I/O +	GND	I/O +
5	I/O +	GND	I/O +	GND	ISC_SCL	I2C_SCL	GND	I/O -	GND	I/O -
6	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
7	I/O -	I/O +	clk_I/O -	I/O +	I2C_SDA	I2C_SDA	I/O -	clk_I/O +	I/O -	I/O +
8	I/O +	GND	clk_I/O +	GND	I2C_SCL	I2C_SCL	GND	clk_I/O -	GND	I/O -
9	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
10	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +
11	I/O +	GND	I/O +	GND	I/O +	I/O -	GND	I/O -	GND	I/O -
12	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
13	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +
14	I/O +	GND	I/O +	GND	I/O +	I/O -	GND	I/O -	GND	I/O -
15	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
16	I/O -	I/O +	clk_I/O -	I/O +	I/O -	I/O +	I/O -	clk_I/O +	I/O -	I/O +
17	I/O +	GND	clk_I/O +	GND	I/O +	I/O -	GND	clk_I/O -	GND	I/O -
18	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
19	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +	I/O -	I/O +
20	I/O +	GND	I/O +	GND	I/O +	I/O -	GND	I/O -	GND	I/O -
21	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
22	I/O -	I/O +	I/O -	I/O +	ADC_1	ADC_1	I/O -	I/O +	I/O -	I/O +
23	I/O +	GND	I/O +	GND	ADC_2	ADC_2	GND	I/O -	GND	I/O -
24	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
25	I/O -	I/O +	I/O -	I/O +	ADC_3	ADC_3	I/O -	I/O +	I/O -	I/O +
26	I/O +	GND	I/O +	GND	ADC_4	ADC_4	GND	I/O -	GND	I/O -
27	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
28	clk_I/O -	I/O +	I/O -	I/O +	ADC_5	ADC_5	I/O -	I/O +	I/O -	clk_I/O +
29	clk_I/O +	GND	I/O +	GND	ADC_6	ADC_6	GND	I/O -	GND	clk_I/O -
30	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
31	I/O -	I/O +	I/O -	I/O +	ADC_7	ADC_7	I/O -	I/O +	I/O -	I/O +
32	I/O +	GND	I/O +	GND	ADC_8	ADC_8	GND	I/O -	GND	I/O -
33	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
34	I/O -	I/O +	I/O -	I/O +	TMS_B	TMS_A	I/O -	I/O +	I/O -	I/O +
35	I/O +	GND	I/O +	GND	TCK_B	TCK_A	GND	I/O -	GND	I/O -
36	GND	I/O -	GND	I/O -	GND	GND	I/O +	GND	I/O +	GND
37	clk_I/O -	I/O +	I/O -	I/O +	TDI_B	TDI_A	I/O -	I/O +	I/O -	clk_I/O +
38	clk_I/O +	GND	I/O +	GND	TDO_B	TDO_A	GND	I/O -	GND	clk_I/O -
39	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND
40	SENSE_K	SUPPLY_J	SENSE_H	SUPPLY_G	SENSE_F	SENSE_E	SUPPLY_D	SENSE_C	SUPPLY_B	SENSE_A

5.2. DaughterBoard

- **Current DaughterBoard revision:**
  - Two completely independent sides with
  - Independent power supply
  - Two Kintex7 FPGAs
  - High speed serial communication up to 11.25Gbps
  - Filtered supply voltages for better jitter performance
  - Additional clock circuitry for jitter cleaning



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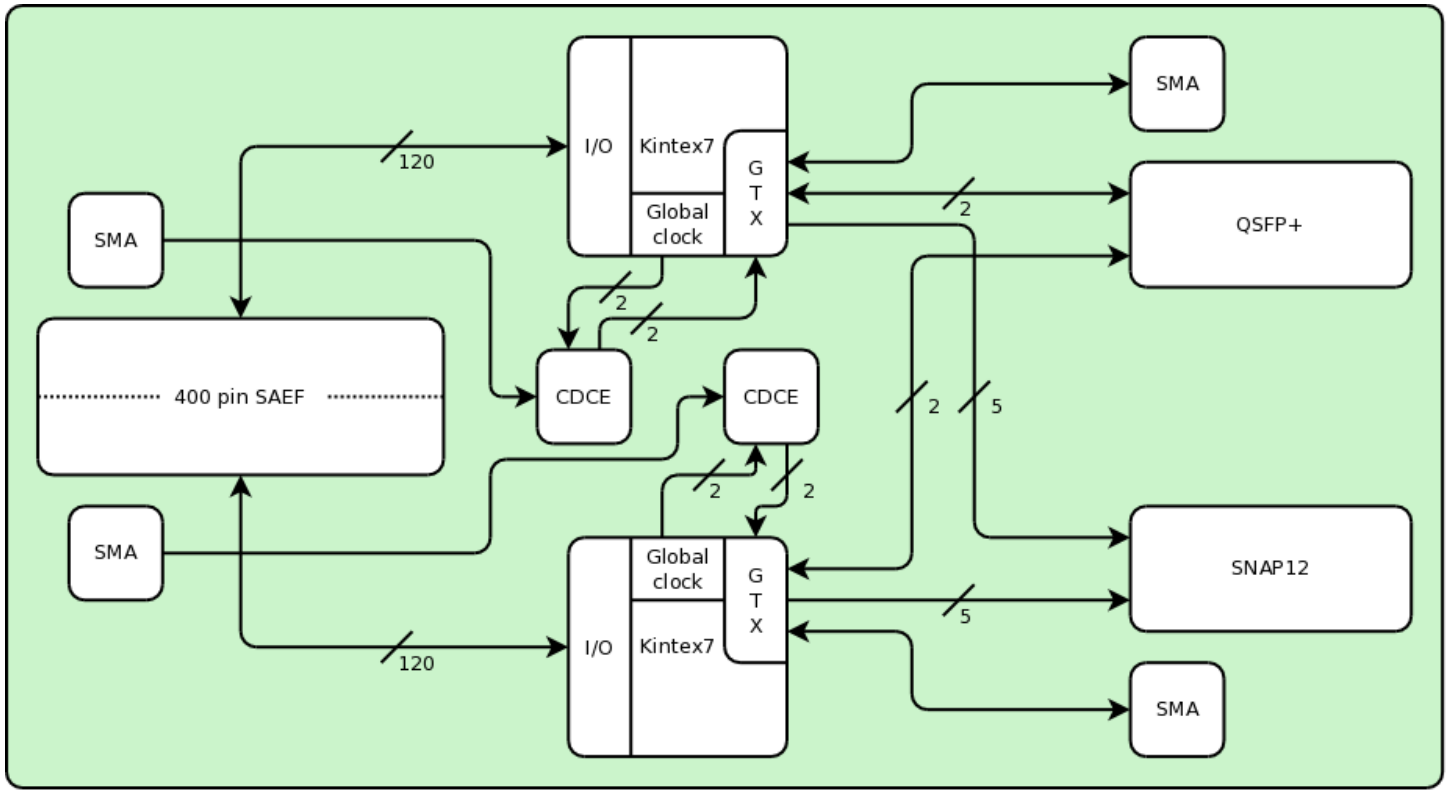
5.2. DaughterBoard

- Current DaughterBoard revision – logical partition:



- There will be no SNAP12 connector on the next revision

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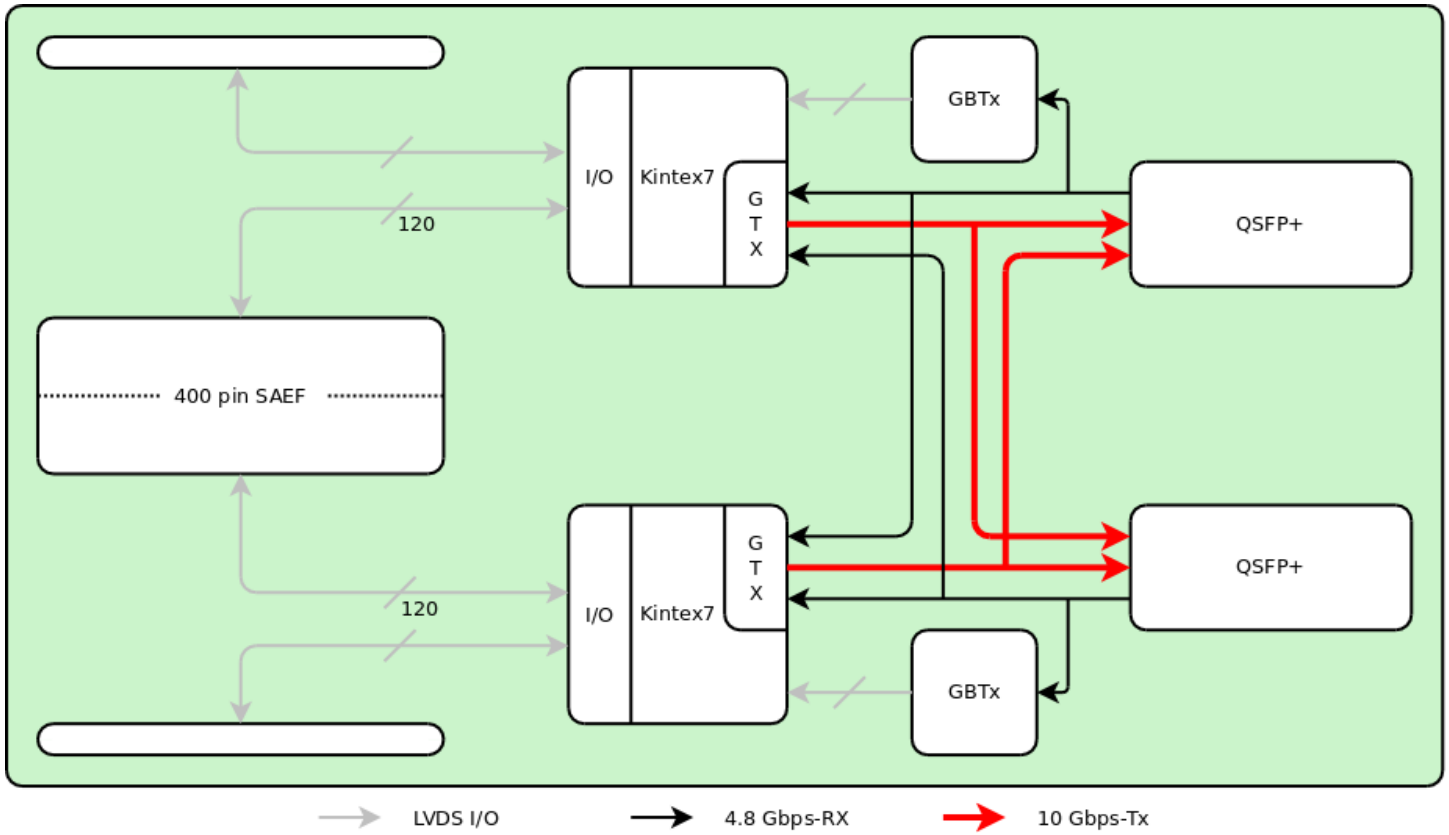
5.2. DaughterBoard

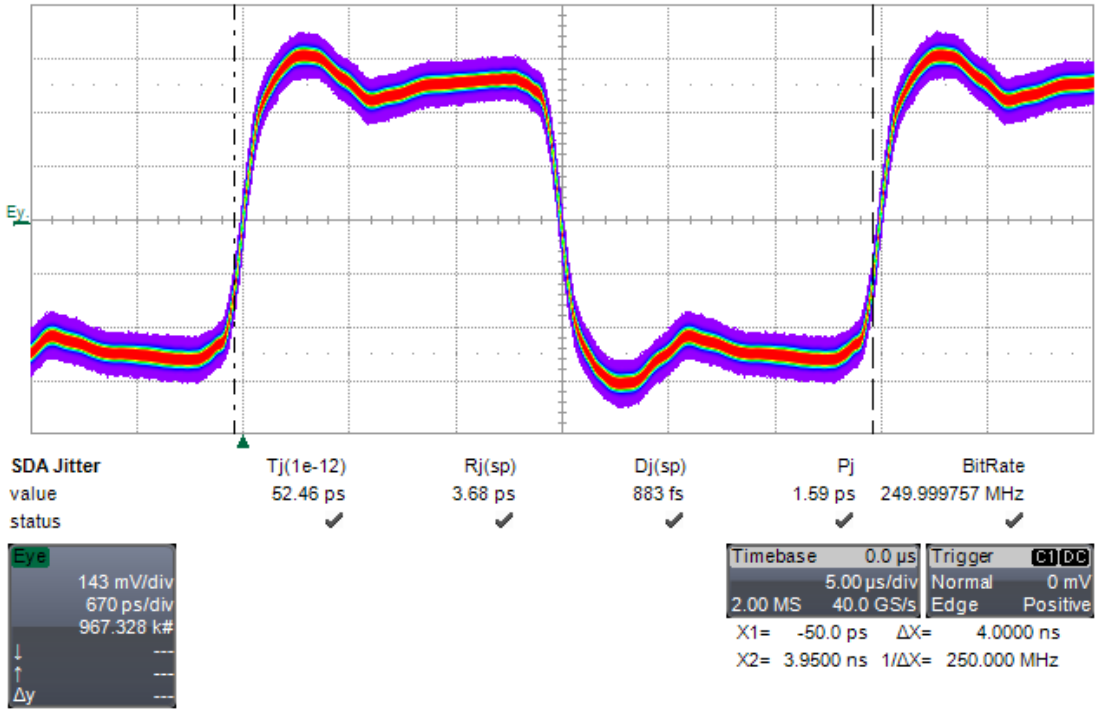
- Final DaughterBoard revision – High-speed communication:
  - Either 4.8 Gbps or 10 Gbps, depending on direction



- Redundantly connected QSFP+ modules
- **Two GBTx for FPGA independent data reception**

5.2. DaughterBoard

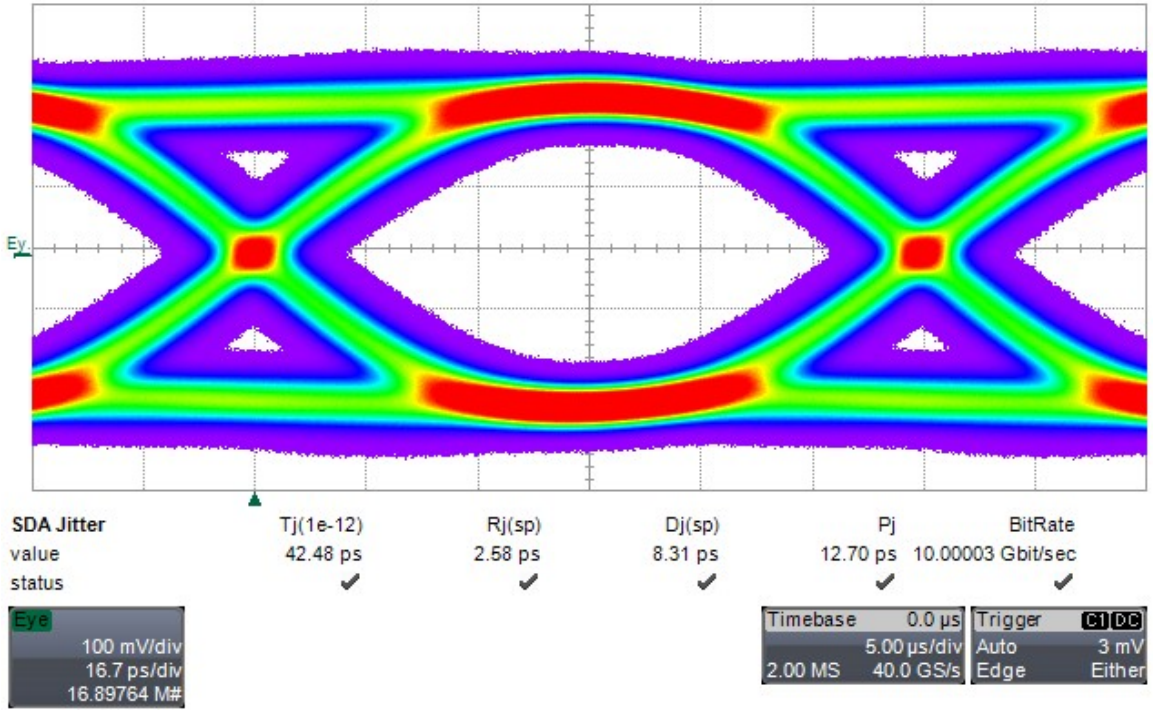
- **DaughterBoard electrical characterization:**
  - High quality clock signals available on the board
  - Either through the IC mounted on the board (CDCE62005)
  - Or through synthesis within the Kintex7
    (better jitter performance due to filtered supply voltages)



CDCE62005 output signal synthesized from 100 MHz input

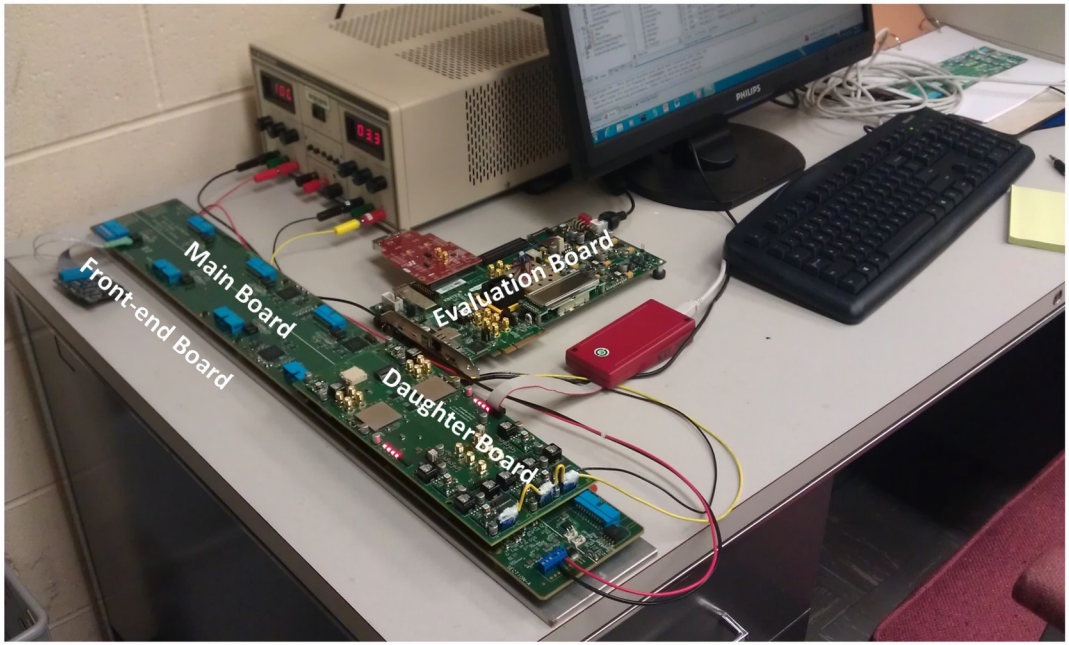
5.2. DaughterBoard

- DaughterBoard electrical characterization:
  - Wide open eye when measuring electrical performance of the Kintex7 gigabit transceivers (GTX)
  - FPGA utilization measurements performed to evaluate impact on GTX performance



6. Test setup

- Example test setup at the University of Chicago for implementing a complete communication chain using:



  - XILINX development board KC705 serves as sROD emulator
  - IPBUS or PCIe will be used for data transmission to a control PC

7. Conclusion

- Current status:
  - Firmware development for DaughterBoard, MainBoard and sROD emulator is ongoing
  - Layout of next revision DaughterBoard is in progress and will be finished soon
  - Radiation tests of 3-in-1 FEB were successfully performed
  - Radiation tests of MainBoard and DaugherBoard are planned and test designs are in development

- Outlook:
  - Radiation tests in October
  - Fully working Demonstrator by the end of the Year
  - Installation of the Demonstrator in the middle of 2014