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Upgraded Readout and Digitizing System for the ATLAS Tile Calorimeter Demonstrator

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During the shutdown of the ATLAS scintillating Tile calorimeter (TileCal) in 2013/14 one of its ondetector electronic modules will be replaced with a compatible hybrid module, which also serves as a demonstrator for future upgrades. This is being built to fulfill all requirements for the complete upgrade of the TileCal electronics in 2022 but augmented to stay compatible with the present system.

We describe a new Front End Board (FEB) that provides amplification and shaping, a Main Board that handles digitization and a high-speed communication Daughter Board. This system will permit us to acquire experience with a future fully digital readout system without disturbing the current analog trigger system.

Summary

In 2022 the LHC will undergo a major upgrade, with the aim to increase the average luminosity to a level more than an order of magnitude larger compared to the nominal value. To respond to the increased event rate it is necessary to provide more information to the early triggers in order to make them more selective. For the TileCal detector system this means directly reading out all information to the counting room rather than just reading out trigger tower data together with data from events selected by the first level trigger. However, this will require a complete redesign of all on- and off-detector electronics. To study how this can be achieved a demonstrator containing a possible (and probable) solution to how the on- and off-detector electronics can be implemented is currently under construction. This demonstrator will replace one module of the detector after the 2013/14 shutdown and run in parallel with the current electronics. The on-detector hardware part will be divided into four types of boards, each one with a dedicated purpose. These are: the Front-End boards, the MainBoard, the DaughterBoard and the High Voltage Power Supply.

The DaughterBoard, developed at Stockholm University, is a key component responsible for the multi gigabit data communication with the off-detector as well as for controlling and monitoring of all the on-detector electronics. To reach the demonstrator goal, the hard- as well as the firmware has to be thoroughly tested, verified and later proven to be sufficient radiation tolerant.

Although a first generation of the DaughterBoard (reported last year) addressed some of the issues much remained to be studied with a second prototype. The hardware features of the second generation DaughterBoard have now been tested and verified, including the electrical characterization of the gigabit transceiver performance at 10Gbps and user IOs at 600Mbps for Single Data Rate (SDR). The firmware was adapted to the upgraded hardware of the second generation, which now included a Kintex7 FPGA and a QSFP+ module for high speed communication. Furthermore the clock layout was revised allowing reception of a 4.8Gbps data stream encoded with the GBT protocol and transmitting data with either 5Gbps or 10Gbps which can be received without losing synchronization with the 40MHz LHC clock. Using this communication framework, loopback tests with different setups were performed using two different custom evaluation boards.

As a result the second generation DaughterBoard is a major step towards a working demonstrator. At this point most of the functionality of the second prototype has been verified and the process of manufacturing a final functional prototype has already started. If proven sufficiently radiation tolerant, this hardware will be used in the TileCal demonstrator project and inserted into the detector in the middle of 2014.

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