A Full Mesh ATCA-based General Purpose Data Processing Board

J. Olsen, T. Liu, Y. Okumura, H. Yin
Fermi National Accelerator Laboratory, P.O. BOX 500, Batavia, IL, 60510, USA

Introduction

High luminosity conditions at the LHC pose many unique challenges for potential silicon-based trigger systems. This is true for both Level-1 and Level-2 trigger applications. Among these challenges is data formatting, where high bit and clock rates from many thousands of silicon modules must first be shared and organized into overlapping c crates of data to be sent to the LHC experiment's main level-1 trigger. To help achieve this goal, a high-bandwidth, low-latency FPGA backplane is required. For this purpose, we have selected the Advanced Telecommunications Computing Architecture (ATCA) platform as it supports a high bandwidth backplane and a robust and reliable industry standard form factor. We have designed our backplane based on the ATCA full-form factor backplane specification to plug in our custom processor boards (FTK).

The Pulsar IIa Prototype

The Pulsar IIa Prototype is a reconfigurable multi-board, multi-processor system designed to meet the requirements of the ATLAS and CMS experiments. The Pulsar IIa is designed around a new system architecture that uses a full mesh backplane for inter-node communications, high-performance FPGAs for data processing, and a 4-core AMD Opteron processor for control and management.

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Pulsar IIa Testing and Results

Our first attempt at designing an ATCA backplane has proven to be quite successful. The FPGAs are driving data at 10Gb/s through the RTM transceivers and achieving a bit error rate of 10^-10.

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Pulsar IIb

Leveraging the experience gained through designing, building and testing the Pulsar IIa, we are in the final stages of integrating it in the next generation board, the Pulsar IIb. The new board design replaces the two Kintex-625T devices with a single single T7 FPGA. The T7 FPGA transceiver count has increased up to 8, allowing for much higher throughput. The FPGAs are connected to the VME F7 card, which contains the VME power supplies and the VME power distribution board. The FPGAs are connected through the backplane bus to the VME F7 card.

Pulsar IIb Features:
- Designed around a single Virtex-7 FPGA. Supported parts are: XC7VX115T, XC7VX145T, XC7VX950T, XC7VX230T. These parts are available with up to 3600 10GBaseT transceivers for full duplex operation.
- Power management block for ATCA level-1 and level-2 trigger applications.
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