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Design of an FPGA-based embedded system for the ATLAS Tile Calorimeter front-end electronics test-bench

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The portable test bench (VME based) used for the certification of the Tile calorimeter front-end electronics has been redesigned for the LHC Long Shutdown (2013-2014) improving its portability. The new version is based on a Xilinx Virtex 5 FPGA that implements an embedded system using a hard core PowerPC 440 microprocessor and custom IP cores. The PowerPC microprocessor runs a light Linux version and handles the IP cores written in VHDL that implement the different functionalities (TTC, G-Link, CAN-Bus) Description of the system and performance measurements of the different components will be shown.

Summary

The architecture of the Tile Calorimeter back-end electronics, as most of the others ATLAS sub-detectors is based on the VME standard. All the functionalities needed for the data read-out and the configuration of the front-end boards and the trigger were designed using this standard.
As it is very common in HEP VME systems were deployed also in the standalone test benches that are used during the LHC shutdowns in the campaign of detector maintenance for the verification and certification of the FE electronics.
A new version of the test bench has been designed and built for the LHC Long Shutdown (2013-2014) with the aim of improving the portability of this tool and to explore new architectures.
The new test bench is based on a commercial Xilinx ML507 development board housing a Virtex 5 FPGA which includes a hard core PowerPC 440 processor. The boards include an SFP optical connector, an Ethernet port 10/100Mbit, USB and serial ports and a huge number of GPIOs.
To manage all the components in an effective way, a complete embedded system has been designed using the hard core PowerPC 440 processor. Custom IP cores are written in VHDL to interface the FPGA with the hardware components connected.
This architecture allows the replacement of the CPU, TTCvi and TTCex VME boards and the ODIN cards used in the previous system using two IP cores which are connected to the SFP module on the board: the Glink and the TTC IP cores. The Glink IP core receives digital data from FE electronics through a GTX transceiver and decodes it similarly as the Agilent HDMP 1034 chipset does in the ODIN card. After decoding the data is stored on a RAM memory until user reads it. The Glink IP core also computes two types of CRC using the received data packet, one for each of the 16 DMU and one for the whole packet.
The TTC IP core generates and handles the TTC commands needed to configure and control the front-end electronics during tests. A VHDL component encodes and multiplexes the desired commands into the A and B channels using the BCM (Biphase Mark Code).
One CAEN V792 VME ADC was used to measure the analog trigger signal in the old system. This is replaced by a custom made ADC board which is controlled through the ADC IP core. This configures the two ADC chips (ADS5271) and handles the data using the Xilinx ISERDES blocks to deserialize the data at a data rate of 480Mbps per channel.
Other custom IP cores are used to control two other custom boards, the PMT High Voltage and a LED driver using GPIOs.
The embedded system runs a light and custom embedded Linux version developed with the ELDK 4.2 toolchain.

All the custom IP cores contains a set of registers connected to the PowerPC processor via the PLB bus, this allow the embedded Linux to manage the hardware in a friendly way.

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